3D electronics
SUNTHARALINGAM Vyshnavi
MIT Lincoln Laboratory-USA

3-D Integrated Circuit Fabrication Technology for High Density Electronics
Vyshnavi Suntharalingam
Brian Aull, Robert Berger, Jim Burns, Chensin Chen,
Jeff Knecht, Chuck Stevenson, Brian Tyrrell,
Keith Warner, Bruce Wheeler, Donna Yost, Craig Keast

12th Workshop on Electronics for LHC and Future Experiments
19th International Workshop on Vertex Detectors
23-29 September 2006

Motivation for 3-D Circuit Technology

- 3-D Circuit = Multi-layer (multi-tier) stacked circuit
- Advantages
  - Reduced interconnect length
  - Reduced chip size
  - Reduced parasitics
  - Reduced power
  - Fabrication process optimized by tier function
- Applications
  - High bandwidth microprocessors
  - Mixed material system integration
  - Advanced focal planes
    - Local computation on-chip memory
    - 10X fill factor diodes

Pad-Level “3D Integration”
Die Stacking

Stacked-Die Wire Bonding
Stacked Chip-Scale Packages

ChipPAC, Inc.
Tessera, Inc.

In Production!

Pixel-Level 3-D Integration
Cross Sections Through Two-Tier Imager

Limitations – Standard Bulk CMOS APS
Monolithic APS – MAPS

- Fill factor compromised
  - Photodetector and pixel transistors share same area
- Low photoresponsivity
  - Shallow junctions
  - High doping
  - Limited depletion depth
- High leakage
  - LOCOS/STI, salicide
  - Transistor short channel effects
- Substrate bounce and transient coupling effects

Outline

- Advantages of Vertical Integration for Focal Planes
  - MIT-LL Demonstration of Three-tier ring oscillators
- Fabrication Sequence
- MIT Lincoln Laboratory Demonstrations
  - Two-tier backside-illuminated visible imager
  - Three-tier laser radar focal plane
  - Three-tier 3-D IC Multiproject Run
  - Two-tier bonding and interconnection to InP detector material
- Summary
Advantages of Vertical Integration

- Pixel electronics and detectors share area
- Fill factor loss
- Co-optimized fabrication
- Control and support electronics placed outside of imaging area

3-D Pixel

- 100% fill factor detector
- Fabrication optimized by layer function
- Local image processing
- Power and noise management
- Scalable to large-area focal planes

Approaches to 3D Integration

(BPhotos Shown to Scale)

- Bump Bond used to flip-chip interconnect two circuit layers
- Two-layer stack with insulated vias through thinned bulk Si
- Three-layer circuit using Lincoln's SOI-based vias

3-Tier, 3D-Integrated Ring Oscillator

(DARPA 3D1 Multiproject Run)

- Functional 3-tier, 3D-integrated ring oscillator
  - Uses all three active transistor layers, 10 levels of metal and experimental stacked 3D-vias
  - Demonstrates viability of 3D integration process

Outline

- Advantages of Vertical Integration for Focal Planes
- Fabrication Sequence and Five Key Elements
  - Low dark current photodiodes
  - Silicon on Insulator (SOI) circuits
  - Low-temperature, wafer-scale oxide-to-oxide bond
  - Precision overlay
  - High-density vertical interconnection
- MIT Lincoln Laboratory Demonstrations
  - Three-tier ring oscillators
  - Two-tier backside-illuminated visible imager
  - Three-tier laser radar focal plane
  - Three-tier 3-D IC Multiproject Run
  - Two-tier bonding and interconnection to InP detector material
- Summary

3-D Circuit Integration Flow-1

- Fabricate circuits on SOI wafers
  - SOI wafers greatly simplify 3D integration
- 3-D circuits of two or more active silicon layers can be assembled

1. Low Dark Current Photodiodes

- Photodiode independent of CMOS
- High-resistivity substrates
- Back-illumination process
- Photodiode leakage <0.2nA/cm² @ 25°C
- Similar results after 3D-stacking
2. Silicon-On-Insulator Circuits

- 3.3-V, 350-nm gate length, fully depleted SOI CMOS
- Buried oxide
  - Dielectric isolation
  - Reduced parasitic capacitances
  - Enhanced radiation performance
  - Essential wafer-thinning etch stop

3-D Circuit Stacking

- Invert, align, and bond Tier 2 to Tier 1
- Oxide-Oxide Wafer Bond

3-D Circuit Stacking

- Remove handle silicon from Tier-2

4. Precision wafer-to-wafer overlay

- Provide a wafer-to-wafer alignment accuracy compatible with a submicron 3D Via
- Tool based on modern IC wafer stepper technology
- 0.5 μm 3-sigma overlay demonstrated

3. Low Temperature Oxide Layer-to-Layer Bonding

- Deeply scaled 3-D interconnect technology requires robust wafer-to-wafer bonding technology
- MIT-LL low temperature oxide bonding process provides
  - Thin and controllable bondline
  - Enables use of standard IC high aspect ratio contact etch and plug fill technologies
  - ~475°C process
  - Allows for 3-D interconnect to be sintered
  - Standard, high reliability semiconductor material

Repeatability Data

- MIT-LL Precision Aligner

- Data from five repeated alignments of same wafer pair
- Nine die measured per alignment
### 3D Via Layout Comparison
*(Based on MIT-LL 180nm FDSOI CMOS rules)*

**Previous capability**

- 3D via landing pad: 5.5 μm
- 3D via: 2.0 μm
- Inner metal via: 0.6 μm

**With recently developed precision alignment system and via technology**

- 3D via landing pad: 2.0 μm
- 3D via: ~1.0 μm

### Bonded Two Wafer Imager Stack

150-mm Diameter Wafer Pair

### Inter-Tier Via Connections

- Pattern, etch, and fill 3-D vias
- (Additional circuit tiers could be added)

### Thermal Cycle Effects on 3D-Via Chains

**Thermal Cycle: 300 K/77 K/300 K**

<table>
<thead>
<tr>
<th># of 3D Vias in Series</th>
<th>Total Resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1000</td>
<td>1000</td>
</tr>
<tr>
<td>2000</td>
<td>2000</td>
</tr>
<tr>
<td>3000</td>
<td>3000</td>
</tr>
<tr>
<td>4000</td>
<td>4000</td>
</tr>
<tr>
<td>5000</td>
<td>5000</td>
</tr>
<tr>
<td>6000</td>
<td>6000</td>
</tr>
<tr>
<td>7000</td>
<td>7000</td>
</tr>
<tr>
<td>8000</td>
<td>8000</td>
</tr>
<tr>
<td>9000</td>
<td>9000</td>
</tr>
<tr>
<td>10000</td>
<td>10000</td>
</tr>
</tbody>
</table>

### 5. High Density, High Yield, Compact 3D-Via

- Leverages standard high-yield IC process technology for 3D interconnection
  - High density plasma oxide etch of via hole
  - Chemical vapor deposition of tungsten plug
  - Chemical mechanical planarization (CMP) to form damascene plug

### Back Metal-1 and Back Metal-2

- Deposit and pattern Back Metal-1
- Deposit and CMP ILD
- Deposit and pattern Back Metal-2
- Sinter
Completed Back-Illuminated CMOS Imager

- Thin photodiode substrate to 50μm
- Epoxy bond to quartz

Outline

- Advantages of Vertical Integration for Focal Planes
- Fabrication Sequence
- MIT Lincoln Laboratory Demonstrations
  - Three-tier ring oscillators
  - Two-tier backside-illuminated visible imager
  - Three-tier laser radar focal plane
  - Two-tier 3-D IC Multiproject Run
  - Two-tier bonding and interconnection to InP detector material
- Summary

Four-Side Abutable Goal

- 3-D CMOS imagers tiled for large-area focal planes
- Foundry fabricated daughter chip bump bonded to non-imaging side

Four-Side Abutable Vertically Integrated Imager

- Silicon photodetector layer (Tier-1)
  - Four-side abutable 1024 x 1024 array of 8μm x 8μm pixels
- Address and readout layer (Tier-2)
  - 3.3 volt FDSOI CMOS layer
- Timing, control, and analog-to-digital electronics (Tier-3)
  - 1MBSI fabricated chip bump bonded to detector array
- Active-pixel architecture for radiation tolerance

Design Goals

- Four-side abutable Active Pixel Sensor
- 1024 x 1024 array of 8μm x 8μm pixels
- 3-D interconnections per pixel
- 3.3-V operating voltage
- Full digital control and readout at 10 fps

Completed 3D-Stacked Imager
Wafer and Die Layout

- 150mm wafer
- 1024 x 1024 pixels per cap
- 22 mm
- Processing: Wafer bumps, die attach, cap, and test

35
3T Pixel Schematic and Layout

- Design Variations
  - pFET Reset with 15fF capacitor
  - nFET Reset with no capacitor

1024 x 1024 Imager Array Architecture

Preliminary Tier-1-2 3D Imager Test Results

- Electrical probe station preliminary imager test result using frontside illumination
  - Final processing steps will result in unobstructed backside illuminated device

Sample Dark Background

- Raw image without fixed pattern noise suppression
- Dominant yield detractor is row/column drop-outs

Four-Side Abutable Vertically Integrated Imaging Tile

- Wafer-Scale 3D circuit stacking technology
  - Silicon photodetector tier
  - SOI-CMOS address and readout tier
  - Per-pixel 3D interconnections
  - 1024 x 1024 array of 8 μm x 8 μm pixels
  - 100% fill factor
  - >1 million vertical interconnections per imager

Outline

- Advantages of Vertical Integration for Focal Planes
- Fabrication Sequence
- MIT Lincoln Laboratory Demonstrations
  - Three-tier ring oscillators
  - Two-tier backside-illuminated visible imager
  - Three-tier laser radar focal plane
  - Three-tier 3-D IC Multiproject Run
  - Two-tier bonding and interconnection to InP detector material
- Summary
Three-Tier Laser Radar Focal Plane

- Based on single-photon-sensitive Geiger-mode avalanche photodiodes
  - 64 x 64 demonstration circuit (scalable to larger imager formats)
  - Pixel size reduction from 100 μm to 30 μm
  - Timing resolution reduction from 1 ns to 0.1 ns
  - 100x reduction in voxel volume

Functional 3D-Integrated, 3-Tier Avalanche Photodiode Focal Plane

- VLSA laser radar focal plane based on single-photon-sensitive Geiger-mode avalanche photodiodes
  - 64 x 64 format
  - 60-μm pixel size

64x64 LADAR Focal Plane

- Rudimentary Ladar image of 28° long cone with 8-in timing resolution
  - Timing circuit limited to only 8-bits of its full 12-bit range

3-D IC Multiproject Run Completed

- MIT-LL 3D circuit integration technology
- Preliminary 3D design kits developed
  - Mentor Graphics – MIT-LL, Cadence – NCSU
  - Thermal Models – CFRCC
- Design guide release 11/04, fab start 6/05, 3D-integration complete 3/06

Cross-Section of 3-Tier 3D-integrated Circuit

- DARPA 3DL1 Multi-project Run
- 3 FDSOI CMOS Transistor Layers, 10-levels of Metal

Outline

- Advantages of Vertical Integration for Focal Planes
- Fabrication Sequence
- MIT Lincoln Laboratory Demonstrations
  - Three-tier ring oscillators
  - Two-tier backside-illuminated visible imager
  - Three-tier laser radar focal plane
  - Three-tier 3-D IC Multiproject Run
  - Two-tier bonding and interconnection to InP detector material
- Summary
3D Technology Improvements
(DARPA 3DL1 Multiproject Run)

- 3D technology enhancements successfully demonstrated in 3DL1 Run
  - Stacked 3D-vias for electrical and thermal interconnect
  - 2X reduction in 3D-via size
  - Improved tier-to-tier overlay

- High-Yield on x400x-link Scaled 3D-via Chains

- 0.5 µm 3D Tier-to-Tier Registration

- Stack 3D vias demonstrated
  - >90% yield on 4800 tiers chains
  - Stacked 3D via resistance ~1Ω
  - Can be used as thermal vias

Summary

- MIT Lincoln Laboratory-developed 3D circuit integration technology has been applied to advanced focal planes and three-tier computational circuits

  - Successful demonstrations:
    - Two-tier visible imager: 1056x1056 array of 8µm x 8µm pixels integrated to 100% fill factor photodiodes, backside illuminated
    - Three-tier ring oscillators in 180-nm gate length technology
    - Three-tier laser radar focal plane: 64x64 array of Geiger-mode avalanche photodiodes with per-pixel timing and bias circuitry
    - Three-tier 3-D IC Multiproject Run in 180-nm gate length technology
    - Two-tier bonding and interconnection to SWIR-sensitive detector materials (InP)

Silicon to InP Wafer Bonding

- Successful demonstration of 3D-bonding of SOI CMOS circuit layer to InP handle wafer

- Enables extension of 3D-integration technology to higher density, longer wavelength focal plane detectors
  - Tight pixel-pitch IR focal planes and APD arrays
  - InGaAsP (1.06-µm), InGaAs (1.55-µm)

- Oxide-bonded circuit layer transferred from silicon wafer

150-mm-diameter InP Wafer

MIT Lincoln Laboratory