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HIGH SPEED SYNCHRONIZATION MODULE IMPLEMENTED IN ALTERA STRATIX II FPGA

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Abstract

These papers present programmable FPGA-based divider of high frequency reference signal dedicated to generate various frequencies for synchronization of particle accelerator subsystems. The digital circuit was synthesized using pure VHDL description thus can be implemented not only in target ALTERA Stratix II high-speed FPGA chip but others FPGAs as well. The implemented circuit operates up to the FPGA frequency limit of 500 MHz. The generated frequency signals can be time shifted by programmable multiplicity of the clock period (2ps) without introducing additional phase skew to the output signals.

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KEYWORDS: FPGA, VHDL, radio frequency, programmable divider

Abstract: These paper presents programmable FPGA-based divider of high frequency reference signal dedicated to generate various frequencies for synchronization of particle accelerator subsystems. The digital circuit was synthesized using pure VHDL description thus can be implemented not only in target ALTERA Stratix II high-speed FPGA chip but others FPGAs as well. The implemented circuit operates up to the FPGA frequency limit of 500 MHz. The generated frequency signals can be time shifted by programmable multiplicity of the clock period (2ps) without introducing additional phase skew to the output signals.

INTRODUCTION

High-energy accelerators use Radio Frequency (RF) field to accelerate charged particles. The various subsystems of accelerator control require various synchronization signals. These signals are generated from high frequency master oscillator clock (in RF range) by division in high-speed frequency dividers. For that purpose currently the very fast ECL logic circuits are used. They must be carefully designed in order to obtain low phase skew on various outputs and are difficult to modify. Application of FPGA for that purpose is much more convenient since the flexibility of FPGA enables fast and easy modification of circuit parameters. The block diagram of the synchronization module is presented in Fig. 1.

Fig. 1 Synchronization module block diagram

The reference frequency signal is an asymmetrical 500MHz sinusoidal waveform. It is converted into symmetrical one with LVDS levels in RF level translator and connected to the FPGA. The FPGA circuit contains several frequency dividers with constant dividing factors and multiplexer selecting required

signal. Two outputs drive the same frequency signal but the delayed one shifts it in time by chosen number of input clock periods. User can do the selection of output frequency by setting multiplexer inputs by an external DIP switch and choose phase shift between both output signals through asynchronous serial receiver.

HIGH SPEED ECL TO LPECL DIFFERENTIAL SIGNAL RECEIVERS

The high frequency reference signal is accessible as a 500MHz sinusoidal waveform with 0dbm level. The digital FPGAs can handle only digital signals thus the synchronization module requires the sinusoidal/digital waveform converter at the input. For such high frequencies the differential signals standards are usually used. The Altera Stratix II can handle several differential signal standards (LVDS, LVPECL and others).

The sinusoidal/digital waveform converter was designed using ECL to LPECL/LVDS Micrel EL16V [1,2] differential receiver (Fig. 2). The sinusoidal input signal was fitted by RF transformer to the ECL standard levels and was driving inputs of EL16V.

Fig. 2 Schematic diagram of the RF input module

The Micrel EL16V differential receiver is 5/3.3 V input tolerant and thus can accept analogue input signals. The signal propagation time is about 250 ps but this parameter is not crucial for our application. The maximum signal frequency of 4 GHz is much higher than required 500 MHz.

All inputs and outputs of RF module are terminated with 50 Ω resistors [3]. It was also necessary to add 50 Ω resistor between non-inverting output and inverting input of EL16V receiver to avoid self-oscillations on the device outputs.

THE IMPLEMENTATION OF SYNCHRONIZATION MODULE

The synchronization module requires seven frequency dividers with constant division factor. All required values of those factors are collected in Table 1.

TABLE 1. Division factors for frequency dividers

Ch. №	Division factor	Decomposition into prime numbers
1.	10560	$2^6 \cdot 3 \cdot 5 \cdot 11$
2.	4400	$2^4 \cdot 5^2 \cdot 11$
3.	3840	$2^8 \cdot 3 \cdot 5$
4.	1100	$2^2 \cdot 5^2 \cdot 11$
5.	482	$2 \cdot 241$
6.	480	$2^5 \cdot 3 \cdot 5$
7.	48	$2^4 \cdot 3$

The frequency divider by odd number n can be realized as a counter that counts clock pulses until it reaches maximum value $(n/2-1)$ and then resets. Every counting cycle the output signal from the counter is toggled (Fig. 3). The duty cycle of output signal is always 50%.

Fig. 3 Frequency division by 6 using counter mod 3

The division by even numbers is more complicated. For that purpose one can use counters that are reset or loaded with 1 in successive counting cycles (depending on output value – Fig. 4). It is also possible to use other components (e.g. rotating registers containing sequence of 0's and 1's – Fig. 5). The output signal duty cycle in the case of division by even number is not 50%.

Fig. 4 Frequency division by 5 using counter mod 3 reloaded with $n=0$ when $out=1$ and $n=1$ when $out=0$

Fig. 5 Frequency division by 5 using rotating register

The counters require data register and ALU calculating the increment (the adder). It is necessary to remember that adders introduce speed limitation from carry chain that restricts the adder (and counter) length for given operating frequency. For counting frequency of 250MHz (since the input frequency of 500MHz can be in every case listed in Table I simply divided by 2 in a T type flip-flop) the counter length is limited to 6 bits for ALTERA Stratix II [4,5].

Fig 6 The block diagram of the divider module (direct implementation)

The block diagram of the direct implementation of the divider module consisting of all dividers is presented in Fig. 6. The design requires in total 23 dividers. The frequency dividers by 2 can be realized in hardware by T type flip-flops. Division by other number has to be implemented by counter or other methods. One can notice that the structure of the module can be optimized using slightly different order of division factors. The optimized structure of the divider module is presented in Fig. 7. The total number of dividers is 19.

Fig. 7 Optimized structure of the divider module

The input clock signal is initially divided by 2. That decreases the operating frequency of further components to 250MHz.

The decomposition into product of prime numbers of all required frequency division factors shows that the most problems with circuit synthesis are expected in the case of divider by 482. This case requires application of divider by 241 which is a prime number. Other division factors in table 1 requires only divisions by small numbers in the range of 2÷11.

The TABLE 1 shows that frequency divider module can be realized in many ways using various design strategies. Some design solutions that could give different implementation results are collected in

TABLE 2. The first three methods (A, B and C) use only counters. The division factors were grouped differently in each case in order to check the resource consumption. The fourth method (D) uses rotating registers. This method is not dependent on adder speed but it consumes many FPGA resources for registers. The last method of circuit implementation (E) mixes counters and registers and uses counters wherever they are fast enough and rotating registers in other cases. This method is an optimal one (in the sense of fulfilling design requirements and consumption of the FPGA resources).

TABLE 2. Division factors for frequency divider

Ch. №	Division factor	Prime numbers decomposition	Method A (counters)	Method B (counters)	Method C (counters)	Method D (rotating registers)	Method E (mixed)
1.	10560	$2^6 \cdot 3 \cdot 5 \cdot 11$	$2^5 \cdot 330$	$2^3 \cdot 6 \cdot 10 \cdot 22$	$22 \cdot 10 \cdot 6 \cdot 8$	10560	
2.	4400	$2^4 \cdot 5^2 \cdot 11$	$2^3 \cdot 550$	$2 \cdot 10 \cdot 10 \cdot 22$	$22 \cdot 10 \cdot 10 \cdot 2$	4400	
3.	3840	$2^8 \cdot 3 \cdot 5$	$2^7 \cdot 30$	$2^5 \cdot 6 \cdot 10$	$10 \cdot 6 \cdot 32$	3840	
4.	1100	$2^2 \cdot 5^2 \cdot 11$	$2 \cdot 550$	$22 \cdot 50$	$50 \cdot 22$	1100	
5.	482	$2 \cdot 241$	$2 \cdot 241$	482	482	482	
6.	480	$2^5 \cdot 3 \cdot 5$	$2^4 \cdot 30$	$2^4 \cdot 30$	$30 \cdot 16$	480	
7.	48	$2^4 \cdot 3$	$2^3 \cdot 6$	$2^3 \cdot 6$	$6 \cdot 8$	48	

TABLE 3. Comparison of FPGA utilization

Resource	Method A (counters)	Method B (counters)	Method C (counters)	Method D (rotating registers)	Method E (mixed)
Logic cells	90	109	112/	27	43
Registers	296	72	73	20911	2601
Global CLKs	7	12	10	2	9
LUTs	332	115	119	20925	2618
Fmax [MHz]	431,22	462,11	455,79	591,02	585,82

The most difficult to implement part of the divider module was the divider by 241. As it was expected the length of the counter and the high frequency of its operation makes synthesis of the circuit impossible. The maximum operating frequency in each case when the divider by 241 was realized as a counter was lower than required 500MHz. There was not big difference between various methods using only counters. The FPGA resource utilization is quite small for A-C methods. One can notice that those methods consume a few global clocks (7-12).

The method using rotating registers gives the best performance ($f_{\max} > 591.02\text{MHz}$) but consumes a lot of FPGA resources (over 20k LUTs). It does require only 2 global clocks. The last method (mixed one) provides required speed while consumes only a little bit more resources than methods using only counters.

THE IMPLEMENTATION OF VARIABLE OUTPUT DELAY

The synchronization module has two outputs with same signals shifted in time by variable offset. The time offset between those outputs must be adjusted by the user. The variable delay can be realized as a chain of D-type flip-flops with adjusted length. The idea is to use multiplexers that allow the signal to skip part of the flip-flop chain. They have to be configured in a way that successive multiplexers skip a power of 2 (1, 2, 4, 8 ...) number of flip-flops. That allows selecting any signal delay. The block diagram of the output delay circuit is presented in Fig. 8.

Fig. 8 Delaying registers block diagram

The offset in the form of 16bit long number is transmitted to the circuit through serial interface from PC compute and stored in internal register DLR (Delay register). Each bit of the DLR controls 2 in 1 multiplexer and when this bit is set the multiplexer directs the signal in delayed output through additional shift register of length depending on bit position in DLR (Fig. 8). However the multiplexers in the delayed signal path introduce additional latency absent in direct signal path that introduce skew between those outputs and limit operating frequency. This can be easily noticed in the case when all bits of DLR are cleared – the delayed path consists of a chain of combinational multiplexers with non-zero propagation time while the direct path does not consist of any latency. Therefore each multiplexer in the delayed signal path is buffered by a latch introducing one clock cycle delay and the direct signal path is delayed by the same amount of clock cycles by a shift register. This way allows obtaining low skew between direct and delayed output signals together with high operating frequency.

CONCLUSIONS

This paper presents a prototype of high-speed synchronization module realized in Altera Stratix II FPGA. The maximum operating frequency exceeds required 500MHz while the circuit consumes only a small amount of FPGA resources leaving space for other applications. The design was built and tested in real

operating environment and performed tests proved the proper operation of the device.

Several implementation methods of the circuit were tried out. The synthesized circuits were analyzed using Altera Quartus II 4.1 Timing Analyzer design tool [6]. The high operation frequency of the circuit was a real challenge and forced to use special design strategies and optimization.

The high-speed digital circuits require careful design. The sinusoidal/digital waveform converter was not easy to build on the experimental PCB board. All the parasitics had to be compensated in order to obtain stable operation.

The most important conclusion is that modern FPGAs allow operating in the RF frequency range. The flexibility of FPGAs-based circuits is much higher than fixed-structure ASICs or discrete element circuits. However, the VHDL circuit description has to be carefully designed and optimized – many problems occur that are not important for lower operating frequency circuits.

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REFERENCES

- [1] High speed differential receiver distributor home page, <http://micrel.com/index.do>
- [2] EL16V reference manual link, <http://www.micrel.com/page.do?page=/product-info/products/sy10-100el16v.shtml>
- [3] Termination techniques for RF drivers, <http://www.pericom.com/pdf/applications/AN036.pdf>
- [4] FPGA distributor home page, <http://www.altera.com/>
- [5] Stratix II FPGA reference manual, <http://www.altera.com/literature/lit-stx2.jsp>
- [6] Quartus II User Manual, 2004 Altera Corporation