PROCEEDINGS

OF THE TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS

Naxos, Greece, 15–19 September 2008

Organized by

National Technical University of Athens (NTUA)
National and Kapodistrian University of Athens (NKUA)
University of Ioannina (UOI)
National Centre for Scientific Research Demokritos (NCSRD)
Aristotelean University of Thessaloniki (AUTH)

with support from CERN, the European Organization for Nuclear Research

GENEVA
2008
ABSTRACT

The purpose of the workshop was to present results and original concepts for electronics research and development relevant to particle physics experiments as well as accelerator and beam instrumentation at future facilities; to review the status of electronics for the LHC experiments; to identify and encourage common efforts for the development of electronics; and to promote information exchange and collaboration in the relevant engineering and physics communities.
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National Technical University of Athens (NTUA)
National and Kapodistrian University of Athens (NKUA)
University of Ioannina (UOI)
National Centre for Scientific Research Demokritos (NCSRD)
Aristotelean University of Thessaloniki (AUTH)

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Thijs WIJNANDS CERN
Marc WINTER IRES
Ray YAREMA FNAL

Workshop Secretariat and Proceedings Editors

Evelyne DHO & François VASEY CERN
OVERVIEW

The purpose of the workshop was

- to present results and original concepts for electronic research and development relevant to particle physics experiments as well as accelerator and beam instrumentation at future facilities
- to review the status of electronics for the LHC experiments
- to identify and encourage common efforts for the development of electronics
- to promote information exchange and collaboration in the relevant engineering and physics communities.

The main subjects of the workshop were recent research and developments in the following areas relevant to particle physics experiments:

- Electronics for Particle Detection, Triggering and Acquisition Systems
- Electronics for Accelerator and Beam Instrumentation
- Custom Analog and Digital Circuits
- Applications of Programmable Digital Logic
- Optoelectronic Data Transfer and Control
- Packaging and Interconnect Technologies
- Radiation and Magnetic Tolerant Components and Systems
- Production, Testing and Reliability
- Power Management and Conversion
- Grounding, Shielding and Cooling
- Design Tools and Methods

The welcome address was given by François VASEY chairperson of the programme committee, and the introduction was given by Manolis DRIS.

One full workshop day was devoted to LHC Upgrades (Topical sessions 1 and 2). This took the form of a number of invited and contributed presentations followed by a discussion.

Three dedicated working group meetings were held, one on microelectronics, one on optoelectronics and one on power conversion and management.

An optional tutorial took place on the Friday afternoon following the workshop. Larry G. Edson lectured on Designing Printed Circuit Boards Not To Fail.
PLENARY SESSIONS

Plenary session 1 - High Energy Physics in Greece, Chaired by Manolis DRIS

An overview of the Experimental High Energy Activity in Greece PETRIDOU, Chara
Greek Contribution to the ATLAS Experiment KOURKOUMELIS, Christine
CMS in Greece MANTHOS, Nikolaos

Plenary session 2 - Opening plenary, Chaired by François VASEY

NESTOR participation in the KM3NeT ANASSONTZIS, Efstratios
The European XFEL Project TRUNK, Ulrich
Development of a 3.2 GPixel Camera for the Large Synoptic Survey Telescope (LSST) OLIVER, John

Plenary Session 3 - Chaired by Christophe DE LA TAILLE

FPGAs in 2008 and Beyond LINDENSTRUTH, Volker

Plenary Session 4 - Chaired by François VASEY

Optoelectronics, a global telecom carrier's perspective BATTEN, Jeremy

Plenary Session 5 - Commissioning the LHC machine and interlocking with experiments, Chaired by Thijs WIJNANDS

Commissioning the LHC Accelerator and its Physics Programme WIJNANDS, Thijs
3D IC Pixel Electronics, the next challenge YAREMA, Ray

Plenary Session 6 - LHC upgrades: needs and reality, Chaired by Geoff HALL

Overview and Electronics Needs of ATLAS and CMS High Luminosity Upgrades HESSEY, Nigel
CO2 cooling for HEP experiments VERLAAT, Bart

PARALLEL SESSIONS

Parallel sessions A were chaired by DE LA TAILLE, Christophe
FORMENTI, Fabio
GONIDECE, Alain
WIJNANDS, Thijs

Parallel sessions B were chaired by FARTHOUAT, Philippe
PETROLO, Emilio
VASEY, Francois
YAREMA, Ray

TOPICAL SESSIONS

Jorgen CHRISTIANSEN and Geoff HALL chaired the topical groups.
POSTERS

John OLIVER chaired the posters session.

TUTORIALS

Larry G. EDSON gave a tutorial on Designing Printed Circuit Boards Not To Fail.

INDUSTRIAL EXHIBITION

C.A.E.N, Viareggio, Italy.
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NEXT WORKSHOP

The next workshop will take place in Paris, France, on 21–25 September 2009
I. SOME STATISTICS

The Topical Workshop on Electronics for Particle Physics (TWEPP-08) took place in Naxos, Greece, from 15 to 19 September 2008. Thirteen invited and 126 contributed papers (61 oral and 65 poster) were presented in 7 plenary and 11 parallel sessions to an audience of approximately 160 participants. Twenty-one of these participants came from the United States and three from Japan, while the rest originated from Europe. Of all presented papers, 43% referred to the LHC project, 25% to the SLHC upgrade, and 32% to ILC and other experiments.

II. SESSION SUMMARY

Some of the main conclusions from the sessions dedicated to ASICs, Optoelectronics, Power, Installation and Commissioning, LHC Upgrades, Trigger and Posters are summarized in Sections A to G below. Owing to space constraints, many contributions have to be omitted from this summary, but the interested reader can find them all at [1]. Invited presentations during the opening session of the workshop surveyed the High Energy Physics activities in Greece, highlighting a healthy programme covering accelerator-based physics at CERN, DESY, and FERMILAB, as well as other experiments such as Nestor and KM3Net. Two other HEP projects were presented: the European XFEL Photon Source and the Large Synoptic Survey Telescope (LSST). Many additional invited talks introduced the sessions reviewed below.

A. ASICs

The two ASIC sessions hosted 12 talks, 9 of which were dedicated to pixel readout chips, showing the important R&D effort needed to meet the challenges of the next generation of tracking detectors and calorimeters. These chips are intended for the SLHC, the ILC or the Gigatracker at NA62. For all these, the challenges of denser integration, minimizing power dissipation and tolerating increased radiation levels are being tackled through new technologies or innovative design. The three remaining talks addressed Si-Photo-Multiplier readout, high speed serializers, and the radiation hardness of SiGe technology.

Electronics designers have to meet new challenges in order to provide larger systems at a lower cost per channel. Modern microelectronics technology makes it possible to implement in silicon more functions than ever before (analog and digital blocks, often combined together with several programmable features). Several technologies are available to the designers. They evolve so rapidly that it is often a challenge to get the best compromise between the constraints of project planning and the choice of the latest technology. Design engineers have to select their preferred technology on the basis of the performance required at the system level, the available resources, the requested delivery time, and the long term availability of the technology. The range of available library functions best suited to the application must also be taken into account.

An important requirement to any chip operating in the front-end of SLHC systems is radiation hardness. Modern fine-feature technologies appear to offer this hardness almost without any special preventative measure; however, engineers continuously looking for best performance at the highest radiation levels must constantly confirm this fact.

Besides coping with the increase in electronic channel density and the need for radiation hardness, achieving higher speed with reduced power dissipation becomes the next design challenge. Modern microelectronic technologies can contribute to solving this problem, thanks to their lower power supply voltage. Generating and distributing this power was the subject of a dedicated session reviewed in section C below.

Testability is an important issue at the system level, but in the ASIC domain an almost costless solution is possible. With the capability to integrate more functions per surface area, designers have the possibility to implement inside the ASIC several
complementary functions to check its correct behaviour. This does not substantially increase the cost of the final device, while considerably decreasing the costs related to debugging and future on-board verification and maintenance.

The Microelectronic User Group (MUG) meeting which followed the ASICs session of the workshop consisted of a presentation of the design tools and of the foundry access services provided by CERN to the HEP electronics design community, followed by an open discussion among the participants. The presentation gave an overview of the technologies that are currently supported at CERN and focused on the CMOS 130nm technology that presently constitutes the mainstream for the designers in the HEP community. The digital design flow and the technical challenges associated with designs in modern deep submicron technologies were addressed. Complex physical design rules and manufacturability design constraints, signal integrity issues caused by signal cross-couplings and tough final timing closure for digital designs, requirements for systematic multiple corner simulations, requirements for rigorous analysis of voltage drops on power distribution lines and of electro-migration effects, can only be tackled effectively by employing modern ASIC design tools. Industry offers sophisticated CAE tools to master the difficulties of modern technologies and the key element for delivering successful designs is now the definition and implementation of a specific work flow with those tools formalizing a design methodology. Adoption of common design methodologies and training are two key elements assisting the work on large distributed designs among multiple institutes, enhancing team productivity and increasing silicon accuracy. A fully automated digital design methodology, packaged in a digital design kit, is currently being employed in the CMOS 130nm technology and has been used to implement a series of digital designs. The digital design kit has been distributed to seven collaborating institutes and five training courses were organized at CERN, in the last two years. This design kit is expected to be replaced by a new one that will cover a broader spectrum of functionalities incorporating a design methodology for Analog and Mixed Signal designs, the most typical case of ASICs in the HEP community. The design kit will integrate the foundry Physical Design Kit with digital standard cell and IO pad libraries and a configuration management tool will automate the setup of the design environment.

The Multiple Project Wafer (MPW) services organized at CERN were also presented. MPW runs help in keeping low the cost of prototype fabrication and small-volume production by enabling multiple participants to share production overhead costs. CERN has also developed a working relationship with the MPW provider MOSIS as an alternative means to access silicon for prototyping when demand is not high enough to justify a CERN organized MPW. With the current industry prices, a CERN organized MPW becomes more cost efficient than a MOSIS run at around 90 mm² of silicon area.

During the open discussion session, technical issues with the CMOS 130nm design kit were addressed. The issue of building and maintaining a common IP block repository was raised. The repository can be maintained at CERN and could host IP blocks created by the designers of our community. There was a general consensus that this facility is of great importance. To realize this undertaking there must be a consensus among the designers that some effort will have to be invested from their part. The circuits delivered to the repository have to be packaged as IP blocks to facilitate their integration in the design kit, and must be accompanied by a minimal set of specifications and by a simulation test bench when appropriate. Availability of the designers to provide some level of technical support for their circuit is also important for the success of this endeavour.

The organization of more regular MUG meetings was also suggested, to provide effective means of exchanging information in the community and allow designers to become acquainted with ongoing developments.

B. Optoelectronics

The optoelectronics session of the workshop consisted of 5 oral presentations and 7 posters. In addition, 7 short presentations and discussions took place during the opto-working group meeting which followed the session.

Approximately one third of the contributions were dedicated to existing LHC systems, their commissioning and analysis. As already pointed out in 2007, the optical systems installed at LHC are all operational with a dead channel count well below the 1% level. System-level test and setup procedures as well as tools and results were presented by both ATLAS and CMS, confirming that the good system performance observed had been obtained at the cost of a significant effort during installation and commissioning. It was agreed during the opto working group meeting that these lessons will be appended in 2009 to the existing and published “lessons-learned” report.

The remaining two thirds of the contributions were dedicated to future optical systems. Total dose and total fluence tests of PIN diodes, VCSELs and fibres (both single and multi-mode) were reported. Candidate high speed components were identified which seem to resist SLHC radiation levels. These are all very encouraging results, which will be confirmed and reproduced on a larger scale within the opto-working group. Single Event Upsets generated in PIN diodes were also measured at gigabit per second speeds and analysed statistically. Interestingly, not only zero-to-one bit flips, but also
one-to-zero SEU-transitions were observed, as well as multi-bit bursts. In cases where unshielded trans-
impedance amplifiers followed the pin diode, very long bursts of errors were also reported, indicating
that not only the photodiode, but also the succeeding analog electronics will need to be appropriately
designed and qualified to cope with high particle fluxes. In the field of components and systems
characterization, test setups operating up to 10 Gbps were presented. Results were shown, confirming that
the know-how and equipment is now becoming available in our community to develop high speed
links. A figure of merit was described which allowed a quantitative comparison of transmitters
and receivers, paving the way to a broad survey of market components. Finally, a status report of the
joint versatile link project was presented, highlighting the progress made during the first six
months of work.

C. Power

Power supplies and power distribution are key issues for the next generation of experiments. A lot
of work is invested in the subject as shown by the number of presentations and posters in the session.
There were 7 oral presentations in the dedicated power session, plus 6 posters and another 5
presentations during the power working group session. The vast majority of them were related to
future systems.

The main issue for future experiments is to find an efficient way of bringing power inside the
experiment volume where the space is highly limited and where the environmental conditions are
extremely harsh (magnetic field and radiation). Some examples of power levels needed for SLHC
upgraded trackers were given. They show that while the power per electronics channel is expected to
decrease (due to the use of smaller feature size technologies) the total amount of current to be fed to
the detector volume is increasing (higher number of channels and lower operating voltage). As more
current means thicker cables, solutions must be found to reduce this current and maintain the cable
envelope.

Two main routes are being pursued to reduce power supply current: one based on DC-to-DC
converters and one based on a serial powering scheme.

The principle of DC-to-DC converters is to transform a high-voltage low-current input to a low-
voltage high-current output, the input power being equal to the output power divided by the yield of the
converter. This technology is heavily used in commercial equipment but needs some adaptation to
our needs. First of all, in order to be effective this solution requires the converters to be positioned
inside the detector volume and operate in the presence of a strong magnetic field. Most
commercial converters rely on magnetic elements for the energy conversion and these elements will not
work at the field levels present in the detectors. There are two ways of attacking this problem: one is
to use air core inductors and the other is to use capacitors instead of inductors for the energy
transfer. Both options are being looked at and both could be used efficiently. For instance a two-stage
conversion scheme was presented in which an inductor based DC-to-DC convertor provides a
relatively high current and medium voltage (a few amperes at 3 to 5 V) and then a capacitor based DC-
to-DC convertor would be embedded in the front-end chips to deliver the low voltages used by the
analog and digital circuits. The overall power dissipation in the system could be highly optimized
with such a scheme.

Two other problems need to be studied and solved for the DC-to-DC conversion scheme to be
successfully demonstrated. One is the potential noise increase which could come from the switching
currents in the air core inductors and the other is the need for operating power devices in a high radiation
environment. Several noise studies have been pursued using detector elements from ATLAS or
CMS powered with either commercial or custom convertors. This work is very promising. It has led to
the definition of a measurement method and reference setup that everybody can use. The second
problem is the radiation hardness, where the situation is still unclear. Commercial devices were
tested but none of them sustained the required radiation level for the trackers of SLHC. A
technology to be used for developing a full custom ASIC had been identified but recent radiation tests
have also shown some unacceptable limitations.

For the coming year, work will concentrate on
finishing the design of a buck DC-to-DC convertor ASIC, on testing several technologies against
radiation, and on pursuing the study of commercial devices and of noise effects.

The serial powering scheme is also a DC-to-DC
converter but working in a very simple way: N elements needing a current I under a voltage V are
put in series and powered with a voltage N*V and a
current I. Several measurements have been made,
showing that this scheme works and does not
introduce extra noise. It also has the advantage that
the circuitry required does not need a special
technology and hence the radiation hardness is less
of an issue than for the DC-to-DC convertors.
However, at the system levels it presents a number
of challenges. Firstly, in a distribution chain the
devices are all at different potentials leading to
constraints on the connection of the readout
electronics to the detectors and the way the readout
is implemented (AC coupling becomes mandatory,
for instance). Secondly, this scheme can only remain
power-efficient if all the devices to be powered
consume the same amount of current. Thirdly, the
control of the system (switching ON and OFF for
instance) has to be studied with great care (when a device is OFF, the current is still flowing through it). Finally, the separation of power supplies on a device (for instance if one wants to split the analog and the digital supplies of a device) is less efficient power-wise as this can only be done with local linear voltage regulators.

Several successful tests have been done with up to 30 devices serially powered and some custom circuitry is expected to become available soon: a new silicon strip readout chip (ABCn) developed for ATLAS contains the necessary elements for implementing the serial powering scheme and an ASIC designed at Fermilab (SPI, or Serial Powering Interface) provides the shunt regulator and the control logic (including protection circuitry) necessary for serially powering a device.

For the time being, it is too early to choose between these two approaches and the R&D work has to be pursued in parallel. It is important, however, to put in place all the methods allowing coherent testing and an easy comparison of performance between the different solutions. A good fraction of that is already in place (e.g. the noise characterization) and it was agreed during the power working group session to design the readout hybrids for the ATLAS R&D work on strip detectors with the capability of including different power devices.

D. Installation and Commissioning

The successful startup of the LHC on 10 September, just before the beginning of the workshop, was a major milestone for the accelerator and all experiments. The establishment of a circulating beam in the presence of media from all over the world was the result of carefully carried out hardware and sector commissioning and of various successful synchronization tests with beam in the preceding months. Both machine and experiments worked extremely hard to meet the tight schedule as exemplified by several presentations:

- The accelerator cryogenic control system, for example, is partially located in the tunnel and is therefore designed to be radiation tolerant. To keep the magnets in nominal conditions, the distributed cryogenic instrumentation connects to approximately 18 000 sensors and actuators. To commission the tunnel electronic crates, a Mobile Test Bench (MTB) based on a PXI platform was developed. The MTBs are equipped with a Software Configuration Management (SCM) tool that provides a centrally managed storage area.

- For the ATLAS pixel detector, dedicated calibration techniques were developed for each detector assembly stage, matching the demands of the real detector services and readout system. Nearly the entire pixel detector was successfully commissioned in situ which allowed combined cosmic runs with the rest of the tracker (SCT and TRT).

- From 2006 to 2008, the full detector system for the ALICE silicon pixel detector (SPD) was tested in a dedicated area at CERN. At the same time, as much as possible of the read out electronics were commissioned. Together with the use of automatic control procedures, this enabled the successful recording of the first particles generated by injection tests in the LHC in June 2008. The SPD has been operated almost without interruption since that time.

- The CMS high resolution electromagnetic calorimeter (ECAL) on- and off-detector electronics were commissioned within CMS in situ. An important milestone was the startup of the monitoring system that uses the beam abort gap to calibrate the system. During the synchronization tests of the LHC ring, 98% of the crystals lit up when a beam was dumped on a collimator in the tunnel upstream. ECAL is now operating as expected with occasionally some problematic channels.

- The procedure for the hardware installation and commissioning of the ATLAS LAr calorimeter system was to perform a test as soon as possible in standalone mode. If successful, the elements were integrated with the previously commissioned detector and continuously exercised with pedestal runs, calibration runs and cosmic runs to verify its behaviour and stability. The detector now has 100% of the HV channels operational with a very stable readout system (calibration constants stable to better than 0.1% over a few months).

In summary, the installation and commissioning session was the occasion to review the lessons learned so far. After completion of the commissioning of the individual systems, global tests with cosmic rays were successfully performed and concluded with the observation of the first tracks from the beam halo generated by the first circulating beams in the LHC on 10 September. The cosmic runs provided a useful test of the software, of the readout chain and of the detector performance in the global environment and in the presence of cross-talk and noise. They also provided a test of the detector alignment. Various difficulties encountered during the individual and global commissioning were reported and lessons for the future were pointed out. Despite difficulties which, in some cases, caused important delays (cooling problems, noise problems during large scale tests) most of the detector systems have been successfully tested to perform to the expected performance levels. The LHC experiments are now looking forward to the first collisions.

E. LHC Upgrades

The sub-title of this year’s topical session was “needs and reality”, quite vividly illustrated in descriptions of requirements for ATLAS and CMS operation at $10^{35}\text{ cm}^{-2}\text{s}^{-1}$ luminosity. The LHC
machine will be upgraded in two stages, and may reach a luminosity $\sim 3 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$ about five years after the LHC switches on, once collimator and final focus quadrupole improvements have been made. This will already require greater performance from the detectors, surpassing that of the current designs. Beyond the first machine upgrade phase, the picture is less clear but ideas are being explored to find the best way to achieve an order of magnitude increase in luminosity as early as 2018 following a lengthy shutdown during which detector installation could take place. The physics goals depend partly on discoveries in the coming years but it is expected that demands for a ten-fold luminosity increase will be justified in a few years. In this new environment, detector performance will need to be maintained despite pile-up.

Some machine improvements involve higher beam currents, higher reliability or shorter fill time but others require new machine elements or ideas such as magnets inside the experiments for “early separation” of proton beams. This would have a major impact on detector design and likely backgrounds. Others, such as crab cavities, might be easier to adapt to but remain unproven. In most scenarios, luminosity levelling to avoid dramatic differences in event rates is considered desirable for best operation, including easing the design of trigger and readout systems.

Detector plans for Phase I are reasonably clear: incremental improvement to DAQ systems and a 6–8 month shutdown to replace the radiation damaged innermost tracking detectors. In CMS the pixel detector can be replaced quickly, while ATLAS requires at least one year to replace the innermost B-layer. Therefore, plans to insert a new B-layer inside the current detector, along with a smaller diameter beam pipe, are being considered. In the longer term, improved triggers at Level-1 with new contributions from tracking detectors, or topological triggers combining different sub-detectors, are expected.

A vital aspect of future tracking detectors is cooling, especially given expected power challenges. It is envisaged that more heat must be removed than at present, however carefully future electronics are designed. Requirements for silicon detectors are clear: many distributed heat sources in large volumes, low temperature gradients between them, and constant cooling avoiding thermal runaway of irradiated silicon. Cooling pipes must have low mass and a low structural impact, and the fluid should be radiation resistant. The use of evaporative carbon dioxide cooling, as used in a pioneering development for the LHCb Vertex detector, has attracted a lot of attention as a promising candidate for future cooling.

Minimizing front-end electronic power consumption is vital to all tracker upgrades. New IC technologies offer significant power savings per channel but the number of channels is expected to increase significantly and digital, rather than analog, power consumption may become dominant so techniques to minimize it must be exploited. Power savings can also be achieved by adopting low current differential signalling schemes to replace present standards. Prototypes developed for a possible upgrade of the CMS pixel detector have demonstrated less than 10 pJ per bit per link at 160 Mbit/s over a 2 m long low mass unshielded twisted pair cable.

The ATLAS Pixel Detector upgrade envisages a larger system with more layers. New front-end chips must be developed, with a new module, readout architecture and powering scheme, aiming to reduce the material budget. New optical links with higher transmission speed are required, and a new detector control system is also needed.

The architecture of the readout electronics for the upgraded ATLAS tracker is a change from the current design. The detector is organized in staves with a hierarchical readout with fewer but higher speed links. Some components are not required in very high quantities which may encourage common solutions. Preliminary studies of a front-end preamplifier-shaper-discriminator in 130nm CMOS show a power dissipation below 200 µW per channel while its distribution requires special efforts; savings of factors 5–10 in total current compared to the present system are thought possible.

Progress towards a new CMS microstrip tracker readout for SLHC includes evaluating advantages and disadvantages of different architectures, including trade-offs between power, FE chip and system complexity, system robustness, and performance. A three year development programme is about to start, to deliver a full chip prototype in the second year. Several system level decisions are still open, such as sensor choices, powering scheme and choice between analog and binary, sparsified or not. There are significant advantages in using a binary, non-sparsified design for short strip readout, which results in a simpler chip and system. However, triggering remains the most challenging aspect of the CMS tracker for SLHC, and ideas are still developing which require more simulation results.

Upgrade plans are not restricted solely to the trackers. A possible upgrade of the ATLAS Monitored Drift Tube Detector was presented, allowing it to cope with SLHC background rates. There are several options: to use small tubes, or tubes with field shaping, or other gaseous detectors, such as MicroMegas. For the hottest regions of the detector, 150–180 MDTs will have to be rebuilt covering 600–700 m². Either an increased global readout bandwidth by factor 5–10 must be used, or selective readout based on trigger chamber information. For less hot regions, FE electronics should also be redone, ideally using radiation tolerant FPGAs. Everywhere, ageing behaviour must be evaluated and improvements in the radiation tolerance of power supplies achieved.
Peter Sharp described in his invited talk some lessons learnt during the development, production and commissioning of the LHC detectors and their electronics. He summarized his experience and recommendations to the HEP community on microelectronics, optoelectronics, power supplies and off-detector electronics, all of which raised many important issues for future system development. It is widely acknowledged today that effective use of microelectronics is vital for high performance particle physics detectors. In the early days of the LHC, microelectronics was still emerging and significant investments in skilled manpower and tools were needed to take advantage of modern CMOS technologies. This was accomplished taking advantage of support for microelectronics teaching in universities via EU-funded projects, allowing affordable tools and access to technology.

Appropriately skilled personnel are vital, becoming even more so as technologies advance, and rely on increasingly complex CAE tools. To work in the very hostile radiation environments of the LHC with minimal power consumption requires additional expertise to be developed and maintained. Partnerships with foundries have been found important. For development of systems for SLHC, design groups with sufficient critical mass to master new technologies and tools will be critical. The increased complexity and cost of ASIC developments will surely imply that effort must be concentrated on a limited number of different front-end chips to be produced in large quantities.

Optical link technology is also now vital and the development of radiation hard links has required a large qualification effort, where many details contribute to ensure highly reliable systems. Links with very different characteristics have turned out to have very similar production and development costs, in contrast to some expectations.

Power supplies for LHC front-end systems provide an example where it would have been advantageous to include them earlier in system designs. Supplying clean power and implementing grounding and shielding is non-trivial. Constructing systems to supply power over significant distances and tolerating radiation and magnetic field in experimental caverns required non-standard industrial products.

Off detector, many LHC systems profited from the performance and flexibility of FPGAs but in some cases choices were fixed before FPGAs were widespread. Clearly, technology decisions should not be made too early to profit from commercial electronic progress. Extensive use of FPGAs has delivered benefits but also introduced problems of managing large amounts of complex firmware that must be maintained, supported, and probably upgraded over time.

In future, the community must find (more) efficient ways to produce systems with hundreds of thousands of chips, tens of thousands of modules and optical links, thousands of power supplies and large, complicated readout and DAQ modules. Engineering and quality assurance of such large systems will require a disciplined and professional approach and may require changes to the way HEP collaborations operate. The expertise to build and run such systems must be distributed so that large projects do not become over-dependent on a few key individuals. It is vital to maintain a critical mass of experienced engineers, with appropriate facilities, to conserve experience from current systems.

The discussion session which followed the presentations had a lively debate on the question of appropriate time schedules. It is clearly acknowledged that such large and complex systems require significant time for their development, production, qualification, integration and commissioning. For Phase 1 upgrades there is practically no time to do basic R&D. In important cases it is necessary to start development of Phase 2 SLHC upgrades systems soon to be capable of having working systems available in ~10 years. This may leave very little time for generic R&D programmes based on new technologies that potentially offer major advantages to new detectors.

Spending too much time on generic R&D generates a risk of not having systems ready in time. To take advantage of new technologies it will be important to find ways of shortening the time needed for production, integration and commissioning. This is clearly a major challenge for large collaborations and expected to be a major subject for discussion over the next few years.

F. Trigger

The Trigger session presentations were largely focused on the commissioning and first operation phase of the trigger systems used as part of the regular data taking: recording cosmic muons for long periods and comparing rates with Monte Carlo expectations and measured flux in the cavern. Whilst waiting for first collisions, the focus has been mainly on the development of timing and energy calibration procedures.

During the commissioning phase, misconnections of cables and bad modules were fixed and extensive tests of signal integrity and stability were performed. The challenging requirements at the board and system level could then be verified. The accumulated experience will allow for a better control of the systems in terms of stability and trigger rates, and to fulfil their main role of providing a reliable trigger decision to the experiments.

The work of the present and past year was also largely dedicated to the development of software
tools essential to system operation and monitoring. On the hardware front, the extensive use of FPGAs made it possible to adapt board behaviour to system performance by just changing and upgrading the firmware.

Most recently, the systems have been successfully used with LHC related particles during the very first tests, in injection and dump mode and with single beam radio-frequency capture, collecting events reconstructed in the detectors.

Studies on SLHC trigger systems are ongoing. Much work still needs to be done in the definition of trigger requirements and in identifying the appropriate technology for system implementation.

G. Posters

The poster session contained some sixty-five contributions covering a broad range of topics including ASICs, Trigger, Power Conversion, Optoelectronics and Experiment Commissioning. Just over half of these covered developments for LHC experiments, with the others representing a broad range of interesting applications. Overall, the depth and quality of the poster presentations was impressive. The session enabled in-depth one-on-one discussions in a way which is generally not possible in oral sessions. It was very well attended and generated lively discussion between the attendees and poster presenters. Just over half of the posters were presented outdoors where the balmy Aegean breezes enhanced the experience.

III. CONCLUSION

The TWEPP-08 workshop was characterized by a very open and positive atmosphere. It provided the right framework for discussing old and new projects, reviewing developments, encouraging robust engineering and quality assurance practices, and discussing access to technologies and tools. The oral and poster sessions, together with the parallel working group meetings proved to be the right forums to ensure that critical mass is maintained in our community and that lessons learned are passed on from generation to generation.

Finally, the local organizing committee must be praised for turning this workshop into such a pleasant event [2] in a truly exceptional location.

IV. LINKS

## Programme Overview

### TWEPP–08 Topical Workshop on Electronics for Particle Physics

**15–19 September 2008**

**Naxos - GREECE**

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Monday 15 September 2008

Plenary Session 1
An overview of the Experimental High Energy Activities in Greece

Chara Petridou, Aristotle University of Thessaloniki, Greece
chariclia.petridou@cern.ch

The Activities

Greek Experimental HEP Activities

Accelerator Experiments
- PhD's: 44
- PhD-students: 30

Non-Accelerator Experiments
- PhD's: 12
- PhD-students: 4

Detector/Accelerator R&D
- PhD's: 3
- PhD-students: 2

Accelerator Physics Experiments

LHC Experiments
- ATLAS
  - PhD's: 18
  - PhD-students: 10
- CMS
  - PhD's: 17
  - PhD-students: 10
- ALICE
  - PhD's: 3
  - PhD-students: 5

nTOF

Accelerator Physics Activities

Fermilab Experiments
- Tevatron-CDF
  - PhD's: 1
  - PhD-students: 2

Neutrino Physics
- PhD's: 1
  - PhD-students: 1

DESY Experiments
- HERA-H1/ZEUS
  - PhD's: 3
  - PhD-students: 1

Non-Accelerator Physics Experiments

Experiments in Greece
- NESTOR
  - PhD's: 4
  - PhD-students: 2
- HELYCON
  - PhD's: 3
  - PhD-students: 2

Experiments at CERN
- CAST
  - PhD's: 4
  - PhD-students: 2

The Greek ATLAS Project

NKUA, NTUA, AUTH all three institutes collaborated for the construction of the BIS chambers of the ATLAS Muon Spectrometer, consisting of 128 MTD Muon chambers.

All chambers installed in the ATLAS pit since Dec 2006

All chambers commissioned with cosmic rays Ready for data taking

C. Kourkoumelis This Conference
The Greek ATLAS Project

- Muon studies:
  - DCS and HV/LV, Bfield control for MTD’s, Muon Data Quality Assessment software, Cosmic ray runs for the detector commissioning, Muon energy loss in calorimeters, Muon reconstruction performance
  - Physics studies and interests:
    - Higgs (SM H–>4l, H/ A–>2μ)
    - Exotics (Z’–>μμ, W’–>μν, Heavy quarkonia, Lepto-Quark)
    - SM diboson production, search for anomalous couplings

CMS in Greece

- 2008: 17 PhD physicists
  - Participations:
    - CMS Preshower (DEMONKRITOS–UoI)
    - Development:
      - sensors (Si-strip-hybrids)
      - FE: development & test (UoI)
      - Off-detector electronics (UoI)
      - Preshower DAQ (UoI)
      - Assembly & test
      - 1000 modules (DEMONKRITOS)
    - Simulation-calibration
    - DQM (UoI)
    - Beam tests

ALICE in Greece

- Trigger/DAQ (mainly DEMOKRITOS)
  - Development (GTPe)
  - Construction (IOP, GTPe)
  - Evaluation
  - CASTOR (UoA)
    - Project management
    - Development/Simulations
    - Construction
    - Beam tests
  - Physics analysis
    - CMS physics coordination (UoA)
    - Physics analysis of ECal-Preshower test beam data (DEMONKRITOS, UoA)
    - Physics analysis of the CMS/Physics/TPC (DEMONKRITOS, USA)
    - Development of IP injection algorithms & electron efficiency (DEMONKRITOS)
    - Si-Microstrip x解说 x MET channel (UoA)
    - RISER and Mini Trig. search (DEMONKRITOS)
    - W and Z–ejection in the electron channel Zγ (UoA) and TGC (DEMONKRITOS)
  - Future plans: Data Analysis, SLHC

ALICE in Greece

- CASTOR: quartz / tungsten Cherenkov EM/HAD calorimeter, at the very forward rapidity region for forward QCD studies and unexplored cosmic ray phenomena.
- Half of the CASTOR is installed in the CMS line for the LHC start up.
- CASTOR: quartz / tungsten Cherenkov EM/HAD calorimeter, at the very forward rapidity region for forward QCD studies and unexplored cosmic ray phenomena.
- Half of the CASTOR is installed in the CMS line for the LHC start up.

Hardware/Software Contributions of the NKUoA to ALICE

- Design, development and construction of the H.V. Distribution System (HVDS) for the TRD detector.
- Design and development of a monitoring system (Gate Pulser I) for the ALICE TPC.
- Development of the DAQ monitoring system for the Forward detectors of ALICE–used by all ALICE detectors.
- Compact Software upgrade for online monitoring (MODD)
- Software development for Data Flow Control for all ALICE detectors (AMORE)

Hardware Contributions of the NKUoA to ALICE

- A Master/Slave power supply distribution system has been designed and constructed in order to provide the required anode (1.9kV) and drift voltage (-2.5kV) to the ALICE TRD readout chambers.
- The system can switch on and off, monitor (at the mV level), protect, and regulate (current control) each channel from a common ground voltage.
Hardware Contributions of the NKUoA to ALICE

**HVDS Specifications**

- **Both Systems:**
  - Output Channels: 180
  - Ramp-up rate: 1-30 V/s
  - Ramp-down rate: 1-100 V/s
  - HV stability: <0.1% /24h
  - Achieved HV stability: ~0.002%/24h
  - Ripple rejection: ~40 dB
  - Current accuracy: <0.2%
  - Achieved Current accuracy: ~0.03%
  - Response time: < 50 ms

- **Anode System:**
  - Dynamical range: 900 - 1900 V
  - Max. current: 7 μA

- **Drift System:**
  - Dynamical range: 1450 - 2500 V
  - Max. current: 270 μA

Contributions to the ALICE Physics Performance Reports (I + II)

Contributions to Physics Analysis Software of the NKUoA in ALICE

- Physics preparation Studies with Monte Carlo simulations:
  - Topological K/π identification,
  - <Pt> studies,
  - K/π ratio,
  - Charge fluctuations,
  - Wavelets method,
  - Balance Function,
  - Hadronic Resonances etc.

Contributions to Physics Analysis Software of the NKUoA to ALICE

- **K/π separation from their decays in the TRD detector**

Contributions to Physics Analysis Software of the NKUoA to ALICE

n_TOF – Phase 2

2008 and beyond

Capture measurements

- Mo, Ru, Os stable isotopes
- repent, resonances calculation
- isotope patterns in S.C. glasses

- F, Ne, Zn, and Se (stable isotopes)
- s-process nucleosynthesis in massive stars
- Intermolecular nuclear yields for structural materials

- A-170 (isotopes used)
- s-process branching points
- long-lived fusion products

- 238U, 239Pu, 241Am, 242Cm
- Th/U nuclear fuel cycle
- standards, conventional U/Pu fuel cycle
- incineration of minor actinides

Greek Contribution to nTOF

- Aristotle University of Thessaloniki
- NTUA
- University of Ioannina
- NRCS Demokritos

- Measurements relevant to fundamental physics,
  - Nuclear Astrophysics,
  - Nuclear fuel cycles and incineration of nuclear waste

Accelerator Experiments: FermiLab

- Tevatron-CDF

- Participation: University of Athens
  - Activity:
    - Top mass measurement
    - Use Pt, lepton to estimate mass
    - W > eν cross-section measurement
    - Use forward electrons
Greece in CDF

- Lepton $p_T$ spectrum sensitive to the top mass
  - Use maximum likelihood method to fit data with signal + SM background for different top mass values
- Method can be applied to LHC data

V. Giakoumakopoulou PhD Thesis

Greece in CDF

- Forward electron $p_T$ spectrum
  - Measured cross-section
  - Compared to cross-section from central region
  - Theoretical prediction: $2720 \pm 130$ pb

A. Staveris PhD Thesis

University of Athens Neutrino Group (NKUoA)

Activities:

- DONUT Experiment (Completed)
- MINOS Experiment: Far Detector PMT Testing and Characterization; Near Detector Commissioning; CC Data Analysis.
- MINERvA Experiment (In construction); PMT Testing and Characterization; Design of the Test stand; Software development.
- NOvA Experiment (In construction)
- Construction of a PET prototype

N. Saoulidou: DONUT (PhD), MINOS
C. Andreopoulos: DONUT, MINOS (PhD)

Beam: NuMI beam, 120 GeV Protons $\rightarrow$ $\nu_{\mu}$ (High Intensity)

Detectors:

- ND, FD
- Near Det: 980 ton version of FD, at FNAL ($L = 1$ km): Measure beam composition and energy spectrum
- Far Det: 5.4 kton magnetized Fe/Sci Tracker/Calorimeter at Soudan, MN ($L = 735$ km): Search for evidence of oscillations

Best Fit: $|\Delta m^2| = 2.43 \times 10^{-3}$ eV$^2$ $\sin^2(2\theta) = 1.00$

World’s Best $\Delta m^2$ measurement

The MINOS Experiment

FAR MINOS DETECTOR

- 5.4 kton Magnetized Scintillator Calorimeter/Muon Spectrometer
- Structure: Steel / Scintillator
  - 2.5 cm thick steel
  - 4 cm x 1 cm polystyrene strips in Al cover
  - WLS fiber
  - 8m x 8m Octagonal Planes
  - 8 modules/plane, 192 strips/plane
  - 15.2 k A-turn coil
  - Cosmic Ray Shield
  - Total: 486 Layers

NEAR MINOS DETECTOR

- Electronics: Viking chip (VA) based
- Structure:
  - Veto section
  - Target section
  - Shower detector
  - Muon spectrometer
- 282 steel planes
- 153 scint. Planes
- 1 kT, 3.8 m x 4.8 m "squeezed" octagon
- Electronics: QIE chip based

MINOS Detector Technology

- Scintillator Module
- WLS Fibers
- PDEs (2-6 m)
- Clear Fiber Ribbon C
- Multiplex Box
- PMTs
- Connection to electronics

Electronics: QIE chip based

Objects not to scale
NKUoA in MINOS

constructed an automated test station for Hamamatsu M16
• performs a wide range of precise measurements
• tests 10 PMTs simultaneously
• fully automatic
• runs a sequence of data-taking modes
• without human intervention for ~3 days
• at 500 Hz DAQ rate Þ ~ 2 GBs/batch (not raw data)

WHAT TO TEST
• Gain determination (dependence on HV)
• Correlation Nontrivial HV (Gain = 1±0.5)
• Dark count spectra and dark count rate
• Verify good SPE separation
• Cross-talk
• Uniformity
• Linearity
• Using term stability

Total number of tested PMTs for MINOS FAR DETECTOR: 750

Greece in HERA/H1

LQ Exclusion Limits – Comparison with LEP & Tevatron
HERA extends the exclusion region
I. Panagoulias DIS2008 – work on PhD / NTUA & H1/HERA

The Nestor Project in Greece

The Nestor Project in Greece

The Nestor Project in Greece

S. Anasontzis This Conference

HELYCON
Hellenic Lyceum Cosmic Observatories Network

HELYCON: Detector Construction

• Obtain direction of showers from time differences between stations
• Correlations between showers
• Flux of showers
• Synchronization between stations achieved through GPS
**HELYCON: Testing and Shower Reconstruction**

**HELYCON: Detector Deployment**

**CAST in Greece**

**Micromegas for SLHC**

- ** PARTICIPATING INSTITUTES:**
  - University of Patras
  - NRCPS Democritos
  - Aristotle University of Thessaloniki
  - National Technical University of Athens

- **MAJOR CONTRIBUTIONS TO THE EXPERIMENT:**
  - Strong Greek involvement in the proposal and the creation of the Collaboration
  - Contribution to development, construction and installation of Micromegas detectors
  - Monte Carlo simulations and data Analysis
  - Software development for the He-3 system controls

A project to investigate the feasibility and determine the working parameters of Micromegas for SLHC tracking

*In conjunction with the ATLAS SLHC Micromegas chambers effort*

**Participating Institutions**

- *Saclay*
- *Demokritos*
- *Univ. of Athens*
- *Univ. of Thessaloniki*
- *Technical Univ. of Athens*
The Telescope

Detector parameters:
- Design and construct 6 ($X$,$Y$) detectors to form a beam telescope
- Design and construct several test detectors with different pitches (0.5, 1 and 2 mm), some with resistive layers
- Use GASSIPLEX electronics and later a faster front-end system
- Design Labview DAQ and later a faster system

Measurements:
- Assessment of protection against sparks
- Improvement of spatial resolution
- Gas mixture studies

The Test beam prototype

The Test beam prototype

Status

X and Y Micromegas chamber design finished
2 prototypes constructed
8 more chambers under construction
Labview DAQ and Monitoring under development
Planning for initial tests in October 08

LHC Grid Computing

The WLCG Project in Greece

Six Grid clusters of the Hellas Grid are currently running in Greece
Approximate 1000 64-bit CPU units and 100 TBytes online storage, connected over an end-to-end Gigabit backbone
The HellasGrid infrastructure is fully integrated within the pan-European Grid infrastructure EGEE
No MoU yet signed with the WLCG
The Greek contribution to the ATLAS Muon Spectrometer and the physics studies

Christine Kourkoumelis

University of Athens, Physics Dept, Panepistimioupoli, Ilissia 15771, Greece

Christine.Kourkoumelis@cern.ch

Abstract

The ATLAS Muon Spectrometer is an essential part of the ATLAS Detector at the LHC. It is used both for triggering and for momentum measurements of the muons. The Greek contribution to the construction and commissioning of the Muon Spectrometer is reviewed. In addition, the physics studies, leading to lepton final states, performed by the Greek groups are summarized.

I. INTRODUCTION

The ATLAS Detector [1] is a large (length 55m, width 32m, height 35m) general purpose detector, installed at the Point-1 of the Large Hadron Collider (LHC) at CERN and waiting for particle collisions.

The outermost part of the ATLAS detector, the Muon Spectrometer (MS), is designed to perform efficient and accurate stand-alone muon identification and momentum measurement inside the toroidal field created by powerful toroid magnets. In addition, the MS performs the triggering of the muons. For these purposes the MS consists of muon chambers of four different types/technologies: Monitored Drift Tubes (MDT’s) and Cathode Strip Chambers (CSC’s) for precision tracking and Resistive Plate Chambers (RPC’s) plus Thin Gap Chambers TGC’s) for triggering.

The momentum measurement should have a resolution of ~10% at p_T= 1 TeV/c. For optimum resolution over all the momentum range, the MS and the Inner Detector (ID) measurements should be combined. As shown in figure 1, in the low energy regime the accuracy of the ID dominates the muon momentum estimation, while at higher momenta the MS resolution dominates. The crossover point spans from p_T = 80 GeV/c in the barrel to p_T = 20 GeV/c in the forward region.

In order to achieve the momentum resolution goals stated above, the sagitta of the high momentum muon tracks (~1TeV/c) should be measured with an accuracy of 50 μm, which means that the Precision Muon chamber alignment and position should be determined with a comparable accuracy. Sophisticated alignment systems for both the Barrel and the End-Caps have been built for this purpose [3]. Besides the placement and the continuous monitoring, the construction of the chambers had to meet very tight precision specifications.

Three Greek Universities have undertaken the task of building about 10% of the MDT’s within the very strict construction specifications [4]. These chambers were the BIS (Barrel Inner Small) 112 chambers (figure 2), consisting of 29000 drift tubes of ~1.7 m length and arranged in eight layers of tubes (figure 3).
The construction task of the BIS was divided into three different complimentary subtasks:

The University of Athens (UoA) was responsible for the MDT tube assembly; the National Technical University of Athens (NTUA) was responsible for the Quality Assurance/Quality Control of MDT tubes and the Aristotle University of Thessaloniki (AUTH) was responsible for the MDT chamber assembly and test.

II. CONSTRUCTION OF THE BIS CHAMBERS

The construction of the BIS spectrometer started with the wiring the first tubes in the UoA in 1998 (module 0). Subsequently all Greek sites passed the Site Review in May 1999 and started the series production in September 1999.

The wiring of the tubes in the UoA was performed in a clear room of constant temperature as shown in figure 4 and involved a number of precision steps in order to meet the tight construction specifications.

A few tests were performed “in situ”, while the main QC/QA was performed in the NTUA facilities. The wiring of 30,000 tubes took four years and was finished in November 2003 (see figure 5).

From 1999 up to April 2004 continuous QA/QC of wired tubes was performed at NTUA. Figure 6 shows some of the test facilities in NTUA.

The following tests were performed:

- Gas leak rate measurement
- Wire position measurement
- Wire tension check
Figure 7 shows the measurements of all wire positions. Note that the scales are in μm.

![Figure 7: The anode wire position measurements for the z and y coordinates for the two ends of each tube (zA, yA, and zB, yB).](image)

After all detailed tests, it turned out that the failure/rejection rate of wired tubes was extremely small, under 1% (Table 1).

### Table 1: Statistics on the 29,000 wired tubes (the rest of the 1,000 wired tubes were used for assembling the initial two test modules plus spares.)

<table>
<thead>
<tr>
<th>Category</th>
<th>Number of tubes</th>
<th>Percentage (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total</td>
<td>28700</td>
<td>100.00</td>
</tr>
<tr>
<td>Good</td>
<td>28455</td>
<td>99.15</td>
</tr>
<tr>
<td>Crimping</td>
<td>25</td>
<td>0.08</td>
</tr>
<tr>
<td>Broken wire</td>
<td>11</td>
<td>0.04</td>
</tr>
<tr>
<td>Finished length</td>
<td>10</td>
<td>0.04</td>
</tr>
<tr>
<td>Leak current</td>
<td>13</td>
<td>0.04</td>
</tr>
<tr>
<td>Gas leak</td>
<td>108</td>
<td>0.38</td>
</tr>
<tr>
<td>Wire location</td>
<td>20</td>
<td>0.07</td>
</tr>
<tr>
<td>Wire tension</td>
<td>58</td>
<td>0.20</td>
</tr>
</tbody>
</table>

The tested tubes were then shipped to Thessaloniki and assembled into chambers on a granite table in a clean room of class 50000, temperature control to ±0.5°C and humidity to ±5% (figure 8).

![Figure 8: The chamber assembly laboratory in the AUTH.](image)

The chamber assembly at AUTH lasted about four years (end 1999-May 2004). At the end of it, the chambers were shipped to CERN to get equipped with services (figure 9).

In parallel with the assembly, a random sample of chambers including the initial ones, were sent to CERN and tested with the X-Ray Tomography at CERN [5]. All the chambers met the ATLAS specifications, except the very first chamber (module 0).

### III. SERVICES AND COMMISSIONING

From February 2004 to January 2006, the chambers were equipped with services at CERN (figure 10, 11). Services included: the Faraday cages, gas manifolds, FE electronics, HV cards, cables for read-out, HV and DCS. The on chamber DCS services included B field probes, temperature probes, and survey platforms. The necessary accuracy of the chamber position during construction and after installation in the pit is given by an extensive system of optical alignment sensors called RASNIK whose sensors were installed on various precision platforms on the chambers.

![Figure 9: Fully equipped chambers at CERN waiting for installation in the ATLAS pit.](image)
During the period January 2005 to January 2006 the chambers underwent extensive testing prior to installation in the pit. The tests included checks for gas leaks for the fully assembled chambers, noise tests and cosmic rays at CERN. In June 2006 up to December 2006 all the BIS chambers (112+16) were installed successfully underground in ATLAS pit (figure 12), after extensive testing on the surface.

Figure 12: One of the Greek BIS chambers under installation in the ATLAS experiment

In general out of all muon chambers installed in the ATLAS pit, there were very few bad channels (broken wires), few chambers with problems (gas leak, overpressure accident,...) BUT no holes in the acceptance. A long commission period “in situ” followed the installation and integration of the chambers in the pit. Main part of the commissioning were the so called “Milestone weeks” (December 06) to M8 (July 08), where cosmic rays have been taken with the muon chambers combined with the other integrated systems (figure 13). Special attention was given to the calibration systems, the detector response, its timing, and alignment.

Figure 13: A cosmic ray detected in the ATLAS pit by the Muon chambers and part of the Inner Detector.

After the installation of the BIS chambers in the pit all Greek groups were naturally heavily involved in the commissioning of the MDT’s. In addition, the UoA and NTUA groups were in involved in the commissioning of the CSC’s., and the NTUA has been and is still playing a major role in the DCS and HV/LV system and magnet field control for MDT’s. The AUTh, on the other hand, is developing the Muon Data Quality Assessment software. Finally, all groups participate in the development and data taking/analysis of microMegas prototypes for the SuperLHC.

IV. PHYSICS STUDIES

ATLAS since more than a year has started the so called CSC (Computing System Commissioning) exercise which is now finished and the new physics potential “book” [6] will appear soon. The main purpose of the exercise was to have all groups train for data and learn to work in common analysis. The Greek groups were heavily involved from the beginning in a wide range of topics from SM Higgs searches to exotics channels, involving mainly lepton decays. In addition the groups collaborated in specific studies of detector performance mainly for muons.

The UoA has participated in studies for the SM Higgs→4l and the MSSM H/A→2μ. As an example figure 14 shows the invariant mass of a SM Higgs with m_H=150 Gev/c^2 together with the expected background. In addition, the group participated in studies for the estimation of the discovery potential for new heavy vector bosons Z’→μμ and W’→μν.

The group was also very active in studies for the muon energy loss in the calorimeters [7] and the muon reconstruction performance.

The NTUA group is involved in heavy quarkonia searches (figure 15 shows the mass of a χ_b decaying to two J/ψ’s), leptono-quark searches and quark compositeness studies.
V. CONCLUSIONS

The Greek Muon construction project was very successful (<1% failure rate) and timely accomplished, thanks to a fruitful collaboration of all three involved institutes.

We all hope that the data will be soon in hand. We have to work hard towards understanding the data, calibrating the detector and the mass scale. Afterwards, the rich ATLAS detector physics potential can be exploited during the initial physics runs, even for integrated luminosities as low as 1 fb⁻¹.

REFERENCES

CMS in Greece (CMS Preshower-Trigger/DAQ-Castor, Physics)

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nmanthos@cc.uoi.gr

CMS in Greece
(CMS Preshower-Trigger/DAQ-Castor, Physics)

CMS geometry and collaboration - GR financial contribution

ATLAS
CMS

CMS Collaboration
32 Countries, 185 laboratories, 3600 scientists and engineers (including

CASTOR: Centauro
And ST range
Object Research, 5.2 < η < 5.6 , 14.37 m from the interaction point

CMS Preshower geometry

Preshower (20cm)

CMS Trigger/DAQ System (TriDAS)

CMS triDAS

Level 1 Trigger:
Muon and ECAL data, latency 3.6 μs
High Level Triggers (on line filter farm): 100 Hz, 10^6 S65 CPUs - 1500 dual quad-core PCs @2.6 GHz (2009, now 50%)

CMS Preshower

Preshower electronics

μodule construction

It will be inserted in CMS during the LHC winter shutdown.

"ESIAB" has been inserted in CMS mainly to facilitate integration in to the full CMS DAQ, on line monitoring and control systems.
CASTOR: quartz / tungsten Cherenkov EM/HAD calorimeter, placed at the very forward rapidity region of the CMS experiment. It is azimuthally divided into 16 semi-octants and longitudinally into 14 sections, with full length of 10 λ.

CASTOR detector will investigate physics topics both in pp and HI collisions at the LHC:
- Forward QCD studies (effective, low-x, ...)
- Especially designed to study totally unexplored cosmic ray phenomena.
- (Centauros, Strangelets, disoriented chiral condensates-DCC's, ...)

Half of the CASTOR is installed in the CMS line for the LHC start-up run.

Participation of GREEK TEAMS in CMS

University of ATHENS:
- NCSR 'Demokritos', Institute of Nuclear Physics.
- University of Ioannina, HEP Lab.

Official GB CMS financial contribution (CMS M&O U)

- Trigger/Daq: 7.2% (2060kCHF)
- ECAL (Preshower): 1.1% (1360kCHF)
- CASTOR: 2.1% (500kCHF)
- CMS and University of Athens - Publications

5. A. D. Panagiotou, P. Katsas. "Search for Strange Quark Matter with the CMS/CASTOR detector at the LHC".

University of ATHENS - Publications

- Participation in SUSY Analysis.
- Participation in CMS Physics reconstruction and selection.
- Participation in SUSY searches.
- CASTOR Project management.
- Participation in the LCG (LHC Computer GRID).
- CMS Management (Physics coordination).
- Participation in SUSY searches.

Participation of GREEK TEAMS in CMS

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- CMS and University of Athens - Publications

The firmware of the 400kGates FPGA based on mixed VHDL and Handel-C.

2. P. Adzic et al., Energy resolution of the barrel of the CMS electromagnetic calorimeter, JINST 2:P04004, 2007


The Global Trigger Processor Emulator (GTPe) : 5 GTPes

The contribution of the three Greek teams in the construction phase of CMS has been substantial, especially in electronics, instrumentation and in physics.

Publication


Summary and conclusions

We look forward to a similarly substantial contribution also in the operation phase of CMS and in particular in data analysis.

Participation in

Participation in the development of the off-line data for electronics, mainly in the firmware of the digital data filter.

Participation in the development of the Preshower control and DAQ software(XDAQ).

Participation in the development of the Preshower micro-modules (~1000), the PACE3 hybrids (~2000), the PACE3 FE chips (~7000), the Preshower micromodules (~1000), the Preshower token ring kaptons (~400).

Participation in the development of the Preshower Data Quality Monitoring (DQM) system.

Participation in the Preshower simulations and Preshower calibration.

Participation in the preparation of the Preshower Beam test and test-beam data analysis.

Future participation in SLHC.

Notes etc.

11 notes and Internal notes, 8 conference talks.

PhD Theses : 3 completed , 1 in progress
NESTOR Participation to the KM3NeT

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Abstract

The NESTOR Collaboration is a leading participant in the Design Study of the KM3NeT, the European Deep Sea Neutrino Telescope. In this report we describe briefly the KM3NeT and the NESTOR experience and contribution towards this objective; the 4500m deep NESTOR site, the star-like detector, the deployment and recovery of telescope modules and the "DELTA-BERENIKE", the specially constructed deployment ship.

I. INTRODUCTION

In the dawn of science, Man looked up the black night sky of the Fertile Crescent, to the stars and made the first scientific observation. He was looking into the Cosmos using the first optical detector, his eyes, detecting what thousands years later called by the physicists, the photon. And up to now, our knowledge of the Universe is based on the photon, this singular information messenger from the depth of Time and Space. From this vast collection of information, astronomy and astrophysics have evolved to the present date knowledge.

Photons or $\gamma$ (gamma rays) can be produced in hadronic and electromagnetic processes, they are electromagnetic radiation and are recognised as visible photons, UV, IR, long wavelength, short wavelength, x-rays and gamma rays, photons, all travelling in straight lines, thus astronomy, i.e. pointing to a particular source, is possible. Each photon differ in their wavelength, thus, the photons of those fields, require different detectors and the evolution of those detectors has followed the advance of the scientific knowledge and technology.

Photons though have a drawback; they are absorbed by the interstellar matter and they interact with UV and infrared ambient starlight and with the 3K photon background, relic of the Bing Bang. Scientists have looked for others messengers, hadrons and charged leptons, to be used in order to probe deeper into the physical processes of the stars. But particles, travelling through space, are attenuated by the interstellar matter AND, if they are charged, are bent by the magnetic fields thus pointing to a source is not possible.

About fifty years ago the neutrino was discovered. Neutrinos are a unique tracer of energetic hadron acceleration in astrophysical sources and can only be produced from hadronic interactions. They have tiny mass and are neutral, so they interact extremely feebly with matter (energy) and they can travel exceptionally long distances before interacting; those attributes make the neutrino a unique messenger of the mighty powers that rule the Universe. But those attributes make also the neutrino extremely hard to detect.

Their interaction probability is energy dependant. For neutrinos with energy up to a few TeV, the Earth is transparent (to neutrinos) but for energies more than a hundred TeV, Earth is opaque [2]. For energies roughly ranging between 1 TeV to 1 PeV, neutrino may pass through Earth and interact just before they emerge; those are the best candidates for detection.

Neutrinos are detected tracing their interactions’ products (electrons, muons and taus) in a transparent medium using Cherenkov radiation.

II. THE NEUTRINO HISTORY

In 1920s physicists were puzzled with the $\beta$-decay (beta decay); the conservation laws of energy and momentum seemed not to apply. In 1930, Wolfgang Pauli proposed the hypothesis of the existence of a massless and neutral particle, having the "missing energy and momentum"; Enrico Fermi proposed its name: "neutrino", the small neutral one.

There are three types of neutrino, $\nu$, (and their corresponding antiparticles), each named after the particle they produce in the rare case of interaction with matter;
- the electron neutrino, $\nu_e$, discovered by Reines and Cowan in 1956
- the muon neutrino, $\nu_\mu$, discovered by Lederman, Schwartz, and Steinberger in 1962, at Brookhaven
- the tau neutrino, $\nu_\tau$, discovered at Fermilab, 2000

Neutrinos are tracers of energetic hadron acceleration in astrophysical sources since they can only be produced from hadronic interactions. They have tiny mass and are neutral, so they interact extremely feebly with matter (energy) and they can travel exceptionally long distances before interacting; those attributes make the neutrino a unique messenger of the mighty powers that rule the Universe. But those attributes make also the neutrino extremely hard to detect.

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Neutrinos are detected tracing their interactions’ products (electrons, muons and taus) in a transparent medium using Cherenkov radiation.

III. THE NEUTRINO ASTRONOMY

On 24.2.1987 astronomers had observed a supernova, $1.6 \times 10^5$ ly away, in the Large Magellan Cloud. And IMB and Kamiokande discovered that on the same date, an unexpected...
burst of 19 neutrinos was detected [3]. Neutrino astronomy was born.

Neutrino telescopes will eventually help us to understand and extend our knowledge in [1]:

- Galactic and extragalactic neutrino sources and cosmic accelerators, namely detecting neutrinos which are produced by galactic e.g. X-ray binaries or extragalactic sources, such as the active galactic nuclei (AGNs);
- The search for dark matter particles; their annihilation or decay will eventually give neutrinos e.g. neutralinos trapped in the Sun or the Earth.
- Study of the Ultra High Energy neutrinos, with energies more that 10 PeV since no terrestrial accelerator can produce these energies. If the neutrino telescope is large enough the limitation of low flux can be, in part, overcome and this might be the only way for High Energy Physics to reach these Ultra High Energies.
- Multiple W/Z production. Search for possible substructure of the elementary particles i.e. compositeness of quarks and leptons.
- Neutrino oscillations using neutrinos produced in the atmosphere and Long Base Line neutrino oscillations using one of the existing high-energy physics accelerators.
- Supernova detection.
- The Unexpected. A new observational window will open up with these neutrino telescopes. No one has ever viewed sites in the Universe shielded by more than a few hundreds grams of matter. One should keep in mind that every time a new brand of astronomy opened up, a new class of phenomena was discovered.

IV. THE NEUTRINO DETECTOR

High-energy neutrinos interact weakly with matter producing, as was stated before, electrons, muons or taus. The produced charged particle has essentially the direction of the parent neutrino.

M. Markov first proposed to use the sea as a neutrino Cherenkov detector [4, 5]. For neutrino energies of a GeV and above, up to the many PeV, the water Cherenkov technique seems to be the best technique, i.e., we can detect the Cherenkov light emitted by the muon of CC neutrino interactions. When such interactions occur in the sea water or seabed close to the detector, these charged particles can be observed by the Cherenkov photons that they emit transversing the water volume, using the neutrino detector; arrays of sensitive optical detectors, the so called Optical Modules. Electrons have a very short path and they produce a flash of light confined in a very small volume and tau has a very long track in water (several km long) but they are rare. Muons, depending on their energy, have a track of several tens of metres to few km long and produce a lot of Cherenkov photons; from the arrival time and intensity of the light pulses detected by the optical detectors, the direction of the muon, and hence that of the incident neutrino, can be reconstructed.

The above described neutrino detection is of course the Signal. Atmospheric muons are abundant and they also produce Cherenkov radiation that can easily blanket the neutrino-induced muons; they are the Noise (or to be exact, part of the noise, see below). In order to increase the signal/noise ratio (s/n) we should shield our detector from those atmospheric muons; in land detectors this shielding is provided by the rocks above the detector while in a water detector this shielding is provided by the water column, therefore the detector should be deployed as deep as possible.

Another source of noise is radioactivity in the sea and bioluminescence. In sea water the main source of radioactivity is Potassium-40. Moreover bioluminescence, produced by sea life, is a source of light in the detector that we have to take in account.

A sea neutrino detector has to fulfil several requirements:

- Wide area with a gentle slope; to be possible to increase the size of the detector thus to increase the sensitivity and angular resolution of the detector and determine the direction of the detected tracks with higher accuracy
- Short distance from the shore; to minimise the cost of the electro-optical connections between the detector and the shore station. This cable is required in order to transmit data to shore station and power the detector. Moreover short distance form the shore increase safety and easiness of operations
- Deep waters; to reduce the noise background from the down coming atmospheric muons and to reduce bioluminescence since biological activity diminishes with depth
- Clear waters; to reduce light attenuation and increase the active volume of the detector
- Low underwater currents speeds; to minimise mechanical stress on the detector components and movements of the optical modules and excitation of bioluminescence
- Low sedimentation and biofouling; to minimise the sedimentation covering on the Optical Modules and to increase the detector lifetime
- Low optical noise; in order to increase the s/n ratio

V. THE NESTOR SITE

All the requirements described above for a seawater neutrino detector could be found in the Ionian Sea off the south-western tip of the Peloponneseus (figure1). Extensive surveys in 1989, 1991 and 1992 [6, 7] have located a large flat abyssal plateau of 8x9km2 with a mean depth of 4500 m; the so-called NESTOR basin. Situated on the side of the Hellenic Trench that lies between the west coast of the Peloponneseus and the submarine East Mediterranean Ridge, the site is well protected from major deep-water perturbations. Moreover, if deeper waters are required, the Oinousse Pit, the deepest part of the Mediterranean with a 5200 m depth, is located a few km away from the NESTOR basin. The typical coordinates of the, so-called, NESTOR site are 36° 37’ N and 21° 35’ E. The location has a mean depth of 4000 m, is 7.5 nautical miles from the island of Sapienza, where there are two small harbours, and 11 nautical miles from the port of Methoni, while substantial port facilities are available 17 nautical miles away in the bay of Navarino where the town of Pylos is located. The sea bottom of NESTOR site has a clay deposit
accumulated over some tens of thousands of years which provides good anchoring [8].

Measurements of water transparency, using in-lab spectrophotometric analysis of a large number of samples and deployment of open geometry photometers in situ, down to 4000 m of depth [9, 10], show transmission lengths of 55±10m at a wavelength of 460 nm, stable temperatures of 14.2ºC and water current velocities well below 10 cm/s [11, 12, 13, 14]. Typical underwater current at the NESTOR site, obtained within the KM3NeT framework, is shown in figure 2.

Extensive studies of sedimentation [8] and biofouling are performed in the NESTOR site [15]. In particular, for sedimentation, several LIMS (Light Intensity Measuring System), each comprised of 32 photodiode, 2 mm² each, suitably distributed, oriented and located in a glass housing and illuminated by two LEDs located nearby and outside the glass sphere, were deployed (by NESTOR Institute and Hellenic Centre of Marine Research, HCMR) for long time series measurements of sedimentation rate. Results are still under study, but in figure 3a and 3b, a typical graph of the glass transparency (per % of initial transparency) versus time is shown for two photodiodes; one located at 0° and the second at 55° from the vertical. The distance between the photodiodes (in each pair) is less that 2 cm. In figure 3c and 3d, the derivatives of those graphs are shown with an indication of slight degradation of the glass sphere transparency due to sedimentation and/or biofouling, independently of the orientation on the glass housing. Thus, preliminary analysis indicates that the “stick on” probability on the Optical Module is zenith independent. Moreover, from studying the recorded data from all photodiodes we have the indication that we have a recurrent localised degradation of glass sphere transparency that we attribute to “flying” small size residues that attach on the glass housing for a short period of time. The subject is still under study.

Signal contamination by photons from radioactivity was studied. The only abundant radioactive source is the common in seawater potassium-40. Potassium-40 is well distributed in the seawater and is responsible to a noise on 15"
feasibility of a deep-sea neutrino telescope. The KM3NeT prototypes of the three pilot projects demonstrates the terminal access for deep-sea research. The success of the generation neutrino telescope, and to provide long-term kilometre sized deep-sea infrastructure detector; a next-composed to study the How and Where to build a cubic-NESTOR), the KM3NeT Design Study consortium, was from 10 European countries and the three Mediterranean consortia objectives are the building of a deep-sea neutrino telescopes pilot projects (ANTARES, NEMO and NESTOR) (including) 4 beaufort (about wind speed of 8m/s), it is quite obvious that at the NESTOR site, working at sea, is possible most of the time. For those graphs a ten years data recoded by the Hellenic National Meteorological Service were used [18].

Figure 5. Per cent Time period of a particular wind state versus wind state in Beaufort. Wind state 4 beaufort correspond to a wind speed of about 8cm/s

The above described site features indicate the NESTOR site as most suitable site for the installation of a large deep-sea neutrino telescope.

VI. THE KM3NeT

In 2006, a consortium of 40 Institutions and University from 10 European countries and the three Mediterranean neutrino telescopes pilot projects (ANTARES, NEMO and NESTOR), the KM3NeT Design Study consortium, was composed to study the How and Where to build a cubic-kilometre sized deep-sea infrastructure detector; a next-generation neutrino telescope, and to provide long-term terminal access for deep-sea research. The success of the prototypes of the three pilot projects demonstrates the feasibility of a deep-sea neutrino telescope. The KM3NeT consortium objectives are the building of a deep-sea neutrino telescope, the larger ever build detector, and to host facilities for marine and earth science research [19].

The main process than we expect to study is

\[ \nu_\mu + N \rightarrow \mu + x \]

for neutrinos with energies larger than 100 GeV. The angular resolution of the detector is foreseen to be less than (or equal) 0.1°, the time resolution better than 2 ns and it will be optimized for neutrino energies in the range of 1 TeV – 1 PeV. We expect the overall sensitivity to be better than the sensitivity of ICECUBE [20]. The above require that we know the positions of the OMs with a resolution smaller than 0.4m.

The KM3NeT neutrino telescope (detector) will be highly modular; a large number of identical modules should be deployed on a very deep-sea bed. Those modules will be of complex construction but their final design is not finalised yet. Modules will be produced, deployed and connected to shore facilities in line production during 4 years and we expect to accomplish data acquisition and system calibration within the first year. To build the modules and the ancillary units, we will use inoxidizable material; titanium or aluminium, glass or stainless steel with rubber or plastic separators between dissimilar material. For deployment we should use mainly locally available transport vessels and non-highly specialised surface vessels while the maintenance should be minimum with an expected lifetime of the detector of 10 years at least.

Last but not least the design should incorporate as few electronics in the sea as possible. Ideally will be to have all the raw data on shore and triggering, data selection and event preselection to be performed in the shore terminal station.

The primary of the KM3NeT Design Study is the development of a cost-effective design for a cubic-kilometre sized deep-sea infrastructure housing a neutrino telescope with unprecedented physics sensitivity and providing long-term access for deep-sea research, the evaluation of procedures for the assembly and construction of the infrastructure and the preparation of models for its operation and maintenance. Extensive description of the KM3NeT and its aim could be found in the Conceptual Design Report (CDR) in www.km3net.org/cdr [21]

VII. THE NESTOR PROTOTYPE

The pioneer Mediterranean neutrino detector is the NESTOR neutrino telescope; a prototype was deployed in 2003. The basic element of the NESTOR detector is a hexagonal star (or floor) with Optical Modules. Each Optical Module comprise of a 15" photomultiplier (HAMAMATSU – R2018) inside a 17" diameter and 15mm thick glass housing sphere (BENTHOS) with the appropriate DC-DC high voltage converter (EMI) [22]. Six arms, built from titanium tubes to form a lightweight lattice girder, are attached to a central titanium latticed basket. At the end of each arm a pair of Optical Modules are attached, one with the photocathode facing upwards and the other downwards. The electronics for the floor is housed inside a 1m-diameter titanium sphere on special Al panels. The nominal floor diameter is 32 m; the prototype deployed has a diameter of 12m. A full NESTOR tower would consist of 12 such stars stacked vertically with a spacing of 30m between them.
Every star (in the prototype, one star) is flexibly attached to the Anchor Unit, a sea bottom unit, pyramidal construction with Al tubing, that contains the anchor, the junction box, several environmental sensors and the sea electrode that provides the electrical power return path to shore, figure 6. A standard deep-sea electro-optical cable connects the "junction box" to the shore while light electro-optical cables connect the junction box to the stars. The junction box houses the termination of the sea-end of the electro-optical cable, the fan-outs for optical fibres and power to the floors, power smart fuses and a small monitoring system. Calibration modules, above and below each floor, house LED flasher units that are used for calibration of the detector and they are controlled and triggered from the floor electronics.

The floor electronics consist of several electronics boards, the required DC-DC converters and environmental sensors housed inside the one-metre diameter titanium sphere and mounted on aluminium frames, electrically isolated from the sphere (and the sea). Special deep-sea cables connect the Optical Modules to the titanium sphere through GISMA deep-sea connectors to the floor electronics, while the deep-sea electro-optical cable is 30km long and has 18 fibres and a conductor that connects the floor electronics, through the junction box, to the "ShoreBoard" located in the Shore Station.

There are two main DAQ boards: The "FloorBoard", a multilayered board that manage signal reception, procession, trigger and communications and the "Housekeeping Board", a pair of multilayered "piggyback" boards that manage system monitoring and controlling functions.

The FloorBoard is the main board equipped with FPGAs and LPDs for computing power [23]. It receives the PMT signals, resolve the majority logic triggering and perform waveform capture, digitization and event formatting [24]. Moreover, it handles the communications with the ShoreBoard; sending the data to shore and receiving the clock signal, commands and operational parameters.

The heart of the FloorBoard (figure 7) is an ASIC developed at LBNL, the “Analog Transient Waveform Digitizer” (ATWD) [25]. Each ATWD has four channels with 128 common-ramp, 10-bit, Wilkinson ADCs that, after activation, digitize all 128 samples of a selected channel. The sampling rate is controlled and may be varied from 0.2 to 2.0 Gsamples/s. There are five ATWDs on the Floor Board, providing twenty digitization channels. Three channels per IC are used to digitize PMT signals while the forth is used to digitize the 40MHz clock signal sent from the shore in order to check the sampling rate stability. A sampling rate of 273M samples/s was used giving a sampling period of 3.66ns. This gives a dynamical range (active time window) for each ATWD channel of 465ns.

The remaining 4 channels are used to digitize the trigger majority logic signal, to provide information for the synchronization and timing checks and for internal calibration functions.

The event trigger is generated when the required number of PMT signals above a threshold is fulfilled (majority coincidence). The trigger window is adjustable; with the physical layout of the detector floor presently deployed, the trigger window was set at 60ns. The leading edge of the trigger signal is defining the trigger absolute time occurrence with respect to the 40MHz clock and initiates the PMT signal capture by the ATWDs, the reading of the environmental parameters and, after packaging, data transmission to the shore. Forced trigger on demand, by command from the shore control system, could also force data taking, without PMTs signal, for calibration purposes.
The Housekeeping Boards [24] regulate the powering of the PMTs and their high voltage and monitors the PMTs high voltage and data from the environmental sensors. Moreover it operates the LED calibration flashers suspended above and below the floor. In addition a Smart PMT Fuse board protects the system from shorts on any Optical Modules line.

The Shore electronics consist of ShoreBoard and several-networked computers. The Shore Board [24, 26], connected on the EISA bus of the Data Acquisition computer, performs all communication with the deployed detector floor, receiving data and sending commands to the FloorBoard through two fibres of the 30km long electro-optical cable. Event data packages received by the ShoreBoard are stored temporarily in local buffers. Then, every 13 events, the stored data are sent and stored in the computer's permanent storage facilities for keep, distribution and analysis. In addition of the above, the Shoreboard sends a 40MHz clock to the FloorBoard as well control commands, change of the trigger logic parameters and allow the reprogramming of the FloorBoard FPGA/PLDs within the Floor Board, if required.

The NESTOR prototype was deployed successfully March 2003 using the cable-ship RAYMOND CROZE (FranceTelecom). The first deep-sea muon data transmitted to shore, through a 30km long electro-optical cable to the Methoni counting room was achieved on the 30th of March 2003. Detailed analysis could be found elsewhere [14, 27].

VIII. THE DELTA BERENIKE
For the construction of the KM3NeT, the km³ neutrino passing ships. This rocking, pitching and rolling motion may lead to catastrophic situations by exciting oscillations on the scientific payload in the sea underneath it.

The NESTOR Institute has constructed a special purpose deployment platform named DELTA – BERENIKE (figure 8). The design of the DELTA – BERENIKE has been inspired by the off shore oil rigs of the North Atlantic. DELTA-BERENIKE is a Central Well Ballasted Platform of triangular structure with 51m long sides and 48m long base. At each apex of the structure, two concentric cylinders (4 and 6m diameter each) are located, providing the required buoyancy and housing the three (one in each apex) motive engine systems; a CATERPILLAR 322 BHP motor coupled to a SCHOTTEL 360° SPJ57RD jet, which can rotate a full 360°. Using the combinational power and thrust direction of those machines, DELTA-BERENIKE can sail to the required course, dock or hold position on the open sea. The opening in the middle of the triangular structure assures balanced access to the sea surface. The platform is equipped with assorted bridge crane, cranes, winches, etc to be used as required.

DELTA-BERENIKE is equipped with a Dynamic Positioning system that permits precise navigation and station holding in the open sea. This will extremely useful during deployment of NESTOR or KM3NeT instrumentation to exact positions on the seafloor.

It will be also valuable on measuring, with sub degree accuracy, the absolute angular resolution of the deployed neutrino telescope installing cosmic ray arrays on her deck and keeping position above the deployed neutrino telescope.

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The European XFEL Project

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Abstract

The European XFEL project is a 4th generation photon source to be built in Hamburg. Electron bunches, accelerated to 17.5 GeV by the XFEL linac, are distributed to three long SASE undulators. There photon pulses with full lateral coherence and wavelengths between 0.1 nm and 4.9 nm (12.4 keV and 0.8 keV) are generated for three beamlines. It will deliver around $10^{12}$ photons within each 100 fs pulse, reaching a peak brilliance of $10^{33}$ photons $^{-1}$ mm$^{-2}$ mrad$^{-2}$ (0.1% BW)$^{-1}$. Thus it will offer unprecedented possibilities in photon science research including nano-object imaging and studies (e.g. by coherent X-ray scattering) and ultra fast dynamic analysis of plasma and chemical reactions (e.g. by X-ray photo correlation spectroscopy). The detector requirements for such studies are extremely challenging: position sensitive area detectors have to provide a dynamic range of $\geq 10^4$, with single-photon sensitivity, while withstanding radiation doses up to 1 GGy (TID). Furthermore the detectors have to record data from trains of up to 3000 photon pulses, delivered at 5 MHz, which repeat every 100 ms. Three consortia have picked up the challenge to build pixel detectors for the European XFEL DEPFET-APS, AGIPD$^1$ and LPD. Besides the European XFEL source and the related experimental techniques, the concepts and specialities of the DEPFET-APS, AGIPD and LPD detectors are discussed.

I. INTRODUCTION

The application of ultra-short pulses of coherent, visible light generated by lasers provided many fields of research with new insights and discoveries. Detailed investigations on the dynamics of chemical reactions and on the structure of materials can serve as classical examples. Shorter wavelengths, in the regime from VUV to hard X-rays, on the other hand permit the investigation of even smaller structures. But even when created in synchrotrons, the three key features of advanced laser light sources – coherence, ultra short pulse length and power – were not available before the discovery of the SASE$^2$ principle of free electron lasers. However, the length of SASE undulators and the repeated perturbation of the electron beam induced by the random photon-emission process in a storage ring put up a lower limit to the phase space of the electrons in the magnetic lattice. The solution to overcome this limitation and thus further improve brilliance and coherence of the radiation is the employment of a single pass electron source, i.e. a linear accelerator. The TESLA$^3$ technology developed at DESY for the ILC would make up an ideal electron source to drive such a SASE FEL. So it comes to no surprise that already the TTF1 and TTF2$^4$ accelerators were coupled to SASE undulators. The latter was renamed to FLASH$^5$ when it went into user operation in 2005 as the first VUV FEL source. In turn the intriguing idea of using Tesla/ILC to deliver electrons for an FEL emerged. The performance of this source would be unprecedented and open the doors for new areas in photon science.

Figure 1: Peak brilliance of current and projected synchrotron radiation sources.

The obvious scientific benefit, the uncertainty about the construction of the future ILC and the availability of technology, know-how and experience at DESY led to the proposal of the European XFEL project in 2003 as a stand-alone facility. It is set up as a limited liability company (XFEL GmbH), receiving funding from 12 European countries plus China and Russia. The scientific potential is also unprecedented, exceeding existing 3rd generation synchrotron sources in coherence and brilliance by

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$^1$Originally presented as Hybrid Pixel Array Detector (HPAD) but renamed to AGIPD for uniqueness.
$^2$Self-Amplified Spontaneous Emission
$^3$TeV Superconducting Linear Accelerator
$^4$Tesla Test Facility
$^5$Free electron LASer in Hamburg
several orders of magnitude. Fig. 1 shows the peak brilliance of the European XFEL in comparison to other 3\textsuperscript{rd} generation sources, which it surpasses by a factor $\approx 10^9$. Also in average brilliance it exceeds existing 3\textsuperscript{rd} generation sources by a factor of $\approx 10^5$.

II. THE EUROPEAN XFEL SOURCE

The European XFEL source consists of two parts: A 20 GeV electron linear accelerator and three electron beamlines with SASE undulator magnets. Both parts are mounted in a 3.4 km long tunnel, 12 m to 44 m underground. It leads from the premises of Deutsches Elektronen-synchrotron (DESY) in Hamburg-Bahrenfeld to the experimental site in Schenefeld, Pinneberg district, in the state of Schleswig-Holstein, as shown in fig. 2.

Figure 2: Geographical map of the European XFEL civil construction.

A. The Electron Accelerator

The electron accelerator’s beam is generated in a laser-driven photocathode RF gun, located in the injector building on the DESY site in Hamburg-Bahrenfeld. The electrons are then transferred to the main accelerator tunnel, where these enter the first acceleration unit consisting of four superconducting accelerator modules, which in turn contain eight RF cavities made of pure niobium each. The modules operate in the L-band (1.3 GHz) with four modules driven by one RF station. Having passed the first module, the electrons of 0.5 Gev pass a 3\textsuperscript{rd} harmonic RF-system to adjust the longitudinal phase space conditions and a magnetic bunch compressor. After passing three more superconducting accelerator modules and a second bunch compressor, the electron bunches have reached 2 Gev/e and a peak current of 500 kA, which is 100 times higher than the original peak current provided by the injector. The final acceleration to the maximum beam energy of 20 GeV is accomplished in the main part of the linac – 100 superconducting accelerator modules driven by 25 RF stations. The following conventional electron beamline is equipped with collimation and feedback devices, the latter used for trajectory feedback and transfers the electron bunches to the beam distribution system, which mainly consists of two kicker magnets: a fast kicker to remove “bad” bunches and to mask the switching transition of the (slow) flat-top kicker. The latter is used to switch the electron beam between the SASE2 and the (combined) SASE1/SASE3 electron beamlines. The following list summarises the key parameters of the electron linac, while fig. 3 shows the schematic layout of the accelerator.

- $W_{\text{max}} = 17.5 \text{GeV}(20 \text{GeV})$
- $I_{\text{peak}} = 5 \text{kA}$
- $Q_{\text{bunch}} = 1 \text{nC}$
- $P_{\text{beam}} = 600 \text{kW}$
- $N_{\text{bunch}} = 3000(3250)$
- $E_{\text{acc}} = 23.6 \text{MV/m}$
- $f_{\text{bunch}} = 5 \text{MHz}$
- $f_{\text{cycle}} = 10 \text{Hz}$
- 29 RF stations
- 928 cavities
- 116 modules
- $P_{\text{RF}} = 5.2 \text{MW}$
- Emittance (@ undulator) = 1.4 mm × mrad
- $\Delta E_{\text{(@undulator)}} = 1 \text{MeV}$
- 2 bunch compressors:
  - 1/20@0.5 GeV
  - 1/5@2.0 GeV

Figure 3: Schematic layout of the European XFEL accelerator.

The relatively strange bunch structure depicted in fig 4 is a compromise of incompatible requirements:

- highest electron density possible for maximum FEL pulse intensity
- permissible heat load of the superconducting cavities ($\leq 3000$ full bunches/s)
- minimum bunch spacing for trajectory feedback
B. SASE Undulator Sources and Beamlines

Accelerated charges emit electromagnetic waves, which is one of the predictions of Maxwell’s equations. Thus deflected (i.e., transversely accelerated) electrons emit synchrotron radiation, which has a continuous spectrum. To achieve a coherent, monochromatic beam, the emitted radiation has to interact with the emitting media – the electron beam packet in this case – on a periodical basis. But unlike in a dye laser (which in most other respects will serve as a good analogue) there is no “resonator” for X-rays and the real periodic structure of an undulator magnet has to be used: When an electron bunch enters an undulator, it will spontaneously emit photons of several wavelengths when passing the first "bents" of an undulator. Given the right direction and wavelength of this random seed, such photons from the rear part of the electron bunch can interact with photons further ahead in the bunch passing the next "bent" of the undulator and stimulate them to coherently emit synchrotron radiation at the same wavelength as the initial photon (c.f. fig. 5). Thus the power and intensity of the photon beam will exponentially rise along the length of the undulator, while the energy loss of the emitting electrons will cause a microbunch structure of the electron packet. This microbunching will ultimately saturate the intensity of the radiation and terminate the self-amplification process, since the limit for the electron density in the microbunches is reached after a certain number of undulator periods. This is illustrated in fig. 6. Obviously not only the fundamental wavelength, defined by electron energy, the magnetic field and period length of the undulator, but also higher harmonics of it are amplified.

III. EXPERIMENTS

A. XPCS - X-Ray Photon Correlation Spectroscopy

X-ray photon correlation spectroscopy probes the dynamical properties of condensed matter, like e.g. phase transitions, protein folding, viscoelastic flow, crystalline phase transitions or domain switching. These are accessed in the time domain by looking at the normalised autocorrelation function:
which can be calculated from the speckle pattern of the photons scattered by the material. However, in sequential XPCS setups \( \tau \) in eq. 1 is limited by the rate of the synchrotron source or the detector, as fig. 7 shows. Thus only phenomena with time constants larger than \( \tau \) can be investigated.

1) XPCS splitted-pulse technique

To overcome this limitation and investigate phenomena occurring on time scales close to the length of the X-ray pulse, the so-called splitted-pulse technique can be employed. It is illustrated in fig. 8 and does no longer permit the calculation of the autocorrelation function, since the result is only a single image. However the change of contrast with the pulse delay can be used to calculate the temporal evolution of the system.

\[
g(t) = \frac{\langle n(t)n(t+\tau) \rangle}{\langle n \rangle^2}, \tag{1}
\]

Figure 7: Illustration of the XPCS sequential technique (taken from [2]).

Figure 8: Illustration of the XPCS splitted-pulse technique (taken from [2]).

1) Pump-Probe Experiments

This is a third class of XPCS experiment, which can only be used to investigate phenomena, which are triggered by an external pump pulse. This is usually an electromagnetic signal like switching on a magnetic field or a laser pulse. As fig. 9 shows, the autocorrelation function \( g(t) \) can now be calculated from the delay between pump and probe pulse. Also in this case the length of the synchrotron pulse defines a lower limit for \( \tau \). The long readout time of conventional imaging detectors (in the region of several ms) and the x-ray pulse rate of synchrotrons set the lower limits for the time scale of phenomena accessible with XPCS sequential techniques to the regime of milliseconds. Circumventing these limits with splitted-pulse or pump-probe techniques, which is not always possible, moves this limit to fractions of a microsecond, since the length of a synchrotron pulse is typically \( \approx 200 \text{ ps} \) long. The European XFEL will -together with suitable detectors- lower the limits for phenomena accessible to sequential XPCS techniques to the \( \mu \text{s} \) regime, due to the 200 ns bunch spacing. In case of splitted-pulse and pump-probe experiments an even bigger improvement is achieved: The XFEL pulse length of \( \leq 100 \text{ fs} \) will move the limits to the

---

### Table 1: Properties and scientific applications of the 3 XFEL SASE undulator sources.

<table>
<thead>
<tr>
<th>Beamline</th>
<th>X-ray features</th>
<th>Proposed instruments</th>
</tr>
</thead>
<tbody>
<tr>
<td>SASE 1</td>
<td>( \approx 12 \text{keV} )</td>
<td>PCS 1 X-ray Photon Correlation Spectroscopy</td>
</tr>
<tr>
<td></td>
<td>High coherence</td>
<td>FDE 1 - Femtosecond Diffraction Experiments</td>
</tr>
<tr>
<td></td>
<td>High flux</td>
<td>SPB 1 - Single Particles and Biomolecules</td>
</tr>
<tr>
<td></td>
<td>3\textsuperscript{rd} harmonic</td>
<td></td>
</tr>
<tr>
<td>SASE 2</td>
<td>( 0.25 \ldots 3.1 \text{keV} )</td>
<td>CXI 1 - Coherent X-ray Imaging</td>
</tr>
<tr>
<td></td>
<td>High coherence</td>
<td>HED 2 - High Energy Density</td>
</tr>
<tr>
<td></td>
<td>High flux</td>
<td>XAS 2 - X-ray Absorption Spectroscopy</td>
</tr>
<tr>
<td>SASE 3</td>
<td>( 0.25 \ldots 3.1 \text{keV} )</td>
<td>HED 1 - High Energy Density</td>
</tr>
<tr>
<td></td>
<td>High coherence</td>
<td>SQS 1 - Small Quantum Systems</td>
</tr>
<tr>
<td></td>
<td>High flux</td>
<td>XAS 1 - X-ray Absorption Spectroscopy</td>
</tr>
<tr>
<td></td>
<td>3\textsuperscript{rd} harmonic</td>
<td>SQS 1 - Small Quantum Systems</td>
</tr>
</tbody>
</table>

---
picosecond regime, such that the dynamics of most chemical reactions become accessible.

![Figure 9: Illustration of the XPCS pump-probe technique (taken from [2]).](image)

Figure 9: Illustration of the XPCS pump-probe technique (taken from [2]).

![Figure 10: XCDI of a picture etched into a 35 nm thick layer of silicon nitride [3].](image)

Figure 10: XCDI of a picture etched into a 35 nm thick layer of silicon nitride [3].

**Top left:** TEM image of the sample.

**Top right:** Diffraction pattern from the first FLASH UV pulse.

**Bottom left:** Image reconstructed from the diffraction pattern without using information about the sample.

**Bottom right:** Diffraction pattern from a second FLASH pulse proving the destruction of the sample.

**B. XCDI - Coherent Diffraction Imaging**

This technique can be used at the European XFEL to investigate the structure of cells, viruses, biomolecules and other nano-objects. These structures were only accessible if these objects could be forced to form regular structures, as it is well known from protein crystallography. However, it should also be possible to image single molecules and nano-objects, if the very low crossection can be overcome with a sufficiently high flux of coherent photons. But such a high photon density will also ionize the sample and cause it to disintegrate in a coulomb explosion. At FLASH it was shown, that this process takes longer than \( \approx 100 \text{ fs} \) as shown in fig. 10, and that it is possible to reconstruct the object by means of a phase retrieval algorithm, without using any information about the original. Given the higher intensity and photon energy, it will be possible to XCDI to Biomolecules and similar objects to reconstruct their structure, as illustrated in fig. 11.

![Figure 11: Schematic principle of XCDI with single biomolecules [3].](image)

Figure 11: Schematic principle of XCDI with single biomolecules [3].

### IV. 2D Area Detectors

The diffraction patterns from such experiments will be recorded with pixel detectors, which not only have to satisfy the experiment type specific requirements given in tab. 2, but also have to comply with the European XFEL’s time structure shown in fig. 4. Further challenges arise from the high photon flux: The innermost pixel regions will be exposed up to \( 10^5 \) photons per shot. Thus the detectors will accumulate up to 1GGy of TID within 3 years. The resulting effects and radiation damage in silicon sensors is investigated in a common research project for all XFEL detector developments. Despite the shielding by the sensor, up to 10 % of the deposited dose will be accumulated by the readout asics beneath the sensors, which requires the use of radiation tolerant deep submicron CMOS technology and/or radiation hard layout techniques. Another issue related to the high photon flux is the charge density (\( \approx 10^8 \) electron-hole pairs) generated by up to \( 10^5 \) photons incident on a 10 \( \mu \text{m} \times 10 \mu \text{m} \) area in some experiments. Here the charge of the electrons will shield the drift field and a deterioration of the spatial resolution by diffusion before drift – the so-called charge explosion – is expected. In turn its investigation within a research project for all XFEL detectors has been established. Despite these obstacles, the DEPFET-APS LPD and AGIPD consortia took up to the challenge to build pixel area detectors for the European XFEL. The basic concepts and parameters of these detectors are summarised in tab. 3.
Table 2: Detector requirements of different XFEL experimental techniques.

<table>
<thead>
<tr>
<th></th>
<th>PPnX</th>
<th>PPX</th>
<th>CDI</th>
<th>SPI</th>
<th>XPCS</th>
</tr>
</thead>
<tbody>
<tr>
<td>E [keV]</td>
<td>6 . . 15</td>
<td>12</td>
<td>0.8 . . 12</td>
<td>12.4</td>
<td>6 . . 15</td>
</tr>
<tr>
<td>ΔE/E</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>QE</td>
<td>≥ 0.8</td>
<td>≥ 0.8</td>
<td>≥ 0.8</td>
<td>≥ 0.8</td>
<td>≥ 0.8</td>
</tr>
<tr>
<td>Rad Tol</td>
<td>10^{16} ph</td>
<td>10^{16} ph</td>
<td>2 × 10^{16} ph</td>
<td>2 × 10^{15} ph</td>
<td>2 × 10^{14} ph</td>
</tr>
<tr>
<td>Size</td>
<td>200 deg</td>
<td>120 deg</td>
<td>120 deg</td>
<td>120 deg</td>
<td>0.2 deg</td>
</tr>
<tr>
<td>Pixel</td>
<td>7 mrad</td>
<td>100 μm</td>
<td>0.1 mrad</td>
<td>0.5 mrad</td>
<td>4 mrad</td>
</tr>
<tr>
<td># pixels</td>
<td>500 × 500</td>
<td>3k × 3k</td>
<td>20k × 20k</td>
<td>4k × 4k</td>
<td>1k × 1k</td>
</tr>
<tr>
<td>tiling</td>
<td>&lt; 20%</td>
<td>&lt; 10%</td>
<td>See text</td>
<td>&lt; 20%</td>
<td></td>
</tr>
<tr>
<td>L Rate</td>
<td>5 × 10^4</td>
<td>3 × 10^6</td>
<td>10^7</td>
<td>10^4</td>
<td>10^3</td>
</tr>
<tr>
<td>G Rate</td>
<td>3 × 10^7</td>
<td>10^7</td>
<td>10^7</td>
<td>10^7</td>
<td>10^6</td>
</tr>
<tr>
<td>Timing</td>
<td>10 Hz</td>
<td>10 Hz</td>
<td>5 MHz</td>
<td>10 Hz</td>
<td>5 MHz</td>
</tr>
<tr>
<td>Flat F</td>
<td>1%</td>
<td>1%</td>
<td>1%</td>
<td>1%</td>
<td>1%</td>
</tr>
<tr>
<td>Dark C</td>
<td>&lt; 1 ph</td>
<td>&lt; 1 ph</td>
<td>&lt; 1 ph</td>
<td>&lt; 1 ph</td>
<td>&lt; 1 ph</td>
</tr>
<tr>
<td>R Noise</td>
<td>&lt; 1 ph</td>
<td>&lt; 1 ph</td>
<td>&lt; 1 ph</td>
<td>&lt; 1 ph</td>
<td>&lt; 1 ph</td>
</tr>
<tr>
<td>Linearity</td>
<td>1%</td>
<td>1%</td>
<td>1%</td>
<td>1%</td>
<td>1%</td>
</tr>
<tr>
<td>PSF</td>
<td>1 pixel</td>
<td>100 μm</td>
<td>1 pixel</td>
<td>1 pixel</td>
<td>1 pixel</td>
</tr>
<tr>
<td>Lag</td>
<td>10^{-3}</td>
<td>10^{-3}</td>
<td>7 × 10^{-5}</td>
<td>10^{-3}</td>
<td>10^{-3}</td>
</tr>
<tr>
<td>Vacuum</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Other</td>
<td>Hole</td>
<td>Hole</td>
<td></td>
<td></td>
<td>Hole</td>
</tr>
</tbody>
</table>

Table 3: Concepts of the three different XFEL pixel detector projects.

<table>
<thead>
<tr>
<th></th>
<th>DEPFET-APS</th>
<th>LPD</th>
<th>HPAD</th>
</tr>
</thead>
<tbody>
<tr>
<td># of pixels</td>
<td>1 k × 1 k</td>
<td>1 k × 1 k</td>
<td>1 k × 1 k</td>
</tr>
<tr>
<td>Pixel size</td>
<td>200 μm × 200 μm</td>
<td>500 μm × 500 μm</td>
<td>200 μm × 200 μm</td>
</tr>
<tr>
<td>Sensor</td>
<td>DEPFET array</td>
<td>Si-pixel</td>
<td>Si-pixel</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>≥ 10^4 ph</td>
<td>2 × 10^4 ph (10^5 ph)</td>
<td>≥ 2 × 10^4 ph</td>
</tr>
<tr>
<td>Noise</td>
<td>≈ 15 × 10^{-3} ph</td>
<td>≈ 0.21 ph (≈ 0.93 ph)</td>
<td>≈ 45 × 10^{-3} ph</td>
</tr>
<tr>
<td></td>
<td>≈ 50e</td>
<td>≈ 700 e (≈ 3100 e)</td>
<td>≈ 150 e</td>
</tr>
<tr>
<td>Concept</td>
<td>DEPFET nonlinear gain compression</td>
<td>Multiple gain paths</td>
<td>Adaptive gain switching (preset gain option)</td>
</tr>
<tr>
<td></td>
<td>Per-pixel ADC</td>
<td>On-chip ADC</td>
<td></td>
</tr>
<tr>
<td>Storage</td>
<td>8 bit DRAM</td>
<td>3-fold analogue</td>
<td>2 bit digital + analogue</td>
</tr>
<tr>
<td>Storage depth</td>
<td>≥ 256</td>
<td>512</td>
<td>≥ 200</td>
</tr>
<tr>
<td>Challenges</td>
<td>Linearity &amp; calibration</td>
<td>Preamplifier: noise, dynamic range &amp; PSRR</td>
<td>Dynamic gain switching</td>
</tr>
<tr>
<td></td>
<td>In-pixel ADC</td>
<td>Analogue storage</td>
<td>Charge injection</td>
</tr>
<tr>
<td></td>
<td>DRAM refresh</td>
<td>Analogue storage</td>
<td>Analogue storage</td>
</tr>
<tr>
<td></td>
<td>Power budget</td>
<td>Pixel area</td>
<td>Pixel area</td>
</tr>
</tbody>
</table>

Radiation hardness
A. Large Pixel Detector (LPD)

This detector to be built by a consortium consisting of STFC and the University of Glasgow [4] will feature a shingled arrangement of the detector tiles with pixels of 500 µm × 500 µm – thus the name. The overall layout of the detector is depicted in fig. 13, while a single sensor module is depicted in fig. ??.

The sensor of each module is divided in $128 \times 32$ pixels, read out by 8 ASICs with 512 channels each. The basic concept of this readout ASIC is a threefold readout pipeline fed by the same preamplifier, but with different gains. This concept, which is depicted in fig. 14, has been successfully used for the readout of the high dynamic range in several calorimeters at CERN. Single photon sensitivity can be achieved with 20 pF feedback capacitance, as the noise simulation in fig. 15 shows.

B. DEPFET Active Pixel Sensor (DEPFET-APS)

This detector is proposed by a consortium of MPI Halbleiterlabor, Munich, DESY, the Universities of Bergamo, Heidelberg and Siegen, and the Polytechnico di Milano [5]. Unlike the other two detectors, it will make use of active sensor arrays based on the DEPFET principle. As shown in fig. ?? a potential well underneath the gate of the DEPFET will collect the charges generated by ionising radiation in the bulk of the transistor. The drain-source current in this transistor is than not only modulated by the gate voltage, but also by the field induced by the charges in the potential well. In case of the sensors used for the DEPFET-APS detector, this potential well extends underneath the source for higher energy levels. Small amounts of charge will therefore be trapped in the minimum of the well and fully contribute to the steering effect. If more charge is accumulated, some part of the charge is stored under the source and thus will not contribute to the steering effect: The characteristic of the DEPFET becomes nonlinear and a compression effect is achieved. The readout of a DEPFET sensor can be done e.g. by biasing it with a current source and reading the voltage at the source – the so-called source follower readout. The subsequent datapath is depicted in fig. 17: It consists of a preamplifier, a filter, sample and hold and an 8-bit ADC stage writing to DRAM based buffer memory inside each pixel. The DEPFET sensors are divided into $128 \times 512$ DEPFET pixels of 200 µm × 200 µm. The final detector will feature 1 megapixel and will consist of a planar arrangement of $8 \times 2$ sensors.
C. Adaptive Gain Integrating Pixel Detector (AGIPD)

This is a segmented planar 1 megapixel detector built by a consortium of the Universities of Bonn and Hamburg, DESY and PSI [6]. The detector will be constructed from 4 radially movable quadrants, such that the size of the central hole for the direct beam can be adjusted. Each quadrant consists of $2 \times 44$ sensors of $256 \times 128$ pixels each. The sensors are bump-bonded to $2 \times 4$ readout chips of $64 \times 64$ channels, which are mounted on a high-density interconnect flexprint, as shown in fig. 18.

To cover the required dynamic range of $2 \times 10^5$ photons, while providing single photon sensitivity, the charge sensitive preamplifier of each pixel features an adaptive gain: If the amplifier output exceeds a certain level, a discriminator is triggered, causing an additional feedback capacitor to be connected in parallel with the original one. By this the gain is lowered from $1/C_1$ to $1/(C_1 + C_2)$ without losing any of the already integrated charge.

The AGIPD pixels will feature three different gain settings (as shown in fig. 19) and their selection has to be propagated along with the analogue information. The latter will be recorded by double correlated sampling in an capacitor array, as is the gain setting by encoding it to easily distinguishable analogue levels, as depicted in the pixel schematic in fig. 20. By this the same readout path can be used for analogue and digital information. However, since the readout of 200 frames from the chip will take several 10 ms, signal droop caused by leakage currents in switches and capacitors becomes an issue and all analogue information is read before the encoded gain settings. The AGIPD consortium has identified this problem and is investigating leak-
age currents in the chosen 130 nm (IBM cmrf8sf DM) CMOS technology, also under the influence of temperature and radiation.

Figure 20: Schematic of a AGIPD readout chip pixel.

V. SUMMARY

- Signing of the Contract for the XFEL GmbH (company) scheduled for the begin of 2009, the start of civil construction is scheduled for Feb. 2009
- Accelerator: Prototype XFEL modules, similar to those of FLASH/TTF, exist and were successfully tested.
- Undulators: These modules are based on those used in FLASH, also here XFEL prototypes exist
- 2D area detectors
  - 3 projects took up the challenge
  - Individual solutions to the dynamic range challenge were elaborated
  - Same CMOS process for readout ASICs was selected by all 3 consortia.
- Ongoing studies on possible obstacles
  - Charge Explosion
  - Radiation hardness (test chips by LPD and AGIPD exist.)
- First pixels in silicon scheduled for 2009
- Full area detectors planned for 2012

REFERENCES

Development of a 3.2 Gpixel Camera for the Large Synoptic Survey Telescope (LSST)

John Oliver, Laboratory for Particle Physics and Cosmology, Cambridge, UK
jnoliver@fas.harvard.edu

Overview

• Major science drivers
• Critical specifications
• Telescope
  ➢ Sensors
  ➢ Readout electronics

Major Science Drivers

• "Synoptic survey" : Comprehensive & multipurpose
• Survey entire visible sky (20,000 deg²) in five filter bands (400 nm – 1,000 nm) every 3 nights
  ➢ Dark matter survey ➢ Weak gravitational lensing
  ➢ Dark energy probe ➢ Type 1a supernovae discovery > 10³/night
• Galactic structure
  ➢ Near Earth Objects & Potentially Hazardous Asteroids
• Transient phenomena

Dark Matter Survey

- Weak lensing -

Strongly lensed galaxy

- Weak lensing -
Measurements of ellipticity correlations of large numbers of faint galaxies ➢ "cosmic shear"

Tomographic reconstruction of dark matter density from shear data

T. Tyson

Dark Energy Measurement

- Type 1A Supernovae -

• High statistics measurements of Type 1A SN ➢ > 10³ per observing night
  • Redshift & distance measurement
    ➢ Fixed luminosity (standard candle) ➢ distance
  • Photometric redshift measurements in five filter bands to Z = 1.2

Deviations from linearity ➢ Acceleration ➢ Dark Energy ➢ Cosmological constant

T. Tyson
Critical Specifications
- Telescope -

- Survey telescope figure of merit “Etendue” \((\text{Dia})^2 \times (\text{FoV solid angle})\)
- Large aperture ~ 8.4 m, (6.7 m equivalent clear aperture)
- Large FoV ~ 3.5 deg
- Large focal plane ~ 64 cm diameter
- LSST Etendue ~ 320 (deg^2)(m^2)
- High “throughput”

Critical Specifications
- Camera & Sensors-

- Image sensors
  - Large focal plane ~ 64 cm dia
  - ~ 200x 16-Mpixel CCD image sensors, 10µm pixels (0.2") ~ 3.2 Gpixels
  - Back side illuminated
  - Small “Point spread function” - PSF (minimum spot size) ~ 7.5 µ (10 µ max)
  - Low f-number ~ 1.2 must be flat to 10µ (peak-valley) across focal plane
  - High quantum efficiency 400 nm – 1,000 nm (40%, 80%, 40%)
  - Low leakage ~ 1 e/s per pixel \(T \sim 100 \, ^\circ C\)
  - High “full well” capacity ~ 100,000 e/pixel
  - Back-to-back 15 second exposures on each piece of sky ~ Cosmic ray rejection
  - 2 second readout ~ low dead time, high throughput
  - Sky shot noise limited images ~ CCD read noise ~ 5 e rms
  - Focal plane contained in a contamination free evacuated cryostat to prevent fogging of sensor surfaces

- Back to back 15 second exposures on each piece of sky ~ Cosmic ray rejection

Note: Last three requirements highly constrain the readout topology

Critical Specifications
- Implications for readout & sensors -

- Typical sensitivity \(S = 5 \, \mu V/e\)
- \(C_g = 32 \, ff\)
- Dominant noise source ~ “KTC noise”
- KTC noise easily removed by
  - Correlated Double Sampling (Clamp & Sample)
  - Dual Slope Integration (optimal)
Dual Slope Integration sequence

a) Reset
b) Integrate baseline up
c) Move charge to output fet
d) Integrate signal down

\[ \sigma = \frac{1}{\sqrt{T_{int}}} \]

For typical “science grade” CCD

\[ T_{int} \approx 10 \text{ to } 20 \text{ sec} \]

Read noise vs Integration time

- At fpixel-read = 500 kpixels/sec
  - \[ T_{read} > \approx 2 \mu \text{s/pixel} \]

- Each CCD must have 16 parallel outputs & electronic readout channels
- \[ \sim 200 \] sensors
- \[ \sim 3,200 \] parallel readout channels

Critical Specifications

- Implications for Sensors -
  - 16x segments, gap-less
  - \( \frac{1}{2} \) k x 2k each
  - \( \sim 40 \text{ mm x 40 mm} \)

Critical Specifications

- Implications for Sensor Thickness -
  - Small PSF
  - Blue light has very small absorption length
  - Favors thin sensor to minimize diffusion
  - Favors full depletion in high resistivity silicon

- High QE in red
  - Red light has very long absorption length
  - Thin sensor would be transparent in red & near IR
  - Favors thick sensor

- Optimization: “Study of Silicon Sensor Thickness Optimization for LSST” [1]

- Calculations
- Simulations

Effect of sensor thickness on PSF

Beam divergence : f1.2 beam \( \rightarrow \) 46 deg max

Beam divergence in red, (simulation)

Effect of sensor thickness on QE

To get \( > 25\% \) QE @ -100C \( \Rightarrow \) \( t \leq 100 \mu \text{m} \)

Optimal sensor thickness = 100 \mu m

Sensor Requirements cont'

- Temperature Stability -
  - Sensor QE is very temperature dependent near \( \sim 1,000 \text{ nm} \)
  - For accurate photometry, temperature stability \( \sim \pm 0.1 \text{C} \)
  - Sources of heat
    - CCD gates (small)
    - CCD output amplifiers (medium)
    - Heat radiation through lens (large \( \sim \frac{1}{4} \text{ W per sensor} \))
    - Heat removal by thermal strips to a cryogenic plate
  - Thermal control loop
    - High stability temp sensors close to CCD package
    - Heaters \( \Rightarrow \) 0 to \( \sim \frac{1}{4} \text{ W per sensor on sensor package or cold straps} \)


Sensor Status

An array of “study” sensors has been produced by
• e2v
• STA/ITL
• 100μ to 150μ thickness
• All fully depleted between 10V – 25V “back window bias”
• Sizes 1 MPixels to 16 Mpixels
• Multiple output ports
• Tested at BNL
• Not final package

“Pre-Production” sensors
• e2v
• STA/ITL
• 100μ thickness
• Final packaging
  ⇒ 4 side buttable
  ⇒ Flat to 0 μ (p-v)
• Expected ⇒ Fall 2010

Focal Plane Construction

• 3 x 3 arrays of CCDs are mounted into a precision “Raft”
• 144 Mpixels per Raft
• 21 Rafts are mounted onto a grid (SiC) “Grid”
• Major issues
  • Each sensor has ~ 150 bond pads
  • Total of ~ 30,000 bond pads
  • Sensors reside in high-vacuum cryostat
  • To avoid 30,000 cryostat feedthroughs, all readout electronics is placed within cryostat.
  • Each Raft is modular. All its readout electronics must reside in the shadow of the Raft.
  • Raft electronics is divided into two sections
    • Analog, front end, in cryo-zone (-100C)
    • ADC/digital in warmer zone (-40C)

Camera Overview

Camera with filters

Cryostat Assembly

Raft Tower Assembly

9 Sensor Raft

21 “Science Rafts”
4 special purpose “corner Rafts”

~ 64 cm dia
Front End Electronics

- Located within “grid” - Operates at -100C to -120C
- Each “FEB” services 24 CCD segments - 6 FEBs per Raft
- Analog functionality in 2 ASICs
  - Analog Signal Processing ASIC (ASPIC)
- LPNHE/IN2P3 collaboration [1] - France
- Dual Slope Integrator: Programmable gain
- Specs:
  - en < ~ 5 nV/rt(Hz)
  - x-talk < ~ 10^{-3} (achieved in 1st version)
  - x-talk < ~ 10^{-3} (achieved in 1st version)
- Differential output to Back End Boards (ADCs) via shielded flex cable
- 8 channel ASIC, AMS 0.35 μCMOS @ 5V, ~ 25mW/ch

Sensor Control Chip (SCC)
- ORNL - U. Tennessee [1]
- Receives LVDS signals from BEBs
- Converts to Clock levels to CCDs
- Parallel gates (4), Serial gates(3), Reset(1)
- Clock Hi/Lo levels in range 0V to ~ 25V, programmable on BEB
- 4 channels per chip, 2 chips per CCD
- CCD bias level buffers in range up to ~ 30V
- ATMEL BCD-SOI process. HV to 45V
- Status:
  - 1st submission tested & fully functional
  - Some pulse shape “wrinkles” (fully understood in simulation)
  - 2nd submission Fall '08

Additional FEB functionality
- Temp sensing & other usual monitoring
- Raft heaters
  - Part of focal plane thermal control loop

Back End Electronics

- 6x Back End Boards (BEBs)
- 24 channels ea, 18 bit 1 MHz ADCs (COTS)
- Temp sensor processing
- Programmable bias & clock levels for FEBs
- Sensor heater control
- Misc slow controls

Raft Control Module
- FPGA/Xilinx based programmable “Readout State Machine”
- Collects all ADC data (1 MHz)
- All control loops stored locally
- Responds to high level commands from Timing & Control Module (TCM)
- All Rafts in fully synchronous operation
- “Rocket i/o” data output to drive data fiber to DAQ (~1.6 Gb/s)
- Power PC for non-time critical operations

Data Volume
- Per image: 3.2 Gpixels ➔ ~ 7 GB
- Per minute: 4 images ➔ ~28 GB
- Per night: ~ 600 min ➔ ~ 16 TB
- Per year: ➔ ~ 5 PB
- All fibers received by “Science Data System” – (SLAC)
- Public data set

Additional Electronics Issues

Thermal management
- Board level: R_t ~ 20°C/W across 2 oz copper plane
- Crate level: R_t < ~ 0.5C/W

- Outgassing materials may condense on sensor surface
  - ~ 2 m² of pcb materials in cryostat
- Polyimide pcb construction (if necessary)
- Parylene (vapor deposition) or similar coatings
- Electronics separated from focal plane by molecular barriers (tortuous paths) and separate vacuum pumping
- All-in-cryostat materials tested / certified in test “Materials Test Facility” @ SLAC
- Optical loss measurement over LSST pass band & residual gas analyzer (RGA)
Comparison of LSST with existing or in-development cameras

Telescope and site: Cerro Pachon, Chile
TUESDAY 16 SEPTEMBER 2008

PLENARY SESSION 3
FPGAs in 2008 and beyond
Peter ALFKE, University of Heidelberg, Germany
presented by Volker LINDENSTRUTH
alfke@sbcglobal.net  ti@kip.uni-heidelberg.de
including slides from Ivo BOLSENS

**Agenda**
- The FPGA Trends
- The Triple Play Opportunity
- The Platform Approach
- V5 News
- Conclusions

**Twenty Years of Evolution**
- 1988: XC3090
- 2008: XC5VLX330T
- 1000 times the number of LUTs
- 2000 times the number of configuration bits = complexity
- 20 times the speed
- 500 times cheaper per function, not counting inflation

Moore’s Law has been good to all of us!

**FPGA Status**
- More Logic Packing
- 6-LUT architecture
- Faster Time To Market
- Cross Platform Compatibility in T devices
- New PCI Express
- Integrated rel. st., st. End-pi.
- Power & Performance
- Low power 100Mbps to 3.2Gbps GTP
  150Mbps to 6.5Gbps GTX
- Greater System integration
- PowerPC 440 with crossbar and APU
- Integrated Reliability
- System Monitor
- Integrated x1, x4, x8 End-pi.
- PowerPC 440
- Crossbar
- DMA
- SPLB1
- SPLB0
- MCI
- MPLB
- DCR
- Control
- APU
- CPM
- PowerPC 440

**FPGA Capacity Trends**

**FPGA Performance Trends**

**McKenzie Lecture 2007**
The IO Bandwidth

Agenda
- The FPGA Trends
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- Conclusions

The Triple Play Opportunity
- Global Internet traffic will reach 44bn gigabytes per month in 2012, compared to less than 7bn in 2007
- Video goes from 22% of consumer traffic in 2007 to 90% in 2012
- Mobile data traffic will roughly double each year from 2008-2012

Backend: focus on reducing power consumption to reduce operating expense

Consumer Internet Traffic Analysis 2007-2012

All Video: 49% of IP traffic
Fastest growth: Video to TV
Video Comm will be driven beyond 2012
P2P is large portion of IP traffic: 33%

Source: Cisco Visual Networking Index – Forecast and Methodology 2007-2012
Triple Play: Key Technologies

1. Digital Signal Processing
   - Transforming data
2. Packet Processing
   - Transporting data
3. Tera Computing
   - Analyzing data

Wired Networking Trends

- The line rate is what drives the processing and input/output challenge on each line card.
- The challenge is growing in step with Internet traffic growth.

Trend Towards Packetized Network-on-Board

Packets sent over physical serial link

Examples: PCI-Express (local interconnect), QPI (processor-memory), MIPI (mobile peripherals)

Wireless Networking Trends

- Longer-term trends:
  - Multi-mode radio and cognitive radio (increasing adaptability)
  - Mobility as central feature of Internet (increasing demands)

Agenda

- The FPGA Trends
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Bridging the Gap

The opportunities

- Systems and Applications
- Platform Design Methods and Software
- Circuits and Architectures

The full power of silicon
Platform-based Methodology

- Use of high level language:
  - Describe low-level relationships between sub-system components
  - Program processor-based components
  - Program some logic-based components
  - APIs hide all HW components
  - APIs hide external interface detail
  - Debugging in Soft form

- Hides underlying platform detail:
  - ISE and EDK tools
  - OS device drivers
  - Board settings

Design Methodology Roadmap

- User interface
- Programming language and development environment
- Back end technology

High Performance Compute Platform

- Peer Processing
- Co-Processing

Heterogeneous Multi-Processor

- 34GB/Sec
- 32GB/Sec
- 1066MHz Front Side Buses
- Four Memory Channels
- "Clarksboro" 7300 MCH

The Software Solution

- C/C++/FORTRAN Source
- Dynamic library call
- High-performance interconnect

Abstraction API

- Message Passing Interface (MPI)
- Communication in heterogeneous systems
- Processor-to-Processor
- Processor-to-Hardware Engine
- Hardware Engine-to-Hardware Engine
- Heterogeneous API in C & HDL
  - Node Discovery (ID)
  - Node Programming (exe and .bit)
  - Data Send & Receive
  - Software - Hardware

- Abstract and isolate hardware changes
  - Processors: parallel
  - Allows code reuse
  - Improves system scalability
Combining Xilinx FPGA Technologies with Software and Hardware to help the "Domain Expert"

**Measure It and Fix It**
The Engineering Innovation Process

- Design
- Prototype
- Deploy

- LEGO Mindstorms NXT
  "the smartest, coolest toy all the year"
  200's thousands of students

- CERN Large Hadron Collider
  "the most powerful instrument on earth"
  Engineering Team

**Agenda**
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- Conclusions

**Virtex-5 Common Features**
- 36Kb Dual-Port Block RAM / FIFO with ECC
- SelectIO with IDELAY/ODELAY and SerDes
- 10/100/1000 Mbps Ethernet MAC
- 550 MHz Clock Management
- 30% Higher Performance
- Higher Bandwidth

**Virtex-5 FXT Additional Capabilities**
- One or two PPC440 hard Microprocessor cores faster and more efficient than PPC405, super-scalar, larger caches, deeper instruction pipeline, integrated crossbar switch saves thousands of slices
- GTX High-performance Transceivers optimized for performance and low power and pc-board signal integrity for an "open eye"

- 5 family members, 3 in volume production by Sept.08

**More Than Just a PPC440...**
- Four built-in DMA channels provide high speed access to memory or I/O
- Separate memory and I/O buses greatly improve system performance
- External masters can access memory or I/O through the crossbar

**PPC440+128-bit FPU via APU**
- Soft co-processor module, free-of-charge accessible by the 440 processor instruction pipeline
- Single- and double-precision IEEE-754 compliant
- Speed-up 6 to 30 times, 200 MFLOPS sustained
GTX Multi-Gigabit Transceiver

- 8 to 24 transceivers per device (40 and 48 in TX subfamily)
- Supporting data rates from 150 Mbps to 6.5 Gbps
- Power dissipation less than 250 mW per channel
- Programmable Tx pre-emphasis and Rx equalization

6.5 Gb/s Transmit Eye Opening

http://www.xilinx.com/support/documentation/virtex-5.htm#19312

New Additions to the Family

- XC5VTX150T and 'TX240T
- Like 'FX130T and 'FX200T minus the PPC microprocessor, but with twice the number of GTX transceivers
- 40 and 48 GTXs respectively
- Availability: ES 4Q08, Production 1Q09

When you need lots of fast transceivers

Conclusions

- FPGA the programmable platform for
  - Transforming, transporting and computing digital data
- A trend towards specialized HW and SW to support programmable system solutions
- A strategy of working with Academics to enable exploration of new system applications & research
- Multi-gigabit transceivers are very popular
- Moore’s Law will give us much more logic and lower cost
  - Speed, power consumption, packaging pose a difficult challenge
- Users want and need to improve design productivity
  - The pace is becoming faster and more competitive.

Thank You
Optoelectronics, a global telecom carrier’s perspective

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Abstract

This paper summarises the current approaches to high speed optical transmission design. Cable & Wireless operates a large global optical transmission network, with the main purpose of serving the bandwidth market and of providing connectivity for its Internet Protocol data networks. In long haul spans, dense wavelength division multiplexed systems with aggregate capacities of 1 Tbit/s per fibre are deployed. The increase in bandwidth requirement is driving the need for more complex technologies that deliver a jump in system capacity. Emerging optoelectronic technologies are discussed, with particular focus on 40 Gb/s per wavelength transmission and optical wavelength switching.

I. INTRODUCTION

This paper is divided into five main sections. The Cable & Wireless optical network is briefly described to identify the requirement for high speed optical transmission systems. A brief review of optical fibre transmission impairments and dense wavelength division multiplexing (DWDM) is presented to assist the discussion of the merits of the approaches described. A statement of the status of 10 Gb/s transmission is followed by a discussion of two approaches to 40 Gb/s transmission. The final section examines aspects of the architectural development of optical switching.

There has been a surplus of transmission capacity in the early years of the current decade following the dot.com crash and telecom downturn. This was followed by a steady growth in the demand for bandwidth in the last 3 years, which is requiring upgrades to current systems and triggering the deployment of new technology.

II. CABLE & WIRELESS NETWORK

This section reviews the optical transmission network.

A. Company historical highlights

Cable & Wireless has its roots in the 1860s when undersea cables were first being deployed. A number of companies merged to become the Eastern Telegraph Company, which operated cables linking Britain internationally. In 1928 it was merged with Marconi Wireless to form Cable & Wireless and was nationalised in 1947. A new phase began with privatisation in 1981 and was quickly followed by the award of a license to operate in the UK to compete with British Telecommunications under the Mercury joint venture. Since 2005 it has been effecting consolidation in the UK market with the purchase of Energis and Thus (in progress). The company has network presence in around 150 countries and is the incumbent in several ex-UK territories.

B. Optical network services and global infrastructure

The network covers the UK, continental Europe, Asia and the United States of America (EAUS division) and multiple in-country operations (the International division). Principal services are Internet Protocol (IP) virtual private networks, wholesale voice, managed hosting, IP peering (public Internet) and global bandwidth. Together these require high capacity optical networks.

The infrastructure on which optical networks are built varies with geographical area: in the UK, fibre ducts are owned and multiple DWDM systems are deployed per duct; in Europe, the East coast of the US and Singapore, leased fibre are used to deploy single DWDM systems; US, Japan and Hong Kong use lease wavelengths and leased sub-wavelengths are used in the rest of the world. Cable & Wireless has significant interests through joint ventures in several subsea cable systems, the most significant being the Apollo transatlantic cable system [1].

I) Network architecture:

Two principal layers, the packet layer and transport layer, extend from the customer site to the core nodes. In the packet layer a range of service types are demarcated on the Multiservice Platform device, which are connected to core IP Multiprotocol Label Switched routers. The transport layer has devices known collectively as Multiservice Provisioning Platforms that aggregate traffic and perform time domain multiplexing (TDM). These are connected to core devices called optical cross connects, which perform high granularity multiplexing and grooming. The optical transmission network serves the packet and transport layers at several stages as the traffic is aggregated.

C. Deployed DWDM systems

A useful way to look at the growth in capacity of DWDM systems is to look at how the product of the transmission capacity and distance between electrical regenerators has increased over time. This product is used because the number of wavelengths that can be deployed on a system generally decreases with the distance due to the build up of optical noise. Figure 1 shows a plot of deployed Cable & Wireless DWDM systems. This shows that the capacity-distance product has been doubling approximately every 18 months.
1) Typical system characteristics:
Current typical system characteristics can be summarised as follows: scalability to 100 or more wavelengths; un-electrically regenerated reach up to 2000 km; flexibility; power consumption $\leq 2$ kW per 600mm by 600mm by 2.2 m rack with an expectation that a 1 Tb/s system should occupy around 2 racks.

Flexibility is important in three areas. Reconfigurability – this refers to the ability to change the wavelength point of entry to and exit from the DWDM system incorporated into devices known as Optical Add-Drop Multiplexers (OADM), which are described in section VI. Tunability – on the network side optical ports can be tuned to any of the typically 80 supported wavelengths. Such functionality minimises operational costs through reduced spares holding and supports rapid turn up of services. Pluggability – on the client side pluggable optics support a range of wavelengths and fibre types, which has the same benefits as tunability.

III. OPTICAL FIBRE TRANSMISSION AND DWDM REVIEW
Optical fibre transmission has developed rapidly over the last decade and recently many concepts from radio transmission have been borrowed and reinvented: however, transmission in single mode optical fibre is very different to radio transmission, since, the energy density leads to important nonlinear effects. This section reviews optical transmission and DWDM concepts, considering linear and then nonlinear impairments and DWDM principles.

A. Linear impairments

1) Attenuation
Attenuation in silica fibre [2] has a minimum due to intrinsic absorption between 800 nm and 1600 nm. In this region the loss profile is dominated by OH ion peaks and Raleigh scattering, which is proportional to the inverse fourth power of wavelength. The resulting profile is shown in figure 2. Attenuation minima are seen at 850 nm, used for intra-office connectivity, 1310 nm, used for inter-office connectivity and around 1550 nm, which is used for DWDM. The minimum attenuation in this region is around 0.18 dB/km. Raman and erbium-doped fibre amplifiers (EDFA) are used to mitigate attenuation. A typical gain of 25 dB is achieved with EDFA amplifiers leading to amplifier spacing of up to 100km. Raman amplifiers can be used to allow for wider amplifier spacing.

2) Chromatic dispersion (CD)
The International Telecommunications Union (ITU) standardises fibres and two types are commonly deployed: G.652 has the dispersion zero near 1310 nm and dispersion of $\sim 19$ ps/nm.km at 1550 nm; G.655 is a non-zero dispersion shifted type with dispersion zero just below 1500 nm and dispersion of $\sim 5$ ps/nm.km at 1550 nm. At 10 Gb/s the bit duration is 100 ps; $\sim 20$ ps of dispersion can be tolerated. Dispersion compensating fibre is widely used.

3) Polarisation mode dispersion (PMD)
Polarisation mode dispersion is due to polarisation states propagating at different speeds due to physical imperfections in fibre. Typically better than 0.2 ps/$\sqrt{\text{km}}$ but can be much worse. Generally it is not a problem for 10 Gb/s transmission but can be very significant for 40 Gb/s transmission speeds and above. Studies have been done on deployed fibre [4, 5]. Some correlation between year of manufacture and performance has been seen but no correlation between type of
installation—either buried or in Overhead Power Ground Wire (OPGW)—and performance has been seen, as shown in figure 4.

![Figure 4: Dispersion in buried and overhead (OPGW) cables][1]

**B. Nonlinear impairments**

Many types of nonlinear impairments are considered by DWDM system designers, three of which are: self phase modulation, cross phase modulation and four-wave mixing. All are strongly dependent on the optical power density in the fibre and this leads to a trade off between better optical signal-to-noise ratio (OSNR) with increased transmit power and increased intersymbol interference through nonlinear effects as power is increased. The typical per channel transmit power is 2 dBm.

**C. DWDM review**

The basis of DWDM is the ability to multiplex closely spaced optical wavelengths. This multiplexing is commonly done with Arrayed Waveguide Gratings, which are fabricated as planar silicon devices. Multiplexing is often done in two stages, although designers chose different values for the ratio between stages.

![Figure 5: Two stage optical multiplexing scheme.][2]

The wavelength spacing has been defined by the ITU in standard G.694.1. Channels are referenced to a frequency of 193.1 GHz. The commonly used C band and EDFAs yield in excess of 80 wavelengths with 50 GHz spacing.

![Figure 6: Transmission bandwidth and amplifier gain windows.][3]

### IV. 10 GB/s TRANSMISSION

**A. Current industry standard**

The 10 Gb/s transmission speed has become the industry standard. A typical transmitter uses a continuous wave laser, external modulator, which is an electroabsorption positive-intrinsic-positive (pin) or Mach-Zehnder lithium niobate (LiNbO3) device. An On/Off Keyed (OOK) Nonreturn-to-Zero (NRZ) format is almost universally used. Receivers are usually avalanche photodiodes. For flexibility full C band tunability with 50 GHz increments on the DWDM side and pluggable client side for variable reach and wavelength (850/1310/1550 nm) is common. A typical power consumption is 35W per transceiver with client and network side optics.

Forward Error Correction (FEC) [6] has been standardised in ITU recommendations G.975 and G.709, specifying a Reed-Solomon scheme with 7% overhead. Both standards-based and proprietary schemes have been adopted by system vendors and this is crucial in extending the reach, which in many systems is more than 2000km.

**B. Alternative approaches**

A number of alternative approaches are worth noting.

1) **Full electronic dispersion compensation**

This is achieved through digital signal processing and can fully compensate for the dispersion over the full length of the optical path [7], which can save up to 15% on transit delay. The disadvantage is that such an optical network is closed since it cannot accept wavelengths without this technology built in. While not widely deployed at 10 Gb/s this technique is likely to be important for 100 Gb/s solutions.

2) **Return-to-Zero (RZ) and Solitons**

Pulses shorter than the full bit period can have beneficial transmission properties; the added complexity, however, has prevented wide scale deployment. These techniques may also feature in high speed solutions beyond 10 Gb/s.

3) **Advanced amps (Raman)**

---

[1]: #fig:dispersion
[2]: #fig:twostage
[3]: #fig:transmissionbw
Raman amplifiers offer two distinct advantages in increasing the viable distance of a single span, and widening the amplification bandwidth. This has been used by Xtera to increase the 10 Gb/s wavelength count to 240 in a single system.

4) Photonic integrated circuits

Photonic Integrated Circuits (PIC) on indium phosphide (InP) chips have found commercial success. Infinera has developed a PIC with 10×10 Gb/s transmitters or receivers and multiplexers on a chip: cheaper, more frequent, regeneration avoids impairments by reducing regeneration spacing and also enables fast service turn up once the PIC has been installed.

V. 40 GB/s TRANSMISSION AND BEYOND

The deployment of 40 Gb/s has been delayed several years by the economic climate that has affected severely telecommunications and Internet-based technology development. Transmission at 40 Gb/s is, however, now ready for deployment and is being adopted in significant quantities.

A. 40 Gb/s clients

High-end IP routers are the main potential users of 40 Gb/s. Tb/s routers operating at 10 Gb/s would require many parallel links. This causes problems of load sharing, large routing tables, management complexity and power consumption. The solution to this would be to use 40 Gb/s and then later 100 Gb/s.

Modules that perform a 4:1 TDM combiner function to 40 Gb/s are proving to be a strong driver for 40 Gb/s in optical networks since the spectral efficiency is increased compared to discrete 10 Gb/s modules. This is in contrast to the situation at 10 Gb/s where the deployment of 4:1 combiners working at 10 Gb/s network side with 2.5 Gb/s clients was not widely deployed until several years after the first 10 Gb/s client was ready.

B. System requirements

Any candidate 40 Gb/s solution should be deployable with existing DWDM systems to maximise the investment. Link engineering rules–amplifier gain and spacing, attenuation budgets, chromatic and polarisation mode dispersion values and 50 GHz filtering–will be the same and the 40 Gb/s stream must be able to coexist with deployed 10 Gb/s. 40 Gb/s compared to 10 Gb/s has a CD tolerance 16 times worse and PMD tolerance 4 times worse for the same modulation format.

C. Modulation formats

There are four ways to modulate the optical field in an optical fibre: intensity, frequency, phase and polarisation [7]. These are illustrated in figure 7. NRZ OOK used for 10 Gb/s. There are auxiliary modulation features that may be added. Frequency and polarisation modulation have had little focus due to inherent difficulties, whereas phase modulation has produced a rich set of solutions that continue to be investigated. Some important formats are represented in figure 8. Two particular solutions will be discussed in more detail to illustrate the component complexities and relative transmission advantages: duo-binary (DB), an intensity modulation format with phase as an auxiliary modulation, and differential phase shift keying (DPSK), a phase modulation format.

D. Duo-binary (DB)

Duo-binary belongs to a group of correlative coding formats in which there is a correlation between the data and the phase of the transmitted signal. Figure 9 shows the data, amplitude and phase relationship. Whenever there is an odd number of 0-bit levels between 1-bit pulses then a change of phase occurs. This has advantages both in the time domain and frequency domain that lessens the effect of chromatic dispersion. In the time domain, if two 1-bit pulses spread into each other they will interfere destructively thus preserving the low 0-bit level in between. In the frequency domain the spectrum is narrowed due to the smoother +1 0 -1 transitions between consecutive 1-bit pulses. Both these behaviours improve chromatic dispersion tolerance.
1) Duo-binary optoelectronic components

The optoelectronic block diagram is shown in figure 10. NRZ data is precoded such that there is a level change for every 0-bit in the original data. The encoder is a severe low pass filter, which feeds a Mach-Zehnder modulator. Both the precoder and encoder are additional electronic components needed compared to NRZ OOK. The receiver is the same direct detection method used for OOK.

E. Differential phase shift keying (DPSK)

In DPSK the NRZ data is converted to phase encoding such that a 1-bit level leads to a $\pi$ phase change. The data and phase relationship is shown in figure 11.

1) DPSK optoelectronic components

The optoelectronic block diagram is shown in figure 12. The same encoder as for DB is used but there is no need for the encoder. The receiver design is significantly more complex. Tunable dispersion compensation is required as the spectrum is broader resulting in lower chromatic dispersion tolerance. A delay and add MZI feeds a balanced receiver to recover the NRZ data. These three stages represent additional high-cost optical components compared with NRZ OOK and DB modulation.

F. Comparison of modulation formats

Table 1 compares the qualities of DB and DPSK formats discussed above. While DPSK is more expensive, its reach performance combined with lowering costs as economies of scale appear should promote wide deployment.

<table>
<thead>
<tr>
<th></th>
<th>DB</th>
<th>DPSK</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSNR</td>
<td>--</td>
<td>++</td>
</tr>
<tr>
<td>CD tolerance</td>
<td>++</td>
<td>+</td>
</tr>
<tr>
<td>PMD tolerance</td>
<td>Similar</td>
<td>+</td>
</tr>
<tr>
<td>Nonlinearity</td>
<td>Similar</td>
<td>+</td>
</tr>
<tr>
<td>Cost and complexity</td>
<td>Similar</td>
<td>--</td>
</tr>
<tr>
<td>Reach</td>
<td>1000 km</td>
<td>1600 km</td>
</tr>
</tbody>
</table>

G. 100 Gb/s

There is a clear driver for Ethernet connectivity at around 100 Gb/s. Standardisation is in progress—but not completed—and many research papers report results at around this bit rate. Compatibility with current deployed systems is preferred and a field trial of mixed speeds has been undertaken [9]. An example of the approach is shown in figure 13 [10]. The modulation format shown here is polarisation-multiplexed quadrature phase shift keying (PM-QPSK). It is immediately evident that the complexity has increased substantially and the inclusion of digital signal processing (DSP) should be noted.
VI. OPTICAL SWITCHING

DWDM systems have evolved from basic point-to-point formats to include fixed, and then reconfigurable, optical add-drop multiplexing (OADM) functionality. The drivers for this development are to remove costly optical-electrical-optical (OEO) regeneration and to increase speed of provisioning and flexibility. Extending this to a fully functioning optical wavelength switching node [11] would reduce operational and capital expenditure and increase flexibility with all the accompanying planning, provisioning, resiliency and redeployment benefits.

1) Optical add-drop Multiplexer (OADM)

OADM nodes were introduced first incorporating fixed filters that allowed access to a part of the band. Figure 14 shows a schematic for the functionality; only one of the two directions is shown for simplicity.

![Figure 14: OADM block diagram. A single direction is shown for simplicity.](image)

2) ROADM, 1st Generation

Reconfigurability has been added to OADM with the addition of a splitter and wavelength blocker as shown in figure 15. The purpose of the blocker is to remove the wavelengths that are dropped so that wavelengths can be added without interference from the express path. Blocker technology is relatively mature, micro electromechanical systems (MEMS), liquid crystal and planar lightwave circuits (PLC) being the principal solutions. Wavelength equalisation is often incorporated in the blocker.

![Figure 15: ROADM with blocker](image)

3) Blocker scalability problem

ROADMs using blockers run into a problem as the number of directions (degrees) increase because the number of blockers required scales as n^2-n and this makes their use impractical beyond 3 degrees. Figure 16 illustrates the problem.

![Figure 16: Three degree node illustrating requirement of six blockers.](image)

4) Wavelength Selective Switch (WSS) ROADM, 2nd Generation

A solution to this blocker scalability problem is to use a wavelength selective switch (WSS) as shown in figure 17. The number of WSS devices scales linearly with the number of degrees. A WSS can switch any of the served wavelengths from an ingress port to any of its egress ports. Typical port counts are 1 ingress and 9 egress (1x9). WSS technology is relatively immature. MEMS are widely used but also liquid crystal and piezoelectric beam steering solutions have been developed. 100 GHz spaced optical grid with 40 wavelengths is typical but 50 GHz spaced grids are expected to come to market soon.

![Figure 17: ROADM using WSS devices. A wavelength can be switched from the ingress port to any of the egress ports.](image)

The combination of 50 GHz WSS technology and a 40 Gb/s transmission rate is promising to extend significantly the capacity and flexibility of optical networks in the next three years.
VII. SUMMARY

The Cable & Wireless network has been used to illustrate the role of optical networks and to make the case that there is a driver for higher bandwidth and more flexible optical transmission systems. 10 Gb/s DWDM system design is mature and 40 Gb/s is ready for deployment. Two 40 Gb/s design solutions have been described and the merits compared. The development of wavelength selective switches is enabling flexible reconfigurable networks. The prospect of being able to deploy 40 Gb/s DWDM systems with multi-degree ROADMs over the next three years is an exciting one for national and global carriers.

VIII. ACKNOWLEDGMENTS

The author has benefited from the efforts of several colleagues in Cable & Wireless who have helped gather information for the section on the company’s network and who have offered comments on the content of the paper. Thanks also go to Dr Marco Cavallari of Stratalight Communications for many useful discussions and help sourcing material for the 40 Gb/s section. Any remaining errors in this paper are the responsibility of the author.

IX. REFERENCES

[2] A useful fibre attenuation summary can be found at: http://www.electronics.dit.ie/staff/tfreir/optical_1/Unit_1.7.pdf
TUESDAY 16 SEPTEMBER 2008
PARALLEL SESSION A1
ASICs
A Monolithic Active Pixel Sensor for a “Tera-Pixel” ECAL at the ILC


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Abstract

The leading proposed technology for electromagnetic calorimeters for ILC detectors is a highly granular silicon-tungsten calorimeter. We have developed an active pixel sensor for such a calorimeter, which would have extremely fine granularity, allowing binary pixel readout. A first generation chip (TPAC1.0) has been fabricated, and this contains a 168x168 pixel array, consisting of 50x50 micron pixels. Each pixel has an integrated charge pre-amplifier and comparator. TPAC1.0 has been manufactured in a 0.18 micron CMOS “INMAPS” process which includes a deep p-well implant. We present recent results of the performance of the TPAC1.0 sensor together with comparison to device-level simulations.

I. INTRODUCTION

The ILC physics program [1],[2] requires detectors with unprecedented jet energy resolution. To achieve this goal, the detectors will need highly granular calorimeters and, for the electromagnetic calorimeter, the use of a silicon-tungsten calorimeter has been favoured. The granularity and readout requirements of such a calorimeter are closely interrelated.

Detailed simulations [3],[4] show that a pixel size of 50x50 microns results in most pixels only being hit once per event. Thus we can employ a simple binary readout using a comparator instead of an analogue measurement.

CMOS monolithic active pixel sensors (MAPS) have been previously demonstrated as suitable devices for high energy physics applications [5],[6] and so this sensor concept offers the opportunity to implement the necessary fine pixel size and integrated readout and timing electronics in a single silicon die.

The sensor specification is therefore for small pixels that are able to detect an incident minimum ionising particle (MIP); the timestamp and location of such hit events are then stored in local memories for readout in between bunch trains at the ILC. The location of hits in multiple layers of these sensors allows for reconstruction of particle showers thus implementing a digital measure of calorimetry.

The sensor requirements and intended operating mode require some in-pixel analogue signal processing, threshold discrimination and control logic, thus many transistors of both nmos and pmos types: As the charge-collecting junction is formed by an n-well and the p-doped substrate, the n-wells which form the substrate of PMOS transistors would present a significant reduction in the charge-collection efficiency of the pixel. In order to avoid these charge losses, an advanced 0.18 micron CMOS process has been developed, called INMAPS, which features an additional deep p-well implant to shield unrelated n-wells from collecting charge.

A first prototype, the “Tera-Pixel-Active-Calorimeter” sensor, or TPAC1.0, is shown in Figure 1: The device has been well characterised in the past months, with many results included in this document. The results of this recent testing have been used to select a preferred pixel architecture for the TPAC1.1 sensor which is currently in manufacture.

II. ELECTRONIC CIRCUITS

A. Sensor Architecture

The TPAC1.0 sensor comprises 28,224 pixels, row control logic, on-chip SRAM memory banks and I/O circuitry in a 9.7x10.5mm² die. The sensor collects the charge deposited by an incident particle in pixels arranged on a 50 micron pitch. This signal is compared with a global threshold and if a particle is detected, the time-code and location of the event are recorded in memories for readout at a later time. The physics of the target application is such that real incident particles are extremely rare; hence artificial hits caused by electronic noise will dominate the volume of hits that are stored and read out.
Four different pixel designs are implemented for evaluation, which fall into two distinct architectures. A common control and readout architecture serves all pixel varieties, allowing the sensor to be operated as a whole or as sub-regions. Pixels may be individually masked, allowing any permutation of single pixels to be operated and evaluated.

B. Pixel Architectures

1) The preShape pixel

The preShape pixel is based on a conventional analog front end for a charge-collecting detector. The four diodes are connected (in parallel) to a charge preamplifier, which generates a voltage step output in proportion to the collected charge. A CR-RC shaper circuit generates a pulse output in proportion to the input signal with further circuit gain to yield 94uV/e- with respect to total input charge. This signal, along with a local common-mode reference form a pseudo-differential input to the two-stage comparator. The shaper circuit returns to a stable state, depending on the signal size, and is then able to respond to another input signal.

Figure 2: preShape pixel circuit diagram.

The in-pixel comparator has two parts: the first takes two differential signals, and produces a real-time differential discrimination result, with some small analog signal gain. The second comparator generates the full-swing discriminator output, and applies offset trim adjustment with 4-bit resolution. The output of the comparator is enabled with a 1-bit mask input which can be used to prevent the pixel from generating hit events.

Pixels generate a fixed length pulse using a monostable circuit, which is connected to row control logic outside the pixel. The length of the output “hit” pulse is independent of the signal size.

To achieve high circuit gain in the preamplifier, a small value of feedback capacitance was required, which was made using two larger capacitors in series to comply with manufacturing design rules. Two different simulation tools were used to evaluate the optimum orientation of the series feedback capacitors, but the two tools selected different topologies for highest gain. Two capacitor orientations are therefore implemented on the TPAC1.0 sensor as subtle variants of the preShape pixel.

2) PreSample pixel

The preSample pixel is based on a conventional MAPS sensor [7], with in-pixel analog storage of a reference level. Charge integrates on the four collecting diodes, causing a small voltage step proportional to the collected charge and the node capacitance. A charge preamplifier provides gain to generate a larger voltage step which, along with a local sample of the reset level, forms a pseudo-differential input to the two-stage comparator. The voltage step is generated in proportion to the input signal to yield 440uV/e- with respect to total input charge. The charge amplifier and reference sample must be reset after a hit event before the pixel can detect another hit, which is undertaken by the in-pixel logic.

Figure 3: preSample pixel circuit diagram.

The in-pixel comparator stage is common to all pixel architectures, but the preSample pixel includes an additional monostable circuit to generate the self-reset signals that are necessary to prepare the amplifier and reference sample for another hit event.

Similar to the preShape pixel, a small capacitance in the preamplifier feedback is made with two capacitors in series. This gives rise to two subtle variants of the preSample pixel, again based on results from different simulator tools.

C. Logic Columns

The row logic is responsible for monitoring the individual hit outputs from a row of 42 pixels and writing details of any hit events to local memory. An external clock defines the timing with which hit signals are sampled. The hit signal from a pixel is asynchronous, but will have a fixed pulse-width defined by the in-pixel monostable bias setting. This pulse length is set to be O(10%) greater than the hit sampling period, which is generally matched to the bunch crossing rate of the target application. This regimen ensures that an asynchronous hit will always be sampled by the synchronous logic, with a small probability that it will be sampled twice: This is an acceptable data overhead that allows for a reasonable spread in the length of the monostable pulses, with a minimal risk that an entire hit pulse occurs between sampling and hits are therefore lost. The sampling of hits uses a “ping-pong” circuit architecture to ensure there is no dead time between samples.

The row control logic has 19 SRAM registers available for storage of hit data. A memory controller is implemented to organise the use of these registers, such that registers are not overwritten once used, and only those with valid data participate in readout.

The row control logic may be operated in “override” mode, whereby the pixel “hit” inputs are ignored and the value of the hit pattern in each bank is always stored. This operating mode fills the memories in less than 3 complete cycles of the standard control sequence, and so is only intended as a test feature.

The 19 SRAM registers occupy the full 50 micron row pitch. The hit pattern and corresponding multiplex address are stored in the first 9 bits of a register, with a further 13 bits
used to store the global timestamp code, which is incremented each time hit signals are sampled. The cross-coupled inverter structure of a SRAM cell ensures the data will be held indefinitely provided the cell is powered, so there is no requirement to refresh the data for a maximum hold time after which data is corrupted.

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The full TPAC1.0 sensor comprises 4 columns of row logic, each with 168 rows, hence there are 12,768 SRAM registers of 22 bits each in total.

The row control logic and the SRAM register bank occupy a 250 micron wide region adjacent to the 42 pixels. The logic and SRAM are insensitive to incident particles; therefore this structure has an inherent 11% dead area.

III. INMAPS PROCESS TECHNOLOGY

To ensure the success of this design it was essential to develop an additional processing step in a commercially available standard CMOS technology. The pixel designs implement many transistors inside the pixel that, in a standard CMOS process, would introduce a significant reduction in charge collection efficiency.

An incident charged particle deposits electron-hole pairs along its trajectory through the epitaxial silicon layer. This charge diffuses within the region defined by the barrier formed between the epitaxial layer and the bulk silicon. The lifetime of such carriers is long, so they are most likely to reach a collecting n-well diode at a positive potential. Carriers that pass close to a diode are collected and form the signal charge input to the pixel circuits. A charge-collection efficiency reduction occurs when PMOS transistors are also present in the pixel, since these sit also in an n-well that is held at a positive potential. Carriers that pass close to these unrelated n-wells will be lost as they are absorbed by the power supply.

In order to protect the diffusing charge from n-wells of pixel circuits, a high energy “deep p-well” implant is added to the wafer processing. The diffusing charge sees this small change in doping concentrations as a potential barrier and is reflected away from the proximity of the n-well, as illustrated in Figure 5: This implant is essential to the charge-collection efficiency of the pixel, and the success of the sensor. Further information may be found in [8].

A. Pixel Layout

The layout for the two pixel architectures is shown in Figure 6: up to the first metal layer, with the key circuit blocks illustrated. The 50micron pixel boundary is marked with a dotted line, although some circuit blocks extend beyond this boundary the pixels tile correctly to form an array. The preShape and preSample pixels contain 160 and 189 transistors respectively and approximately 30 capacitors. Both pixel layouts have the four diodes in the same location, near the corners for optimum charge collection.

The deep p-well layer is added to the pixel layouts, illustrated in Figure 7: The deep p-well is placed as a symmetrical cross structure, leaving only the four collecting diodes exposed to the charge diffusing in the substrate. The deep p-well geometry is common to all pixel varieties.

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B. Device Simulation

The behaviour of diffusing charge in the substrate was modelled in ISE-TCAD tools, using the GDS data of the submitted design. Charge is “deposited” at a number of points in the pixel: The charge collected at each pixel diode, and the time-profile of this collection is simulated. Sample results from these simulations are shown in Figure 8: Two profiles through the pixel are shown, profile F passes through the very centre of the pixel, while profile B passes close to two diodes.

Figure 8: Simulated charge collection for particle hits in two linear profiles through a pixel (as illustrated).

The simulation results show clearly the benefits brought by the deep p-well, and the poor performance we might expect without deep p-well. Profile F that passes through the centre of the pixel collects very little charge without deep p-well, since it is mostly absorbed by the pixel electronics before it can reach a diode; the protection of the deep p-well layer is clearly demonstrated since the charge is allowed to reach the diodes. Profile B passing near a diode shows similar performance regardless of deep p-well, but again, charge deposited near pixel electronics can only reach the diode when the deep p-well is implemented.

In order to fully evaluate the performance of the new deep p-well implant the TPAC1.0 sensor was manufactured both with and without the additional processing step.

IV. SENSOR TESTING

Sensor test results are organised as those for the separate additional test pixels, single pixels in the main array and the performance of the pixel array as a whole. Test results for the arrays are presented for the preShape pixel variant only, since this was seen to perform more favourably than the preSample variant. The two variants of the preShape pixel are identified as quadrants 0 and 1. The test pixels implemented were only of the preSample variant; hence the details of those pixel circuits are an important part of this script.

A. PreSample Test Pixels

Several test pixels are included at the edge of the main pixel array for detailed testing. These pixels are based on the preSample pixel architecture, and include additional analog buffers to monitor internal analog signals in the pixel circuit. The signal pulse and the reset sample are available for two adjacent pixels, and the internal differential comparator output is available from one test pixel. A third pixel allows evaluation of other in-pixel circuits.

Test pixels were evaluated with a 1064nm laser, pulsed at 25Hz in bursts of 4ns. The laser is mounted in a microscope with adjustable shutters to realise a 2x2um² area of illumination at the focal point. The sensor is illuminated from the rear, to avoid signal attenuation due to the many levels of metal routing in the pixel; the absorption length of silicon at this wavelength is long, so attenuation in this method is negligible. The focus of the laser was adjusted to target the epitaxial layer, accounting for the refraction of the laser light at the interface between air and the silicon. The sensor is mounted on an X-Y stage which can be remotely positioned to 1micron accuracy. Thus it is possible to deposit point-like charge at any location in the test pixel, and observe the analog response of the pixel on an oscilloscope.

Figure 9: Amplitude response of preSample test pixel to laser stimulus: horizontal line profile intersecting two diodes.

The test pixel and the laser operate independently, with no synchronisation, but there is a laser control pulse that can be used to trigger an oscilloscope. The asynchronous pixel reset occasionally occurs during a laser event, but histogramming features on the oscilloscope eliminate susceptibility to this rare event. Signal magnitude and time-delay parameters can be recorded for each position, in an automated sequence. A typical amplitude response for a profile passing through two diodes in the test pixel is shown in Figure 9: The diodes are clearly identified in the scan, at the expected 34 micron separation.

Charge collection time is measured on the oscilloscope using the delay from the laser control pulse and a fixed 30mV threshold on the signal output from the target test pixel. This is compared with simulated results in Figure 10: where the time taken to collect 90% of the total charge is recorded. The profile between two diodes is presented on the same axis for simulation and measured results. There is a fixed-time delay from the laser control pulse to the emission of the laser pulse, but there is good correlation in the charge collection profile
between the two diodes, from which we can attain a reasonable degree of confidence in the device simulations. Automated scans of all positions in and around the test pixels are underway to further compare the device simulations with real behaviour of charge diffusing in the substrate, in sensors both with and without the deep p-well processing.

B. Single preShape Pixel in Array

Evaluation of a single pixel in the main array is achieved by setting the mask bit in every other pixel, thus leaving only a single pixel operational. Analog information is no longer available, since the pixel readout is binary, and stored in local SRAM. The method of evaluation of such pixels is therefore by threshold scan: The number of hits reported by the sensor is recorded for a wide range of thresholds. The resulting profile (see Figure 11) can be used to determine the noise of the pixel, offset and signal response, by taking a number of bunch-trains for each threshold setting. The parameters of such runs can be adjusted for greater precision or faster scan time as required.

The example plot in Figure 11 shows two overlaid threshold scans; the blue response shows a single pixel with no stimulus, effectively showing the electronic circuit noise. For high thresholds, the noise is negligible, and no hits are recorded; for low thresholds the noise triggers the in-pixel comparator and hits are recorded; for very low thresholds, because the comparator is effectively edge-triggered, the comparator does not fire, hence the profile drops for small/negative thresholds. The total number of hits that may be recorded for a single pixel is 19, hence the profile of the pixel noise is capped at this level. The red response shows a typical profile with pixel stimulus, in this case a pulsed laser: The electronic noise generates a similar profile of hits, but the injected signal now generates additional hits for thresholds much higher than the electronic noise, up to the magnitude of the signal, beyond which there are again no further hits recorded. The signal magnitude may thus be estimated from the “roll-off” of this threshold scan. The accuracy of this technique is limited by the statistics of the threshold scan (which can take some considerable time) and the quality of the curve-fitting algorithm applied to the signal “roll-off” response.

An estimation of absolute position is possible using the threshold-scan technique: Rear illumination of the sensor offers no clues as to position, which may not be square to the x/y stage, but laser scans in the test pixels indicate that local maximum should be found scanning through the centre of pixels, or twin-peaks should be seen in scans. Such a scan of pixel centre axes is shown in Figure 12: which shows the response of three adjacent pixels in normalised units. The 50 micron pixel boundary can be easily deduced from these results. This technique is used near the corners of the sensor to establish the alignment of the sensor in the laser system, so that a correction factor can be calculated and applied to any X or Y movement request where comparisons are to be made.

A further comparison with simulation results can now be made, by testing the pixel response to charge deposited in all areas of the pixel. Figure 13: shows the same simulation data from Figure 8, but now with added results from laser induced signals, normalised to the maximum signal size. The
qualitative similarity between simulation and measurements is clear, indicating the predicted benefits of the deep p-well implant are true in the manufactured devices. Similarly, the results from the non-deep p-well sensor clearly show the poor performance we would have achieved if the deep p-well module had not been developed.

The pixel array was also exposed to a strong $^{55}\text{Fe}$ source for a number of days, during which time several pixels were unmasked and threshold scans performed. $^{55}\text{Fe}$ is a key calibration technique, since the emitted 5.9keV X-rays will result in a well defined charge deposit of 1600e- at a point, which will sometimes occur in the diode well where no charge can diffuse. Typical results are shown in Figure 14: The signal roll-off will occur at the peak signal, which is more easily found by taking a derivative, where the small peak (shown) corresponds to the peak $^{55}\text{Fe}$ signal. This technique is used to calibrate the pixel electronics and the “threshold units” relative scale that is generally used.

![Figure 14: Single pixel $^{55}\text{Fe}$ result: Standard threshold scan (with/without source) shown on the left; Derivative is shown on the right, demonstrating $^{55}\text{Fe}$ peak.](image)

C. preShape Pixel Array Performance

Evaluation of the full array of preShape pixels begins by evaluating each individually for noise. Only a single pixel is unmasked in any row and a threshold scan performed. By systematically changing the mask for subsequent runs, a scan over all pixels of the sensor can be built up. The pedestal, or x axis offset from one pixel to the next is large and variable, which is illustrated in the histogram of Figure 15:(left), where the mean value of the noise histogram from all 14,112 preShape pixels is plotted for both pixel variants. This per-pixel data is used to calculate the per-pixel trim adjustment. The trim adjustment is loaded into the in-pixel configuration registers and the per-pixel scan repeated. The correct operation of the trim adjustment can be seen in the histogram in Figure 15:(right).

![Figure 15: Histogram of per-pixel threshold scan mean values for quad 0 (solid) and quad 1 (dashed) preShape array pixels. Left shows before trimming, right shows after trimming.](image)

An evaluation of pixel gain uniformity is possible using the laser source, now that absolute position and pixel pedestals are known. Approximately 250 pixels are hit with the laser in an equivalent position, and their signal magnitude evaluated by the threshold-scan/fit technique. The pedestal-adjusted gain uniformity is shown in Figure 16: for both variants of the preShape pixel. The pixel gain is uniform to 12%, and quadrant 1 shows preferable mean gain and signal-to-noise performance over quadrant 0.

![Figure 16: preShape pixel gain uniformity: histograms shown for quad 0 (solid) and quad 1 (dashed).](image)

V. FUTURE OUTLOOK

Full characterisation of the TPAC1.0 sensor will conclude in the coming months, involving automated laser scans over test pixel regions, and characterisation of many pixels in the main arrays. A stack of 4 sensors will also be used to look for cosmic rays over a long period.

A new sensor, TPAC1.1 has been designed and is due back from manufacture at the end of September 2008. The new sensor selects a single pixel variant, (preShape quadrant 1) and is thus a homogenous pixel array. The in-pixel trim adjustment was upgraded from 4 bits to 6 bits to ensure pixels can be “aligned” to greater accuracy than the pixel noise. Test pixels of the preShape variant are included in TPAC1.1 in order to further learn more about the internal workings of these pixels. Beyond these and some minor changes, the sensor is very similar to TPAC1.0, and as such is I/O, PCB and DAQ compatible. This will enable immediate verification of the revised sensor with a known working test system. The full portfolio of characterisation summarised in this script will be repeated for the new sensors. The homogenous pixel array make this sensor ideal for beam tests, which are anticipated in early 2009: Four sensors will be mounted in a stack, with a number of tungsten plates and scintillators to prove the sensors in a demonstration ECAL environment with particle showers.
VI. CONCLUSIONS

We have successfully designed, built and demonstrated operation of a highly complex pixellated sensor for an ECAL at the ILC. The pixels have been shown to respond to input stimulus from $^{55}$Fe and infrared laser, which studies have shown to correspond to device simulations.

We have successfully developed, implemented and verified a deep p-well implant on a standard 0.18micron CMOS process, to improve the charge collection efficiency of a MAPS detector with in-pixel electronics. The inclusion of such a layer is seen to be essential to the success of the design.

A revised sensor is imminently due back from fabrication, where a single pixel architecture was selected from the characterisation work presented herein. Testing of this new sensor will begin immediately on its return, thanks to complete compatibility with existing test systems. The new sensor has a homogenous array of pixels, and so it well suited to the intended beam test in early 2009, where it is hoped to demonstrate ECAL operation in a real particle beam, using tungsten to generate showers in the 4 layers.

In the long term this collaboration hopes to build larger scale sensors from these pixels and their associated circuits to demonstrate digital calorimetry with a stack of multiple sensor/tungsten layers in a particle beam environment.

VII. REFERENCES

Development of the ATLAS FE-I4 pixel readout IC for b-layer Upgrade and Super-LHC

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Abstract

Motivated by the upcoming upgrade of the ATLAS hybrid pixel detector, a new Front-End (FE) IC is being developed in a 130nm technology to face the tightened requirements of the upgraded pixel system. The main design goals are the reduction of material and a decrease in power consumption combined with the capability to handle the higher hit rates that will result from the upgraded machine. New technology features like the higher integration density for digital circuits, better radiation tolerance and Triple-Well transistors are used for optimization and the implementation of new concepts. A description of the ongoing design work is given, focusing more on the analog part and peripheral design blocks.

I. ATLAS PIXEL UPGRADE SCHEDULE AND CONSEQUENCES ON FE-I4 SPECIFICATION

The development of the FE-I4 pixel chip is motivated by planned upgrades to the ATLAS [1] pixel detector [3]. While upgrade plans are evolving, two distinct upgrades are expected based on the collider luminosity projections. The first upgrade, known as b-layer upgrade, is a new inner layer mounted on the beam pipe at a smaller radius and for luminosity a factor of 2 or 3 higher than present detector specifications. The second upgrade, known as Super-LHC, is on a longer time scale and it consists in the complete replacement of the ATLAS tracking detectors [2], for a luminosity 10 times higher than specified for the present one. The FE-I4 chip is aimed at inner layer use for the first upgrade, and outer layer use for the second upgrade, which is a natural fit because the hit rates for these two cases are comparable. The total area to be covered in the outer layers of the Super-LHC upgrade is about 4 times the total area of the present detector, and so reduction of manufacturing cost is an important requirement for FE-I4.

With a potential smaller b-layer radius and a 2-3 times higher luminosity, the hit rate the FE-I4 will have to deal with will rise significantly. Simulations performed on the current FE-I3 architecture to study the influence of the increased hit rate, show that an unacceptable high number of relevant hits get lost because of pile up effects in the pixels and congestion in the double column data bus [5]. Hence a smaller pixel geometry of $50 \times 250 \mu m^2$ has been chosen to reduce the pixel cross section, having also a benefit on tracking resolution. In addition the digital pixel logic and the double column bus scheme have to be reorganized in a new architecture that is able to process the higher hit data volume. Serial links operating at 160MHz are needed for sending triggered hit data off-chip.

Driven by the need to reduce material and bump-bonding cost, the overall chip size will be increased close to the technology’s limits to approximately $20.0 \times 18.6 \text{mm}^2$. In addition, the higher integration density the new technology offers allows to go to smaller peripheral chip area sizes which increases the active fraction from 74% in FE-I3 to almost 90% in FE-I4. Since bump bonding costs scale with the number of parts that have to be handled during the bonding process, both the bigger chip size and the use of fewer chips per module lower the manufacturing cost.

Material reduction is also correlated to power consumption. To reduce the cable budget and at the same time limit the power losses in the cable, the current flowing through the supply lines has to be minimized. On that account 10µA current target for the analog readout chain has been defined per pixel. The same amount of current is dedicated to the digital pixel logic which is sufficient because with the new FE-I4 digital architecture concept the digital activity is much reduced (see section III.). Moreover different powering schemes like serial powering or divide-by-two DC/DC conversion are under consideration to improve efficiency with respect to the conventional parallel powering approach. A comparison between some of the specifications of FE-I3 and FE-I4 is given in table 1.

In the following sections the analog circuits that have been

| Table 1: Specification comparison between FE-I3 & FE-I4 target [3, 4] |
|-----------------|-----------------|-----------------|
|                  | FE-I3            | FE-I4            |
| Pixel Size      | $50 \times 400 \mu m^2$ | $50 \times 250 \mu m^2$ |
| Pixel Array     | $18 \times 100$  | $80 \times 336$  |
| Chip Size       | $7.6 \times 10.8 \text{mm}^2$ | $20.0 \times 18.6 \text{mm}^2$ |
| Active Fraction | 74%               | 89%              |
| Analog Current  | $16 \mu A$/pixel | $10 \mu A$/pixel |
| Digital Current | $10 \mu A$/pixel | $10 \mu A$/pixel |
| Analog Supply Voltage | 1.6V       | 1.5V             |
| Digital Supply Voltage | 2.0V       | 1.2V             |
| Data Rate       | 40Mb/s          | 160Mb/s          |
submitted in 2008 on a FE-I4 prototype and on additional test chips are described and a short introduction to the digital architecture is given.

II. ANALOG READOUT CHAIN

The analog pixel readout chain shown in Figure 1 has been implemented as a two-stage architecture, optimized for low noise, low power and fast rise time. The output signal of the second stage is coupled to a discriminator for comparison with a global threshold. Threshold tuning and trimming of the preamplifier’s feedback current is applied by dedicated local DACs. Calibration of the analog pixel electronics is performed by a local charge injection circuitry. The two-stage approach offers more options for optimization than an ordinary single-stage. The second stage gives an additional amplification factor that is defined by the ratio of the coupling capacitor $C_c$ to the feedback capacitor $C_{f2}$ of the second stage. This extra gain allows to increase the preamplifier feedback capacitance $C_{f1}$ about the same factor without reducing for a given charge input signal the signal pulse magnitude arising at the comparator’s input.

A higher preamplifier feedback capacitance is advantageous for charge collection efficiency, signal rise time and power consumption. To have a high charge collection efficiency, the effective collection capacitance of the charge sensitive amplifier (CSA) which is defined as the product of the preamplifier gain times the feedback capacitor has to be much higher than the detector capacitance. Going to higher feedback capacitances has the benefit that a good charge collection efficiency independent of detector capacitance can be achieved with less preamplifier gain and as a result less power. Signal rise time scales inverse proportional to the transconductance of the preamplifier’s input transistor and the feedback capacitance. With a high feedback capacitance a specific signal rise time can be met with less transconductance of the preamplifier’s input transistor which again means less current and less power.

Furthermore the AC-coupling between first and second stage has the advantage that the rear part of the analog readout chain is decoupled from any DC-shift that could arise because of detector leakage current. Although the pixel is equipped with a leakage current compensation circuit, still the non ideal behavior of the compensation circuit gives rise to small DC-shifts which without AC-coupling would influence the system and would lead to threshold dispersion.

The schematic of the leakage current compensated CSA with constant current feedback that forms the first stage is shown in Figure 2. The preamplifier is implemented as a regulated telescopic cascode with a Triple-Well NMOS input transistor. The availability of Triple-Well transistors allows to exploit the higher transconductance of NMOS transistors with respect to PMOS due to higher mobility and still be shielded from substrate noise. Furthermore the NMOS input transistor gives a low DC output potential that introduces a high dynamic range for the expected positive going output signals. The regulated cascode has a high output impedance and hence a high gain. Moreover the regulated scheme needs less biasing voltages and thus has less crosstalk paths and eases routing. The telescopic structure has the advantage that the highest current in the amplifier flows through the input transistor and not through any biasing transistor which reduces the noise contribution from the biasing.

Continuous reset is applied by a NMOS feedback transistor which is biased by a current mirror topology. For high output signals, the NMOS feedback transistor gets saturated and drains a constant current. A nearly linear return to baseline and as a result a pulse width proportional to the input charge is obtained. A slow differential amplifier monitors the DC shift between input and output of the preamplifier caused by the detector leakage current. If a leakage current is drawn out of the input, the
rising output potential is sensed and a dedicated PMOS transistor connected to the input is steered to compensate for the leakage current flow. Simulations show that for a leakage current of about 100nA, the resulting DC shift is limited by the compensation circuit to 10mV.

The second stage is a PMOS folded cascode. A PMOS input transistor has been chosen due to the well suited output potential that gives a high dynamic range for the expected negative going output signal. Finally the comparator is made out of a classic two stage architecture. The overall analog readout chain performance has been simulated and the results show an ENC dependence on the detector capacitance of $70e^- + 0.15e^- / fF$. The timewalk with a threshold of $1.5ke^-$ and the charge input signal varying between $2ke^-$ and $52ke^-$ is about 20ns.

III. DIGITAL ARCHITECTURE

As seen in section I a digital architecture different than in FE-I3 has to be designed to increase the hit rate capability and reduce the digital activity for power saving. First it is crucial to identify the limitations and restrictions of the currently used FE-I3 architecture. The readout of both FE-I3 and FE-I4 is organized in double columns. In FE-I3 (see Figure 3) every pixel that is hit transfers its data through the double column bus to the end of column (EoC) which is outside the active region at the bottom of the chip. A hit pixel is blocked until the double column bus is free and the data has been stored in the EoC buffer. Simulations show that at ~3x LHC luminosity the double column bus starts to saturate leading to a steep increase in hit losses up to an unacceptable level.

The FE-I4 architecture exploits the fact that 99.75% of the hits will not be triggered and therefore will not be transmitted off-chip. With the higher integration density the new technology offers, it is now possible to store all hits in local pixel buffers inside the double-column bus and to synchronize them by local logic to the trigger. As a consequence the double-column bus is now used only for the transmission of triggered hits and data traffic is drastically reduced. This has the side effect that power is saved because unnecessary digital activity is avoided.

Another new concept of the FE-I4 architecture is the sharing of timing information between several pixels which suits the clustered nature of real hits. In Figure 4, a possible architecture configuration is shown where two adjacent pixels lying one above the other are grouped together in one Regional Logic Unit (RLU) to share the same digital logic. In the same Figure two RLUs store their data locally in the same Local Buffer (LB) of a certain depth. Simulations show that this specific configuration with a Local Buffer depth of six cells at 2-3 times LHC luminosity and 3.7cm b-layer radius can cope with the expected hit rate with an acceptable level of inefficency (for more details see [5]).

Apart from abstract high level C++ simulations the different architecture options are investigated at Verilog Register Transfer Level (RTL), post synthesis and place & route gate level to estimate power consumption and required implementation space.

IV. PERIPHERAL BLOCKS

As a result of the technology change, the full peripheral chip infrastructure needed for the proper operation of the chip has to be redesigned as well, using radiation-hardening techniques. DACs and reference circuits are needed to bias and calibrate the chip. LVDS transmitters and receivers are used for fast off-chip communication. To improve the powering efficiency, a shunt type regulator for the serial powering approach, a divide-by-two charge pump DC-DC converter and a low drop out (LDO) regulator useful for both powering schemes have been implemented.

Various latch designs for use in single event upset (SEU) tolerance studies [6] and a control block for command decoding have been developed. Some of the above mentioned blocks are covered in more detail in the next subsections.

A. LVDS circuits

As has been mentioned in section I, a data transmission rate of 160 Mb/s has been specified for the FE-I4. To have some margin and as a first step towards designing LVDS communication blocks for the needs at super-LHC, LVDS circuits have
been developed to reach a maximum clock rate of 320 MHz. The LVDS circuits have to operate in a supply voltage range of 1.2-1.5V so that the use of thick gate oxide transistors can be avoided and the amount of necessary supply rails is reduced.

As the supply voltage is reduced, these LVDS blocks do not use the usual IEEE LVDS 1.2V offset standard but a reduced offset to the half of the FE-I4 power supply. Note that FE-I4 type pseudo-LVDS driver is still able to communicate with commercial LVDS receivers as the standard stipulates a wide common-mode input voltage range at the receiver side [7], and the offset voltage of a commercial LVDS driver can be adapted to smaller values by added external circuitry so that driving a FE-I4 type pseudo-LVDS receiver for test purposes is also possible.

Regarding the LVDS driver, a standard architecture has been chosen and adapted to the smaller supply voltage range [8]. The output signal current is configurable in a range of 0.6-3.0mA. In a later iteration, a tristate output option has been added to the LVDS driver which might be beneficial for use in combination with a token pass method to multiplex the signal outputs of several FE-I4 chips through one transmission line at the outer pixel layers for SLHC.

In Figure 5, a simplified schematic of the LVDS driver with tristate option is shown. In a standard architecture transistors M3 and M5 or respectively M4 and M6 are connected to the same control signal because either the upper transistor switch is closed and the lower is open or vice versa. In the shown schematic, all switching transistors M3-M6 are steered by separate control signals. Hence it is possible to keep all switches open at the same time which gives a high impedance state at the output and decouples the LVDS driver from the transmission line. Additional logic is needed to control the state of the transistor switches with respect to the data and enable input signal.

Because of the very low supply voltages, it is not possible to use conventional rail-to-rail input stages for the LVDS receiver. An approach with two completely independent comparator input stages has instead been chosen, one having an NMOS differential input pair that is covering high common-mode input voltages, the other having a PMOS differential input pair covering low common-mode input voltages [9]. The two signals paths are combined in a second stage and converted to a full-swing CMOS signal. Although this scheme fits better to the low supply voltage environment, the transistor threshold-voltages still have to be carefully chosen and fine-tuned to obtain rail-to-rail operation.

B. LDO regulator

The Low Drop Out (LDO) regulator is used to down convert an unregulated input voltage of 1.6V to a configurable output voltage in the range of 1.5-1.2V, providing a maximum load current of 500mA at a minimum drop out of 100mV. Line regulation, defined as the percentage of change of the regulator's output voltage relative to the change in input voltage is specified to be 0.3-0.4% for an input voltage ripple of 100mV whereas load regulation which is defined as the percentage of change in output voltage for a specific current load change has been specified to be 0.3-0.4% for a load variation of 150mA.

The implemented LDO shown in Figure 6 is composed of a wide PMOS power transistor, an error amplifier that senses the output voltage through a resistive divider and compares it with a reference voltage and additional circuitry that is employed to allow stable operation even with ceramic output capacitors with low equivalent series resistor (ESR).

Calculations and simulations show that an error amplifier with a DC gain of about 60DB is sufficient to meet the regulation specifications. Therefore the error amplifier has been designed as an two-stage amplifier (Figure 7) avoiding poles located below the gain-bandwidth product (GBW) of the regulators open loop. For a symmetric slew-rate behavior a Class-AB output stage is required which has been realized by a fully-differential first stage combined with a common-mode feedback circuit (M6-M11). Conventional circuits use gate-drain connected transistors in the first stage (transistors M4 and M5 in Figure 7) but this lowers the output impedance and hence the gain of the first stage. Thus the proposed circuit implements a Class-AB output stage in an innovative and power efficient way.

LDO regulators are inherently unstable and therefore special attention has to be given to stabilization. Typically the ESR of the output capacitor is used to introduce a zero into the open loop transfer function which leads to compensation by pole-zero.
cancellation [10]. Unfortunately a very small ESR is necessary for a good fast transient response of the LDO [11], which limits the frequency location of the introduced zero to high frequencies. Hence an alternative compensation method has been applied which allows the use of high quality low value ESR ceramic output capacitors.

As shown in Figure 6, a frequency dependent voltage-controlled current source is used which is steered by the LDO output voltage and feeds its output current into the resistive divider [12]. At high load currents and small drop out voltages, the output impedance of the LDO regulator becomes very small. Combined with the fact that the material budget limits the maximum value of output capacitance, the LDO bandwidth has an untypically high value. As a result the compensation circuit implementing the frequency dependent voltage controlled current source has also to be high bandwidth.

The compensation circuit proposed in the literature [12] has a bandwidth restriction caused by nondominant poles related to the circuit’s complexity. Hence a new compensation circuit (Figure 6 left) based on a transimpedance amplifier input stage has been developed. The output signal of the LDO is AC-coupled to the circuits input which gives a rising AC current flow with frequency. The introduced excess current is flowing out of the circuit into the resistive divider creating a zero in the frequency location of the introduced zero to high frequencies, it does not contribute to the regulation performance and helps distributing the shunt current between the regulators. Therefore an additional ”slope” resistor is placed at the current input of the shunt regulators which smooths out the current to voltage characteristic and helps distributing the shunt current between the regulators.

Although this additional slope resistor is needed for safe operation, it does not contribute to the regulation performance and consumes additional power. Hence a scheme where this constant resistor could be replaced by a regulated resistor of variable size would be very beneficial. The functionality of the PMOS power device used in LDO regulators is that of a regulated resistor. Therefore the regulator architecture shown in Figure 8 has been developed that combines a LDO type regulation scheme with the shunt capability known from shunt regulators.

The LDO part in Figure 8 is composed of the power transistor M1, the error amplifier A1 and the resistive divider R1 and R2 which is used to sense the output voltage. The LDO is responsible for the regulation of the output voltage Vout. To this
scheme an integrated shunt transistor \( M4 \) has been added that is steered to draw all the current that is not flowing through the load connected at the voltage output port of the regulator.

For the control of the shunt transistor, a fraction of the current flowing through the power transistor \( M1 \) is mirrored to transistor \( M2 \) and drained into the gate-drain connected transistor \( M5 \). The amplifier \( A2 \) and the cascode transistor \( M3 \) are added to improve the mirroring accuracy. Amplifier \( A3 \) compares the mirrored current to a reference current flowing into the gate-drain connected transistor \( M6 \) which is defined by the resistor \( R3 \) and the voltage drop \( \text{Vin} \) across the current input and output of the regulator. In this manner, a constant current flow through the regulator is assured which is either drawn by the load or shunted by transistor \( M4 \).

With the proposed regulation scheme a robust parallel operation of regulators generating completely different output voltages is possible without problems rising regarding the distribution of the shunt current. In Figure 9, simulation of the parallel operation of two regulators is shown, having an output voltage of 1.5V and 1.2V respectively. As can be seen in the lower part of the plot the currents flowing through the regulators are exactly the same.

In reality mismatch of the integrated resistor \( R3 \) might lead to a shunt current variation of about 10% but this will not cause device break down. In addition, an on-chip resistor trimming mechanism can be applied or an external high-precision resistor can be used if necessary. As can be seen in Figure 9, the shunt current depends on the supply current which has the advantage that the regulator can cope with an abrupt increase in supply current which can happen if one FE-I4 chip does not contribute to the shunt current any more e.g. because of disconnected wire bonds. Finally this scheme is also very flexible. For use in a normal voltage based powering scheme, the shunt part of the regulator can be switched off and the regulator can be used as an ordinary LDO.

V. CONCLUSION

An overview of the ongoing development effort for the FE-I4 readout chip in 130 nm technology targeting ATLAS pixel b-layer upgrade and the outer layers at super-LHC has been given. Prototypes of the pixel analog array and some of the peripheral structures (DACs, current reference, LDO, LVDS circuits, command decoder, SEU-tolerant latches) are available and functional test as well as pre and post irradiation studies are under way. In parallel new concepts for the FE-I4 digital architecture are refined and investigated by parallel high level C++ modeling, RTL and backannotated gate level based timing simulations. The design of a full-scale FE-I4 IC is foreseen for the year 2009.

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Development of a Front-end Pixel Chip for Readout of Micro-Pattern Gas Detectors.

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Abstract.
With growing importance of Micro-Pattern Gas Detectors in high-energy physics there is a need to develop a dedicated front-end read-out chip. The new chip should secure high spatial resolution provided by the gas-filled pixel detector and be able to operate at high track rates. In addition, it is highly required to keep power consumption as low as possible.

A number of prototype IC’s have been submitted in order to demonstrate the performance of the new front-end circuit (preamplifier and comparator) and the feasibility to implement a high resolution TDC per pixel.

In line with the present results we discuss system requirements and a list of specifications for a final large size chip.

I. Introduction
With the invention of Micro-Pattern Gas Detectors (MPGD), in particular the Gas Electron Multiplier (GEM) and the Micro-Mesh Gaseous Structure (Micromegas), the Integrated Grid on chip offers the potential to develop new gaseous detectors with unprecedented spatial resolution, high rate capability, large sensitive area, operational stability and radiation hardness. Modern wafer post-processing techniques allow the integration of gas-amplification structures directly on top of a pixel readout chip. Thanks to these recent developments, particle detection through the ionization of gas has a large field of applications in future particle, nuclear and astro-particle physics experiments with and without accelerators [1].

A CMOS pixel chip can be assembled directly below the GEM or Micromegas amplification structure (see Fig.1) and serve as an integrated charge collecting anode. With this arrangement electrons generated in an avalanche, are collected on the top metal layer of the CMOS chip; every input pixel is then directly connected to the amplification, digitization and sparcification circuits, integrated in the underlying active layers of the CMOS technology. Using this approach, gas detectors can reach the level of integration density typical of solid-state pixel devices.

A number of research groups have expressed interest in exploring the potential of the pixel readout of gas detectors. At the same time there is interest in the High Energy Physics tracking community and in the Medipix Collaboration for a general purpose readout chip with similar characteristics. All users require a pixel cell providing simultaneously both energy and hit time information and a readout architecture which would allow the chip to be triggered externally. Given the resources needed for such a development it is beneficial that a chip could be designed that satisfies as many users as possible.

II. Prototypes: experimental results.
A number of prototypes of the front-end readout chip have been developed with the purpose to demonstrate performance of MPGDs and to characterize the basic circuits.

A. The Timepix chip.
The Timepix is a full size chip designed at CERN in 0.25μm CMOS technology [2]. Detection area of the chip is a matrix 256 by 256 pixels with a pitch of 55μm. This circuit allows for measurements of charge arrival times for each pixel individually with 10-ns accuracy. This feature makes 3D track reconstruction possible. Figure 2 demonstrates spiral tracks of low-energy electrons in a magnetic field taken with the Timepix chip.

Figure 1: Layout of the micro-pattern gas detector with the amplification structure based on an integrated grid.

Figure 2: Spiral tracks of low-energy electrons in a magnetic field.
B. GOSSIPO-1 chip.

GOSSIPO-1 chip [3] was developed at NIKHEF in 2005 in 0.13μm CMOS technology and it contained the prototype of the front-end circuit. The main goal was to demonstrate that a detector with low parasitic capacitance (~20fF) and no sensor leakage current would let us design a fast response time (less than 40-ns peaking time), low-noise (ENC is 70-e RMS) and low-power (2-μw per channel) front-end circuit.

C. GOSSIPO-2 chip.

Gossipo-2 chip (see Figure 3) was a small-area pixel readout array consisting of 16 by 16 pixels with a pitch of 55μm [4]. The main goal of this chip was to prototype a high resolution and low-power TDC-per-pixel architecture, based on a switched local oscillator running at 600MHz. The circuit uses an external 40MHz clock as time reference. For detail characterization a separate TDC block and an oscillator circuit have also been placed on the chip.

III. Characterization of basic blocks.

A. Time-to-digital converter.

The TDC consists of a local oscillator circuit, a 4-bit fast clock counter and a 4-bit (system) clock synchronous counter (see Figure 4).

B. Local oscillator.

The local oscillator (F_{fine} = 560MHz) will be started by the Hit signal and will be stopped by the coming leading edge of the clock signal (F_{coarse} = 40MHz) (see Figure 5). The number of the “fine” clocks will be counted as well as the number of “coarse” clocks until the trigger signal appears. The data is two 4-bit words representing the final state of the counters.

The converter output code as function of the Hit signal delay is in Figure 5. The time resolution of the TDC (1.8ns) is determined by the frequency of the local oscillator. The dynamic range is set by the frequency of the clock signal and the length of the clock counter. The average TDC power consumption depends on the rate of the Hit signal. For the rate of a 100kHz (for LHC experiments) it is about 0.4μW.

Figure 3: Layout of GOSSIPO-2 chip.

Figure 4: Signals in the TDC circuit.

Figure 5. The output of the TDC circuit as function of the delay of the Hit signal.

B. Local oscillator.

The local oscillator circuit includes a NAND gate with a chain of inverters in the feedback (see Fig.6). A positive signal at the input triggers the logic and the circuit will start to oscillate at the frequency determined by the delay in the feedback. The oscillation frequency (560MHz) is 14 times higher than the clock frequency (40MHz). This means that 14 oscillator cycles are within one clock period and that the position of the leading edge of the input pulse can be determined with an accuracy of 1.8ns.
The gate delay of the CMOS inverters is very sensitive to variations in the temperature, power supply voltage. We have carried out a careful study of the stability of the oscillator frequency. Measurements show that the period of the oscillations is directly proportional to the temperature, with a slope of 2% per 10°C, and inversely proportional to the power supply voltage, with the slope of -12% per 100mV. This is in agreement with simulations. We conclude thus that variations over temperature within 30°C or variations over power supply voltage within 50mV would lead to a 6% shift of the frequency. This is tolerable as it results in less than one oscillator cycle within one clock period (25ns) and, therefore, is not visible in this type of TDC.

Transistor mismatch will lead to spread of the value of the delays across the channels. Any tuning solutions are usually unwelcome. In the present design the channel-to-channel spread of the value is 4% which is less than the width of the bin of one TDC. It is possible to reduce the spread by means of resizing of the transistors. However it will lead to the increase of power consumption and the area on the chip.

C: Experimental results; time resolution under various conditions.

In order to estimate time resolution of the complete read-out chain (see Figure 7) we measured the time interval between the Test- and the Trigger (Read) signal. Figure 8 represents results of the measurements of this time interval as function of the threshold value at different input signal sizes. In order to get the best time resolution we should position the threshold just above the noise (350e−). Under this condition the time jitter will be 4 bins of the TDC (7.2 ns) for small signals (1200e−). For larger signals (3000e−) the jitter will be lower 2 bins (3.6ns) and for signals as large as 12000e− the jitter will be kept within 1 bin (1.8ns).

We also did a time scan in the complete read-out chain that covers the dynamic range of the TDC. We shifted the Hit signal in respect the Trigger and monitored the output code. Figure 9 presents result of the measurement under the following conditions: signal size is 4000e− and the threshold is 350e−. In this case the transition region (from one TDC bin to the next) is quite narrow (1ns) and less than 1 TDC bin.

IV. Main specifications for Timepix2 - general purpose readout chip for micro-pattern gas detectors.

It has been proposed within the RD51 collaboration that a new general purpose front-end chip is required for readout of micro-pattern gas detectors. The chip should meet requirements imposed by the groups developing TPC’s (time projection chambers), GOSSIP (gas on slimmed silicon pixel
detectors) and the large-area drift chambers. Moreover the chip should be suitable for readout of silicon-sensor based detectors. The chip would be developed in 0.13μm CMOS technology. Designers from CERN, NIKHEF (Amsterdam), Bonn and Saclay have expressed their interest in this work. The chip would have sensitive area of a 14mm by 14mm (1.98cm²). It will be a matrix of 256 by 256 pixels with the pitch of a 55μm. Only single pixel operation is foreseen. There should be low input referred noise level (70e⁻) which will allow for low threshold operation (350e⁻). Every pixel will be equipped with a high resolution TDC making possible the measurement of the arrival time with an accuracy of about 2ns. The dynamic range of the TDC is not defined yet. It is also required to deliver information on charge deposited to the pixel.

There should be a local (on-pixel) memory for storing data generated by multiple hits in the time until the trigger signal arrives.

The following readout modes are required:
- all pixel readout (time frame based) with zero suppression
- readout of the data associated with a trigger (for LHC like experiments)
- event driven readout.

Data taking and data readout should be independent and run in parallel driven by a 40MHz external clock. For readout a fast serial link (≥1Gb/s) is needed.

V. Summary

A new front-end chip is required for readout of micro-pattern gas detectors (MPGDs).

It should be also suitable for detectors employing Silicon sensors.

A number of prototypes have been fabricated successfully in order to verify the performance of the basic circuits.

The TDC per pixel with local oscillator satisfies the design requirements: low power consumption (0.4μW/channel with 100kHz hit rate), high time resolution (1.8 ns bin) and simplicity. It demonstrates low crosstalk to the sensitive inputs.

Low threshold (350 e⁻) and fast peaking time (20 ns) enable for high quality drift time measurements (jitters 1.8 ns) at large input signals (>4000 e⁻) and after accurate threshold equalization.

Work on the technical specifications and the definition of the structure for a new MPGD chip has started.

VI. References.


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Abstract

CMOS Monolithic Active Pixel Sensors (MAPS) have demonstrated their strong potential for tracking devices, particularly for flavour tagging. They are foreseen to equip several vertex detectors and beam telescopes. Most applications require high read-out speed, imposing sensors to feature digital output with integrated zero suppression. The most recent development of MAPS at IPHC and IRFU addressing this issue will be reviewed. An architecture will be presented, combining a pixel array, column-level discriminators and zero suppression circuits. Each pixel features a preamplifier and a correlated double sampling (CDS) micro-circuit reducing the temporal and fixed pattern noises. The sensor is fully programmable and can be monitored. It will equip experimental apparatus starting data taking in 2009/2010.

I. INTRODUCTION

Subatomic physics experiments express a growing need for very high performance flavour tagging, with emphasis on short lived particles (e.g. charmed mesons) through their decay vertex. This calls for an excellent vertexing and tracking system in order to reconstruct the secondary vertices and to measure precisely the momenta of tracks. This translates into the need to improve the system’s accuracy by typically an order of magnitude with respect to the existing state of the art.

The existing pixel technologies are not adequate for this new challenging requirement level, associated to a highly granular, ultra-light, radiation tolerant, fast and poly-layer vertex detector installed very close to the beam interaction point. CMOS MAPS provide an attractive trade-off between granularity, material budget, readout speed, radiation tolerance and power dissipation, which may suit the ambitioned vertexing performances.

MAPS are developed since several years for this goal. One of their most specific aspects is that the sensitive volume and the front-end read-out electronics are integrated on the same substrate. The charges generated by an impinging particle in the, typically 5 to 15 µm thin, epitaxial layer underneath the readout electronics are collected through thermal diffusion by regularly implanted N-well/P-epi diodes. These charges are then converted, “in situ”, to voltage signal at the capacitance of the sensing diode. The signal can then be treated by the integrated readout electronics. Being fabricated in standard CMOS processes available through many commercial microelectronics foundries, they are attractive for their cost effectiveness and the fast multi-project run turn-over.

MAPS tracking performances are now well established [1]. Thanks to their particularly low equivalent noise charge (ENC), the most probable value (MPV) of the signal-to-noise ratio (S/N) ranges from 15 to 30, depending on the pixel size (Fig. 1a). A detection efficiency exceeding 99.5% was demonstrated, even in the case of a pitch as large as 40 µm, at an operation temperature of up to 40 °C (Fig. 1b). The single point resolution was measured from ~1 µm for a 10 µm pixel pitch up to ~3 µm for a 40 µm pitch, for sensors with analogue readout.

Figure 1: Pixels analogue readout performance

Although analogue readout MAPS show excellent performances, they suffer from moderate readout speed in case of a large amount of pixel information transfer need. Numerous application domains require simultaneously high granularity and fast read-out speed. Integrating signal processing functionalities inside the sensor, such as CDS, ADC (Analogue to Digital Converter), data zero suppression circuitry are then facing severe constraints from the pixel dimensions, readout speed and power consumption. A prototype sensor Mimosa16 [2], with 24 integrated column-level discriminators, had been realised to check detection performances for sensors with digital readout. Figure 2 shows the detection efficiency, the single point resolution and the average fake rate as a function of the discriminator threshold.

The detection efficiency is nearly 100 % up to a threshold
value of 6 mV, corresponding to ~6 times the noise standard deviation, with a fake rate below $10^{-5}$ and a spatial resolution better than 5 µm. The latter is better than a pure digital resolution (pixel pitch of 25 µm) thanks to charge sharing among pixels in a cluster due to thermal diffusion.

These results lead to confirm the choice of a new CMOS MAPS architecture combining, on the same substrate, a pixel array occupying an active area of reticle size, column-level discriminators for analogue-to-digital conversion and a zero suppression circuit for data sparsification.

MAPS are foreseen for several applications, ranging from subatomic physics experiments up to bio-medical imaging devices. Their first use inside a vertex detector coincides with the upgrade of the STAR experiment at RHIC. MAPS also equip the beam telescope of an EU project, called EUDET, underlying the R&D for the ILC (International Linear Collider) vertex detector.

In the first part of the paper, the applications both for the STAR vertex detector upgrade and the EUDET beam telescope will be presented with their technical requirements. In the second part, the architecture of MAPS optimised for these applications, developed by the IPHC-Strasbourg and IRFU-Saclay collaboration, will be discussed in detail.

II. EXAMPLES OF MAPS APPLICATIONS

A. STAR Heavy Flavor Tracker (HFT) upgrade

The STAR upgrade is designed to allow for direct topological reconstruction of D (and B) mesons through the identification of decay vertices displaced from the primary interaction vertex by 100-150 µm [3]. In order to achieve a vertex pointing resolution of about, or better than, 30 µm, two nearly cylindrical MAPS layers with averaged radii of about 2.5 and 8 cm, will be inserted in the existing detector (Fig.3). No space will be available for a sophisticated cooling system. Only simple air flow can be used, meaning that MAPS sensors have to be operated at room temperature. The power consumption of MAPS should therefore be in the order of 100 mW/cm². Moreover, multiple coulomb scattering concerns impose to keep the material budget per layer as low as ~ 0.3% of radiation length. All sensors should therefore be thinned down to 50 µm. The final pixel sensors, expected to be operated with Au + Au collisions at a RHIC II luminosity of $\sim 8 \times 10^{33} \text{cm}^{-2}\text{s}^{-1}$, will face a hit density in the order of $10^9 \text{hits/cm}^2$ in the inner layer. The total ionising dose was estimated to 150 - 300 kRad per year and the non-ionising radiation dose should mainly come from an annual flux of 3 - $12 \times 10^{13}$ charged pions per cm² traversing the inner layer [4].

The HFT vertex development is a three step process. The first step was achieved by operating successfully a MAPS telescope prototype in the STAR environment during the 2007 Au + Au RHIC run [5]. The telescope consists of three planes, each made of a MimoSTAR2 chip [6]. Each chip provides a 128 x 128 pixel array with 30 µm x 30 µm pixels. With its serial analogue outputs, MimoSTAR2 was a first generation sensor. The second step, foreseen in 2009, consists in equipping three sectors (~30 % of the surface) of the HFT with second generation MAPS, named “Phase1”. They feature a 640 x 640 pixel array with 30 µm pitch. This sensor, ready for fabrication, contains on-chip CDS and column level discriminators. The readout is in rolling shutter mode with an integration time of 640 µs. Finally in 2010, the whole HFT vertex detector will be equipped with still faster and more granular sensors, named “Ultimate”. They will contain all attributes of Phase1 sensors, complemented with a faster rolling shutter clock which allows decreasing the integration time to 200 µs. An integrated zero suppression circuitry will be implemented in the sensor. The Ultimate chip will have a 1152 x 1024 pixel array with 18.4 µm x 18.4 µm pixels.

B. EUDET telescope

The aim of EUDET is to provide to the scientific community an infrastructure exploiting R&D on the different detectors for the future international linear collider (ILC). It covers three main activities relating to vertexing, tracking and calorimetry R&D, together with networking activities supporting information exchange. The vertexing activity aims to construct a CMOS pixel beam telescope with six planes of sensors to be operated at the DESY electron test beam facility. The beam telescope, providing an extrapolated resolution better than 2 µm, is to be used for a wide range of R&D applications and quite different devices under test (DUT), from small (a few millimetres) to large (up to one meter) size.

In order to minimise the risk, the construction of the telescope was organised in two stages. In the first stage, a demonstrator telescope (Fig. 4), exploiting the existing CMOS MAPS sensors with analogue readout, has been realised. It is successfully operated since 2007 [7]. In 2009, the final telescope will be equipped with sensors providing an active surface 4 times larger and a readout speed (~100 µs) about an order magnitude faster than the previous one. The sensors will have a 1152 x 576 pixel array with 18.4 µm pitch, and will be
equipped with integrated CDS, fully digital fast readout and integrated data zero suppression circuitry. Their architecture will be extended to the Ultimate sensor for STAR.

Figure 4: EUDET demonstrator telescope

### III. Fast Readout Architecture

The development of this architecture is based on two separate prototyping lines: one addressing the upstream part of the signal detection and processing chain, and one devoted to data sparsification and formatting. Two prototype circuits, Mimosa22 and SUZE, were fabricated in the AMS CMOS 0.35µm technology, addressing these two research lines. The sensor exploring the signal sensing and analogue processing features 128 columns of 576 pixels ended with a discriminator. Each pixel (18.4 µm x 18.4 µm) contains a preamplifier and a CDS circuitry. The sparsification chip incorporates the zero suppression logic and the output memories needed for the EUDET beam telescope and the STAR vertex detector upgrade. In the proposed architecture, the pixel array is read out in rolling shutter mode, the row being selected sequentially by a shift register. The design is organised according to three main issues:

- Increasing the S/N at pixel-level
- Analogue to digital conversion at column end level
- Zero suppression at chip edge level

**A. Pixels**

Pixel-level amplification and CDS are necessary to increase the S/N in order to perform column-level digitisation. The CDS suppresses low frequency noise, including reset and fixed pattern noise (FPN). The difficulty of in-pixel signal processing is that only NMOS transistors can be used, since any additional N-well used to host PMOS transistors would increase and a FPN remaining essentially unchanged. The feedback self biased structure (Fig. 6(c)) exhibits the best behaviour, with the smallest temporal noise increase and a FPN remaining essentially unchanged.

The pixel architecture is illustrated in figure 5. A preamplifier stage is implemented nearby the sensing diode. It is active only when the row is selected to be read, which reduces significantly the power consumption. A source follower connected capacitor, using a MOSCAP, and a clamping switch are used for the double sampling. A source follower function of the ionising radiation dose to which the sensor was exposed. The feedback self biased structure (Fig. 6(c)) exhibits the best behaviour, with the smallest temporal noise increase and a FPN remaining essentially unchanged.

**Figure 5: Pixel topology**

**Figure 6: Pixel amplification**

The three pixel variants been implemented in the prototype chip Mimosa22, and tested with an 55Fe source (5.9 keV X-ray) at 20 °C. The power consumption per pixel, in the activated row to be read out, is about 200 µW. Table 1 illustrates the measured performances. Figure 7 shows the measured temporal noise and FPN of the three pixels as a function of the ionising radiation dose to which the sensor was exposed. The feedback self biased structure (Fig. 6(c)) exhibits the best behaviour, with the smallest temporal noise increase and a FPN remaining essentially unchanged.

**Figure 6** represents the in-pixel amplifier design evolution, which has the following objectives:

- to reach maximal S/N for a given N-well sensing diode size;
- to minimise the power consumption;
- to squeeze the pixel to pixel dispersion.

**Figure 5: Pixel topology**

**Figure 6: Pixel amplification**

<table>
<thead>
<tr>
<th>Pixel types</th>
<th>Diode size (µm²)</th>
<th>CVF* (µV/e⁻)</th>
<th>ENC (e⁻)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS (a)</td>
<td>15.21</td>
<td>57.3</td>
<td>13.3 ± 0.1</td>
</tr>
<tr>
<td>Improved CS (b)</td>
<td>15.21</td>
<td>57.3</td>
<td>13.0 ± 0.1</td>
</tr>
<tr>
<td>Feedback &amp; self biased (c)</td>
<td>14.62</td>
<td>55.8</td>
<td>12.3 ± 0.1</td>
</tr>
</tbody>
</table>

* CVF: Charge-to-Voltage conversion Factor
Increasing the inherent tolerance against ionising radiation damages belongs to the main pixel design goals. At the pixel circuit level, the transistor serially connected to the sensing diode should be an enclosed layout transistor (ELT) surrounded by a guard ring to minimise the drain-source leakage current. As far as the sensing diode is concerned, the thick oxide surrounding it by default needs to be removed by introducing a pseudo-gate ring. The performance of this radiation tolerant diode design has already been reported in [10]. One should note that the results presented both in table 1 and Fig. 7 use amplifiers coupled to radiation tolerant N-well diodes.

The effect of the damage of non-ionising radiation can be alleviated by decreasing the pixel pitch and the integration time and by enlarging the sensing diode area [11]. This favours, in this design, a pixel pitch below 20 µm.

B. Analogue to Digital Conversion

Column-level ADCs will be implemented below the pixel array. According to the rolling shutter readout mode, pixel signals (1152) of the selected row are transmitted to the bottom of the pixel array. The 1152 ADCs have to convert those signals to digital data at the row readout speed. Thus a high speed ADC with low power consumption and small layout size is required. The choice of the number of bits depends on the required spatial resolution and on the pixel size. The requirement on the spatial resolution of a single plane sensor, for the EUDET beam telescope, is about 5 µm. It is even less critical (< 10 µm) for the STAR application. In this case, the best solution is to choose a 1 bit ADC: a discriminator, for its lower power consumption and simplicity. All column-level discriminators (1152) use a common threshold value for comparisons. It will be adjustable and set to its optimal value (~5-6 times the noise standard deviation) to ensure ~100% of detection efficiency and low fake rate (~10^-4).

The column-level discriminator design has been shown in detail in [8]. Considering the small value of the analogue signal, it is mandatory to use an offset compensated amplifying stage (Fig. 8) which corrects the residual offset of the discriminator. The power consumption per discriminator is below 250 µW.

The 128 column-level discriminators implemented in Mimosa22 were evaluated by scanning the common threshold voltage. The “S” curves were fitted with an error function to extract the offset, temporal noise and FPN.

Figure 9 shows the discriminator’s “S” curve. The extracted temporal noise and FPN are 0.3 and 0.2 mV respectively.

![Discriminator “S” curves of the measured Mimosa22](image)

Figure 10 displays the noise performances of the pixel array associated with discriminators. It is shown that the temporal noise comes mainly from the pixel array and column-level discriminators contribute mainly to the FPN.

![Pixel & Discriminator noise of the measured Mimosa22](image)

Mimosa22 was tested with ~120 GeV pion beam at CERN-SPS. The preliminary results show that the detection efficiency is better than 99.5 % for a threshold value corresponding to about 6.5 times the noise standard deviation. The spatial resolution is better than 4 µm while the fake rate is below 10^-4.

C. Zero suppression

The raw data flow of MAPS for STAR and EUDET may reach up to several Gbits/s per chip. The zero suppression circuitry is based on row by row sparse data scan readout and is organised in pipeline mode in 3 stages. This allows a data compression factor ranging from 10 up to 1000, depending on the hit density per frame. In the 1st stage, the 1152 column...
terminations are distributed over 18 banks (see Figure 11) which perform a parallel scan, based on a priority look ahead (PLA) encoding. This allows finding up to N states per bank which result from the encoding of up to 4 contiguous hit pixels (discriminator output set to “1”). This stage handles also the column address encoding and the continuity of the algorithm between the adjacent banks for the entire row. The 2nd stage combines the outcomes of 18 banks of PLA. Its multiplexing logic accepts up to M states per row and adds row and bank addresses. The choice of values for N and M depend on the hit density. The outcome is stored in the 3rd stage, i.e. a memory made of 2 foundry’s IP buffers, with a capacity up to 48 Kbits. The 2 buffers allow a continuous readout. While one buffer stores the compressed data of a frame, the other is read out via two LVDS transmitters at a frequency of up to 160 MHz. The memory capacity and the transfer frequency are adapted to each application.

The testability is another point to be considered. Several test points will be implemented in the design all along the data path, i.e. pixels, discriminators, zero suppression circuit and data transmission. These MAPS will be programmable, like previous sensors [6], via a boundary scan controller, for bias supplies and test mode settings.

For the MAPS used for the STAR vertex upgrade, some additional tests like Single Event Upset (SEU) and Single Event Latch-up (SEL), have still to be performed. Some digital circuit layout may have to be redesigned consecutively, especially the memory IP block.

IV. CONCLUSION

In this paper, a fast readout architecture of MAPS which integrates on-chip data sparsification has been presented. Its feasibility was verified with two prototypes. The readout speed reaches 10 kframe/s. This architecture seems to be an optimum choice for the chosen process technology. The final MAPS for the EUDET telescope will be sent to fabrication before the end of this year and the ultimate sensors for the STAR upgrade in 2009.

V. REFERENCES

Pixel Read-Out Architectures for the NA62 GigaTracker.

G. Dellacasa b, F. Marchetto, G. Mazza b, A. Rivetti b, S. Martoiu b
P. Jarron a, A. Ceccucci a, J. Kaplon a, A. Kluge a, F. Osmić a, P. Riedler a, S. Tiuraniemi a
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Abstract

Beam particles in NA62 experiment are measured with a Si-pixel sensor having a size of 300 μm x 300 μm and a time resolution of 150 ps (rms). To meet the timing requirement an adequate strategy to compensate the discriminator time-walk must be implemented and an R&D effort investigating two different options is ongoing. In this presentation we describe the two different approaches. One is based on the use of a constant-fraction discriminator followed by an on-pixel TDC. The other one is based on the use of a Time-over-Threshold circuit followed by a TDC shared by a group of pixels.

The global architectures of both the front-end ASIC will be discussed.

I. THE GIGATRACKER SYSTEM

The aim of the proposed NA62 experiment at the CERN SPS is to study the very rare decay of the charged K meson into a pion and neutrino-antineutrino pair. One of the key components of NA62 will be the GigaTracker, which consists of three matrices of Si-pixel stations, each covering a sensitive area of 60 mm x 27 mm. Each pixel is 300 μm x 300 μm [1].

The GigaTracker is designed to measure the beam particle trajectory with a space resolution of 100 μm (rms) and a timing accuracy of 150 ps (rms). In order to reconstruct the momentum of the beam particles a system of four dipoles, A1…A4 in Fig.1, provides the momentum selection followed by the beam recombination.

The timing resolution of 150 ps (rms) is an unusual requirement for a traditional pixel detector and none of the existing systems has such a capability. Other challenging aspects are due to the high radiation operational environment and the very low material budget restraint (0.5% X0 per station, sensor thickness 200 μm, read-out chip thickness 150 μm).

Each silicon sensor will be read-out by 10 front-end ASICs, with 45x40 read-out cells each.

The 10 read-out chips will be bump-bonded to the pixels, so only one side of the chip will be used for external connections (wire bonding pads in Fig. 2).
pixel and almost 1 GHz over the whole system (thus the name GigaTracker) [2].

In order to partly recover the radiations effects (10^5 Gy of total dose is expected in one year) the system will be cooled at 5°C or less and it will be replaced after a runtime of 60 days of work under optimum beam conditions.

II. READ-OUT CHIP OVERVIEW

The total average data rate per chip it will be around ~4.2 Gb/s, which corresponds to a maximum of ~6 Gb/s with fluctuations. Due to the huge amount of data to transfer, high speed serial links will be adopted and a trigger less read-out solution will reduce the amount of data to store inside the chip itself. In addiction the read-out chip should achieve the efficiency of 99%.

Two major issues have to be addressed to achieve the required time resolution: the compensation of the discriminator time-walk and the time measurement with such a high density of channels.

Time-walk problem can be addressed either via a Constant Fraction Discriminator (CFD) or a Time-Over-Threshold (TOT) correction. While the first approach requires only one measurement per hit, it poses more challenges on the design of the comparator.

The coarse time information will be provided by a clock counter. The issue of precise time resolution with a high read-out channel density can be dealt either with a Time-to-Amplitude Converter based TDC serving a single pixel or via a bank of DLL-based TDC shared among several pixels.

The TAC-based TDC solution requires more circuitry on the pixel area, thus potentially creating noise problems. Moreover, the pixel area receives a high radiation dose and therefore it has to be designed in order to be radiation-tolerant in both total dose and SEU aspects.

On the other hand, the DLL-based TDC has to be much faster in order to keep the dead time under control because the TDC is shared among pixels. Ambiguities can arise if two pixels which belong to the same TDC are hit close in time. Moreover, the TDC bank has to be placed at the end of the pixel column and therefore the signal carrying the time information has to be transmitted over a well calibrated transmission line in order not to degrade the timing information.

Preliminary investigations did not give a clear advantage of one solution over the other, therefore two prototypes will be designed in order to have an experimental comparison of the performances. For both architectures a demonstrator chip will be soon submitted in CMOS 130 nm technology.

III. ON PIXEL TDC ARCHITECTURE

This architecture will perform the walk time compensation by a Constant Fraction Discriminator filter (CFD) and the TDC option is a Time to Amplitude Converter (TAC) based on a Wilkinson ADC. Both CFD and TDC are implemented on the Wilkinson ADC. The whole information (coarse time, fine time and pixel address) is stored into the output buffer before being transferred to the end-of-column logic.

The system clock frequency is 160 MHz; the coarse time is measured with 10 bits, while the fine time occupies 8 bits. Finally the TDC binning is ~98 ps. One of the advantages of this architecture is the derandomization performed directly on the pixel cell and the very low dead time which is only due to the ramp generator or in case of buffers overflow. Exhaustive simulations have been performed in order to evaluate the FIFO depths (4 for the inner ones, 2 for the output one) and the number of lost events due the dead time (< 0.2% at 140 kHz).

The whole read-out chip is organized in column of 45 pixels each. The Column Controller performs the data reading and formatting. Then a group of m columns (where m depends on the output speed) is connected through the Matrix Controller and merged before to be read-out by a high speed serial output.

Figure 3: The pixel cell model for the on pixel TDC architecture
A first prototype of this read-out chip is going to be submitted by the middle of November 2008, using the IBM CMOS8RF technology (130 nm). The chip is made of 3 columns of pixels cells, fully equipped as described before.

IV. END OF COLUMN TDC ARCHITECTURE

The basic principle of the End Of Column (EOC) architecture is simple, but the implementation is challenging. Essentially, it consists of performing only the essential analogue signal processing functions in the pixel cell. The signals from the sensors are sent to a preamplifier and then to a Time Over Threshold discriminator. The ToT output fast hit signals are transmitted with constant amplitude and pulse width proportional to the input charge to the EOC circuits using transmission lines operating at low signal level in current mode. With this technique the pulse width information is used to correct offline for the time walk. All the rest of the processing functions, as hit time stamping, pixel address encoding, data pipelining in FIFO, and data formatting are done in the far end EOC on the chip periphery.

Each column is organized into two separate bus systems. The first is the data bus which transmits the hit information, leading edge and trailing edge. It comprises 9 coplanar transmission lines, where each line is connected to 5 pixels. The other 5-bit bus contains the address of 9 pixels. The EOC logic matches the signals from the two buses and determines in a unique way the hit address. This bus architecture is a compromise between the huge data flow, each 45-pixel column has peak occupancy of 4 M hits/s and an affordable number of lines of the column bus. The column bus transmits hit information to TDCs placed at the end-of-column. To maintain the efficiency higher than 99%, the solution used in the readout is to keep the column segmentation up to the serializer, as shown in Fig.6, and then connect each column output port to an on-chip or off-chip multiport parallel-in-serial-out Gigabit serializer. Finally the serializer drives the optical fibre Gigabit link. At the end of column, the architecture logic works both in pipeline memories and to equalize data rate fluctuations maximizing the throughput rate.

The TDC bank contains 9 TDC (each one serves 5 different pixels). Each of them contains 2 hit registers (leading edge and trailing edge) 32 bit each.
The DLL based TDC consists of 32 delays elements, 100 ps each and it is driven by a reference clock of 320 MHz. The fine time information of 32 bits is then encoded in 5 bit words, in order to reduce the amount of data. In addiction the EOC also fit 2 more 6-bit counters, to give the coarse time information of the leading edge and the trailing edge. In total, when 5-bit encoders are not implemented, 81 bits of information per hit will be generated.

Also for this architecture a submission of a prototype is foreseen for the middle of November 2008, in IBM CMOS8RF technology (130 nm). It contains a whole folded column of 45 pixels, all of them equipped with the preamplifier and the TOT discriminator. In addiction a 15 pixels columns foreseen, in order to study effects of corners.

Also the End of Column logic (TDC, Counters and data pipelining) will be implemented, for a total of 5+1 TDC. Data read-out is done by a serial LVDS driver.

V. SUMMARY

In Table 1 the main differences between the two possible read-out solutions are summarized. It’s important to note that in one case (on pixel TDC) there is a major concentration of possible problems in the pixel cell (power, noise due the digital circuits, radiation effects) but it is expected to have better performances in terms of dead time and amount of data produced. The second option (EoC TDC) offers a simpler pixel cell (only analog circuits) but a more complicated system of analog transmission lines and a big concentration of digital sources at the end of column (TDC banks, hit registers, decoders and counters).

The two proposed architectures, for the GigaTracker read-out system, are quite balanced in terms of advantages and disadvantages, so there have been no a priori reasons, to adopt one solution over the other. Only the results of the two prototype chips can give an experimental verification of their performances.

<table>
<thead>
<tr>
<th>TDC option</th>
<th>On pixel TDC</th>
<th>EoC TDC</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDC option</td>
<td>TAC based 1 x pixel</td>
<td>DLL based 1 each 5 pixels</td>
</tr>
<tr>
<td>Time Walk Correction</td>
<td>CFD</td>
<td>ToT</td>
</tr>
<tr>
<td>On-pixel logic</td>
<td>Preamp+C FD+TDC+ data buffers</td>
<td>Preamp+ToT+line drivers</td>
</tr>
<tr>
<td>Signals to the EoC</td>
<td>Digital</td>
<td>Analog</td>
</tr>
<tr>
<td>Noise in the pixel cell</td>
<td>Higher due digital sources</td>
<td>Lower (only analog)</td>
</tr>
<tr>
<td>System CLK</td>
<td>160 MHz</td>
<td>320 MHz</td>
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<tr>
<td>Bits per hit</td>
<td>32</td>
<td>81</td>
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<tr>
<td>Dead time</td>
<td>Only during TAC ramp</td>
<td>Multiple hits on the same pixels group</td>
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<tr>
<td>Total dose and SEU issues</td>
<td>Digital logic on exposed area</td>
<td>Only analog circuits on exposed area</td>
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<td>Power in the pixel cell</td>
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<td>Lower</td>
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<tr>
<td>Power in the EoC area</td>
<td>Lower</td>
<td>Higher</td>
</tr>
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VI. REFERENCES


Abstract

We present the ASIC development for the readout electronics of the Gigatracker pixel detector of NA62. Specifications of this detector are challenging in terms of timing precision with a hit time stamp accuracy of 100 ps and a peak hit rate of 50 Mhits/cm²/s. A timing precision and hit rate are more than one order of magnitude faster than pixel LHC readout ASIC. The research for pixel cell design and the readout architectures are following two approaches, which are presented and discussed in this paper. Presently demonstrator prototypes are under development and SPICE simulation results of the frontend, the readout strategy and the pixel-column are also presented and discussed.

I. INTRODUCTION

The pixel Gigatracker system of the NA62 experiment consists of 3 stations with a surface of about 12 cm² each [1]. The pixel cell dimension is 300 µm x 300 µm. Specification are extremely challenging. The hit rates in the centre of the beam of 50 MHz/cm² and the timing precision of 100 ps results in a large output data rate of more than 4 Gbit/s/chip for the 1800 pixels of one chip. The radiation levels are expected to be 10⁵ Gy and the 1MeV neutron equivalent fluence is estimated to be 2 x 10¹⁴ cm⁻² each running year. In order not to degrade the momentum resolution a very low material budget of 0.45 % X₀ is targeted for. This small material budget imposes a pixel ASIC die thinned down to 100 µm and a thin silicon or diamond sensor of 150 to 200 µm thickness. It has a strong impact on the analogue front end sensitivity pushing discrimination threshold down to 0.5 fC. The timing precision of 100 ps imposes to use an ultra fast shaping time in the range of 3-5 ns. Such a fast shaping time puts a specific constraint to silicon sensor operation that should be close to saturation velocity. At carrier saturation velocity, the silicon sensor is expected to deliver full induced charge in approximately 4 ns as presented in Fig. 1. However, such an intrinsic device speed might be not easily achievable in practice, and consequently there is a substantial risk of ballistic deficit [2].

After radiation sensor charge characteristics of the silicon sensor are degraded, and ballistic effect might severely affect signal to noise ratio of the electronic pixel channel. One possible alternative of sensor that NA62 has considered is diamond [3].
Diamond has several advantages in terms of radiation length, carrier velocity, and radiation hardness. However, the charge delivered by one MIP is significantly smaller than in silicon at the same sensor thickness. A deeper study is mandatory to validate the use of diamond sensor.

III. NOISE ANALYSIS OF ANALOGUE PIXEL FRONT ENDS

The main design challenge of the analogue part of the pixel front end is extremely short 5 ns pulse peaking time, combined with minimizing the power consumption, small Equivalent Noise Charge (ENC) and matching. Although the final version of the chip will contain trimming circuits, it is necessary to keep the mismatch of the threshold offsets at a reasonable level allowing a lower resolution of the trim DACs. Good matching together with satisfactory noise performance will permit lower threshold voltage improving timing performance of the comparator providing at the same time high efficiency of the detected signals and low noise occupancy. An analysis of the 130 nm CMOS8 RF LM/DM IBM technology is given in the plot Fig. 2, where ENC of the series, parallel and detector leakage noise contributions are expressed as a function of the total pixel capacitance in the case of an optimised preamplifier.

As one can see, for the 250fF detector capacitance we expect noise lower than 200e-. The actual gain of the front end amplifier is in the range of 70mV/fC and the simulated mismatch of the comparator offset is in the range of 6mV rms. (equivalent to 0.1 fC signal). Therefore the presented demonstrator chip will be able to operate with 0.7 fC threshold allowing both for very low noise occupancy, high efficiency and reasonable time walk of the comparator (1.5 ns between 1 and 4 fC signal) further compensated off line with time-over-threshold measurement.

IV. ON-Pixel TDC CELL

1) On−pixel TDC analogue pixel

The on-pixel TDC option has an architecture close to the traditional readout technique implemented in the ASIC of the LHC pixel detectors. Pixel cell comprises a preamplifier, shaper, discriminator time measurement and local buffering before transmission to the CMOS digital bus. However, the challenging requirements of the NA62 Gigatracker make circuit solutions adopted very different from LHC pixel design. The figure 2 presents the pixel analogue front end.

![Figure 3 schematic diagram of the on-pixel cell](image)

The preamplifier is optimized for a pixel capacitance of 250 fF, and it is followed by the Constant Fraction Discriminator (CFD) filter stage that performs the delay and subtraction with attenuated signal. Here the stage does not use a time variant filter as usually done for a CFD, but a continuous time filter that exhibits a close transfer function. Figure 4 shows SPICE simulation of the processed signals after the CFD stage.

2) TDC based Time to digital converter

![Figure 5 Schematic of the pixel TDC based on a Wilkinson time-to-digital-converter](image)
The on-pixel TDC circuit is based on a time to analogue converter followed by a Wilkinson ADC. Figure 5 presents the pixel TDC. When a hit occurs, the leading edge signal generated by the CDF stage closes switch S1 and C is charged by I1. At the clock leading edge, S1 opens and a voltage proportional to the time interval is build up on C which is transferred to 4C when S2 closes. Then S2 opens and S3 closes which discharge linearly 4C to the Vref potential. The generated ramp is then translated in a number of clock counts.

V. EOC PIXEL CELL

1) Pixel analogue front end

The pixel channel as presented in Figure 6 comprises 7 functional blocks:

- A transimpedance preamplifier
- A differential post amplifier
- A first stage of the discriminator
- Second stage of the discriminator with hysteresis
- A dynamic asynchronous latch comparator with transitional positive feedback
- A differential transmission line current driver with pre-emphasis
- A 300 µm length coplanar transmission line, not shown in the figure

The input stage is built around a cascode stage with an NFET input device biased at 40 µA and a feedback resistor of 200 kΩ.

Figure 6 Block diagram of the pixel channel performing fast charge pre-amplification, hit discrimination, and driving transmission line in GHz bandwidth with current mode pre-emphasis. Bias current of the analogue pixel channel is 120µA and 80µA for the transmission line driver.

2) Bus based transmission lines

The EOC architecture entirely relies on the timing precision of low power signal transmission down to the end of column circuits. CMOS level signal transmission is excluded since it consumes too much power and generates too much digital noise in the active pixel array. A low swing current mode logic level has been adopted. The principle of the transmission line bus is presented in Figure 7.

The bus system is based on lossy transmission lines integrated on the CMOS process [4,5]. The bus architecture comprises for the data hit 9 transmission lines sharing 5 pixels distributed every 9 pixels to equalize pixel hit rate and for the pixel address 5 transmission lines sharing 9 contiguous pixels.

Each transmission line is driven in current mode and is the input resistance of receiver.

The current driving is done by a differential switch that flips a current source when a hit is present. A second DC current source equalizes the DC current during steady state time. The current signal swing defining the logic level in coplanar waveguides has been specified to ±50µA, with a differential swing of 100µA. The far end sensing voltage is 10 mV for a receiver input resistance of 100Ω, about twice the odd characteristic impedance of the transmission line. This choice results from a trade-off between receiver biasing, line characteristic impedance and power consumption. The series resistance of the line varies from 6 Ω for one pixel distance to 300 Ω for 45 pixels distance (13.5 mm), making the maximum drop voltage 3 times the far end sensing voltage. However, this effect does not disturb signal discrimination because the far end amplitude does not change with the pixel to receiver distance thanks to the current drive operation.

The high series resistance of lossy transmission line in CMOS process has a strong impact to the signal integrity of the bus. It considerably degrades signal edge in slowing down rise time signal to about 1.5 ns after 13.5 mm signal propagation. To circumvent this effect a current pre-emphasis [6,7,8] is implemented in the line driver. The signal pre-emphasis is done by injecting a fast current pulse on the edges of the hit pulses. Figure 9 shows the efficiency of the technique.

Figure 8 Schematic of the bus system based on transmission lines

The bus system is on reference purpose in this simulation there is no pre-emphasis on trailing edge.

The waveguide is a RF coplanar cross coupled transmission line design is specified and characterized by IBM.

Cross coupled lines operates in anti-phase polarity and is characterized by the odd impedance.
3) End of column logic

The very low swing voltage imposes strong constraints on the sense amplifier design with the transmission line operating at a large bandwidth of several GHz. We have used an input stage similar to the NINO circuit [9] that senses the differential current with a differential common gate cascode stage and provides the termination of the transmission line. The schematic of the receiver is presented in Figure 10.

![Figure 9 schematic of the line receiver with its dynamic asynchronous comparator output stage providing extremely fast digital signal edges](image)

The receiver input stage biasing is provided directly by the static current of the transmission line of about 250 µA. The output of the receiver input stage is sensed with a broadband differential to single ended amplifier stage whose output is converted into a fast digital CMOS level signal by a dynamic asynchronous positive feedback latch comparator stage which generates pulses edges of 50 ps to drive TDC inputs.

4) End of column logic:

The end of column circuitry comprises one receiver bank (9 receivers, one for each transmission line), one TDC bank (9 TDC’s), address encoding circuits and the digital logic for processing the hit data ready for transmission off chip. For the prototype demonstrator the 32-bit DLL providing the 32 delayed clock signals for the hit registers in the TDC bank and one PLL providing a 320 MHz clock signal for the DLL are common to all end of line circuits. The TDC circuits used in the end of column logic is based on previous development done in 250 nm CMOS technology [10], and in 130 nm CMOS technology [11].

Each TDC consists of two 32-bit hit registers, one for the leading edge and one for the trailing edge of the hit, providing a double time stamping. The leading edge time stamp provides information of the hit arrival time and the trailing edge provides the additional input charge amplitude information needed to correct time walk.

The two 32-bit time stamps are encoded into 5-bit binary words. The double time stamp with coarse counter and address information are stored in a line buffer, which is then serialized and sent off chip.

Distributing DLL outputs to all the 40 columns is an issue as the load comprises 40 TDC banks and a long distance. This problem is solved by having in addition to a strong differential buffer at the output of the DLL a receiving buffer at the input of each TDC bank. The output of the DLL buffer is differential and is converted into single-ended only at the input buffer of each TDC bank. The hit registers use single-ended CMOS level signals. The hit register in the TDC are built of 32 D-type flip flops with rising edge trigger. The output of the receiver cell provides a rising edge trigger for both leading and trailing edge hit registers.

The EOC circuits are outside the beam area and thus the radiation levels are very low. Therefore it looks like there is no need to use digital circuits protected against SEU effects or leaking currents in NMOS devices. Also, as the sensitive analogue circuits are in the pixels and use different power supply as the isolated EOC circuits, there is no need to use differential logic.

![Figure 10 One end of column circuit as designed for the EOC demonstrator circuit](image)

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The clock frequency is 320 MHz resulting in a 3.125 ns period and a delay of a single delay cell of 97.66 ps.

EOC circuits have a very dense layout design since the receiver bank, the TDC bank and the digital circuits must fit inside a 300 µm pixel wide periphery of each column. The address bus has its own receiver bank (5 receivers, one for each address line) which provides the data required for the pixel address. All the data including the address and the time stamps are left non-coded in the demonstrator to give access to raw data.

In addition to the already mentioned circuits two trigger signals are generated from the hit signals to control the writing of data hit in the output line buffer.

VI. CONCLUSION

We have presented the challenges of ASIC development of the NA62 pixel Gigatracker and the current status of the circuit design of the pixel cells and bus system. Speed and noise specification are extremely challenging in terms of ASIC design. Two circuit demonstrators have been developed using complementary ASIC architectures which integrate TDC circuit in the pixel cell and in the end of column circuit. The demonstrator circuits will be submitted to fabrication end of 2008. Characterization of the demonstrators will help to select the best architecture and pixel cell. In particular timing performance and circuit robustness against digital noise are of the prime importance in the choice of the best approach.
REFERENCES

SPIROC (SiPM Integrated Read-Out Chip): Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM read-out.

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Abstract

The SPIROC chip is a dedicated very front-end electronics for an ILC prototype hadronic calorimeter with Silicon photomultiplier (or MPPC) readout. This ASIC is due to equip a 10,000-channel demonstrator in 2009. SPIROC is an evolution of FLC_SiPM used for the ILC AHCAL physics prototype [1].

SPIROC was submitted in June 2007 and will be tested in September 2007. It embeds cutting edge features that fulfill ILC final detector requirements. It has been realized in 0.35m SiGe technology. It has been developed to match the requirements of large dynamic range, low noise, low consumption, high precision and large number of readout channels needed.

SPIROC is an auto-triggered, bi-gain, 36-channel ASIC which allows to measure on each channel the charge from one photoelectron to 2000 and the time with a 100ps accurate TDC. An analogue memory array with a depth of 16 for each channel is used to store the time information and the charge measurement. A 12-bit Wilkinson ADC has been embedded to digitize the analogue memory content (time and charge on 2 gains). The data are then stored in a 4kbytes RAM. A very complex digital part has been integrated to manage all these features and to transfer the data to the DAQ which is described on [2].

After an exhaustive description, the extensive measurement results of that new front-end chip will be presented.

I. SECOND GENERATION SiPM READOUT: SPIROC

A. SPIROC: an ILC dedicated ASIC.

The SPIROC chip has been designed to meet the ILC hadronic calorimeter with SiPM readout [4]. The next figures (5 and 6) show an AHCAL scheme. One of the main constraints is to have a calorimeter as dense as possible. Therefore any space for infrastructure has to be minimized. One of the major requirements is consequently to minimize power to avoid active cooling in the detection gap. The aim is to keep for the DAQ-electronics located inside the detection gaps the power as low as 25 µW per channel.

Table 1: SPIROC description

<table>
<thead>
<tr>
<th>Technology</th>
<th>Austria-Micro-Systems (AMS) SiGe 0.35µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>32 mm² (7.2mm x 4.2mm)</td>
</tr>
<tr>
<td>Power Supply</td>
<td>5V / 3.5V</td>
</tr>
<tr>
<td>Consumption</td>
<td>25µW per channel in power pulsing mode</td>
</tr>
<tr>
<td>Package</td>
<td>CQFP240 package</td>
</tr>
</tbody>
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Figure 1: A half-octant of the HCAL

Figure 2: AHCAL integrated layer

Figure 3: SPIROC layout

The SPIROC chip is a 36-channel input front end circuit developed to read out SiPM outputs. The block diagram of the ASIC is given in Figure 4. Its main characteristics are given in Table 1.
C. SPIROC analogue core

A low power 8-bit DAC has been added at the preamplifier input to tune the input DC voltage in order to adjust individually the SiPM high voltage (see figure 5).

Two variable preamplifiers allow to obtain the requested dynamic range (from 1 to 2000 photoelectrons) with a level of noise of 1/10 photoelectron. Then, these charge preamplifiers are followed by two variable CRRC² slow shapers (50 ns-175 ns) and two 16-deep Switched Capacitor Array (SCA) in which the analogue voltage will be stored. A voltage 300 ns ramp gives the analogue time measurement. The time is stored in a 16-deep SCA when a trigger occurs. In parallel, trigger outputs are obtained via fast channels made of a fast shaper followed by a discriminator. The trigger discriminator threshold is given by an integrated 10-bit DAC common to the 36 channels. This threshold is finely tuneable on additional 4 bits channel by channel. The discriminator output feeds the digital part which manages the SCA. The complete scheme of one channel is shown on figure 6.

The ADC used in SPIROC is based on a Wilkinson structure. Its resolution is 12 bits. As the default accuracy of 12 bits is not always needed, the number of bits of the counter can be adjusted from 8 to 12 bits. This type of ADC is particularly adapted to this application which needs a common analogue voltage ramp for the 36 channels and one discriminator for each channel. The ADC is able to convert 36 analogue values (charge or time) in one run (about 100 µs at 40 MHz). If the SCA is full, 32 runs are needed (16 for charges and 16 for times).

E. Expected analogue performance

The new analogue chain in SPIROC allows the single photoelectron calibration and the signal measurement to be on the same range, simplifying greatly the absolute calibration. An analogue simulation of a whole analogue channel is shown in figure 7. It is obtained with an equivalent charge of 1 photoelectron (160 fC at SiPM gain 10⁶).

For the time measurement, the simulation shows a gain of 120 mV per photoelectron with a peaking time of 15 ns on the “fast channel” (preamplifier + fast shaper). The noise to photoelectron ratio is about 24 which is quite comfortable to trigger on half photoelectron.

For the energy measurement, the simulation gives a gain of 10 mV per photoelectron with a peaking time of about 100 ns on “high gain channel” (high gain preamplifier + slow shaper). The noise to photoelectron ratio is about 11 and should be sufficient for the planned application. On the “low gain channel”, the noise to photoelectron ratio is about 3 and it meets largely the requirement.

D. Embedded ADC

The system on chip has been designed to match the ILC beam structure (figure 8). The complete readout process needs at least 3 different steps: acquisition phase, conversion phase, readout phase, and possibly idle phase.
In the memory in order to start a new one for the next column. When these 72 conversions are over, data are stored in the active analogue memories in each front-end chip during the beam train. An external signal is available to erase the columns if a trigger was due to noise.

- **Acquisition mode**: During the acquisition mode, the valid data are stored in analogue memories in each front-end chip during the beam train. An external signal is available to erase the active column named “No_Trigger”. It can be used to erase the column if a trigger was due to noise.

![Figure 8: SPIROC running modes](image)

- **Conversion mode**: Then, during the conversion mode, the data are converted into digital before being stored in the chip SRAM by following the mapping represented in figure 10. The 36 charges and 36 times stored in SCA are converted for each column. When these 72 conversions are over, data are stored in the memory in order to start a new one for the next column.

The Bunch Crossing Identifier (BCID), hit (H) channels and gains (G) are also saved into RAM.

![Figure 9: Operation of Track and Hold](image)

- **Readout mode**: Finally, during the readout mode, the data are sent to DAQ during the inter-train (20kbits per ASIC per bunch train). The readout is based on a daisy chain mechanism initiated by the DAQ. One data line activated sequentially is used to readout all the ASIC on the SLAB.

![Figure 11: Detector readout scheme](image)

- **Idle mode**: When all these operations are done, the chip goes to idle mode to save power. In the ILC beam structure 99% of power can be saved.

The management of all the different steps of normal working (acquisition, A/D measure and read-out) needs a very complex digital part which was integrated in the ASIC [3] (see on the figure 12).

![Figure 12: Interaction between digital and analog part](image)

**G. Power pulsing**

The new electronics readout is intended to be embedded in the detector. One important feature is the reduction of the power consumption. The huge number of electronic channels makes crucial such a reduction to 25 μWatt per channel using the power pulsing scheme, possible thanks to the ILC bunch pattern: 2 ms of acquisition, conversion and readout data for 198 ms of dead time. However, to save more power, during each mode, the unused stages are off.

**II. MEASUREMENTS**

**A. 8-bit input DAC performance**

The input DAC span goes from 4.5V down to 0.5V with a LSB of 20 mV. The default value is 4.5V in order to operate the SiPM at minimum over-voltage when the DAC is not loaded. The linearity is ±2% (5LSB), just enough for the SiPM operation but consistent with the allocated area. Also,
the dispersion between channels, although not fundamental could also be improved. The power dissipation is well within the specs and the 100nA bias current to $V_{dd}$ makes the chip difficult to measure without special precautions.

\[ \text{Figure 13: 8-bit DAC linearity} \]

**B. Trigger and gain selection 10-bit DAC measurement**

The linearity for the two thresholds DAC was checked by scanning all the values and measuring the signal for each combination. The figure below gives the evolution of the signal amplitude as a function of the DAC combination. By fitting this line in the region without saturation (up to thermometer = 10), we obtained a nice linearity of ± 0.2 % on a large range.

\[ \text{Figure 14: Trigger and gain selection 10-bit DAC linearity} \]

**C. Charge measurement**

Waveforms were recorded with a fixed injected charge of 100 fC and for variable preamplifier gains as one can see on the Figure 15 which represents the amplitude as a function of time for different gains.

\[ \text{Figure 15: High gain slow shaper waveforms for a fixed injected charge of 160 fC and different preamplifier gains.} \]

\[ \text{Figure 16: 1/V_{out} versus C_f (preamplifier gain capacitance)} \]

From these measurements the linearity of the charge output as a function of the gain was calculated to be around ±1 % (see figure below).

The next figure represents the high gain output signal amplitude as a function of the injected charge. The fit to the linear part of the curve is better than 1%.

\[ \text{Figure 17: High gain slow shaper linearity} \]

We also looked at the cross-talk on the slow shaper path. Figure 17 represents the waveforms of a channel 8 and its neighbours for an injected charge of 15 pC. The amplitude of the neighbouring channels is multiplied by 100. The calculation of maximum ratio gave a cross-talk of less than 0.3%. Figure 18: Cross talk.
The photoelectron to noise ratio of 4 allows to nicely resolve the single photoelectrons peaks. The next figure shows the single photoelectron spectrum.

**Figure 19**: SiPM spectrum

### D. Time measurement

Well known S-curves were also studied. They correspond to the measurement of the trigger efficiency during a scan of the input charge or the threshold while the other parameters, like the preamplifier gain, are kept constant. Figure 20 represents the trigger efficiency as a function of the DAC values for the 36 channels of a single chip. All channels were set at $C_f=0.2pF$ and the input signal was fixed at $Q_{inj}=50fC$. We obtained 100% trigger efficiency for an input charge of approximately 50 fC which corresponds to 1/3 pe as requested.

**Figure 20**: 36 channels S-curves

Figure 21 represents the evolution of the 50% trigger efficiency as a function of the injected charge.

**Figure 21**: 50% trigger efficiency input charge versus applied threshold for a single channel and a fixed preamplifier gain

The maximum time amplitude between small and large signal is about 10 ns.

**Figure 22**: Time walk

### III. Conclusion

The SPIROC chip has been submitted in June 2007 and its test started in October 2007. It embeds cutting edge features that fulfill ILC final detector requirements including ultra low power consumption and extensive integration for SiPM readout. The system on chip is driven by a complex state machine ensuring the ADC, TDC and memories control.

The SPIROC chip is due to equip a 10,000-channel demonstrator in 2009 in the frame work of EUDET.

### IV. References

[1] LC-DET-2006-007: Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM readout

S. Blin$^1$, B. Dolgoshein$^3$, E. Garutti$^1$, M. Groll$^2$, C. de La Taille$^6$, A. Karakash$^1$, V. Korbel$^1$, B. Lutz$^1$, G. Martin-Chassard$^5$, A. Pleshk$^3$, L. Raux$^1$, F. Sefkow$^1$

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[4] System aspects of the ILC-electronics and power pulsing

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A Readout ASIC for CZT Detectors

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Abstract

Spectrometers that can identify the energy of gamma radiation and determine the source isotope have until recently used low temperature semiconductors. These require cooling which makes their portability difficult. The material Cadmium Zinc Telluride (CZT) is now available which operates at room temperature and can be used to measure the energy of gamma radiation. In a Compton camera configuration the direction of the radiation can also be determined. A read-out ASIC has been developed for such a system and features 100 channels of electronics, each with a charge amplifier, CR-RC shaper, and peak-hold. A 12 bit ADC converts the data which is sparsified before being read out. The energy, signal rise time, and timestamp of any hit channel is read out together with the data from all of its neighbours. The ASIC has a selectable lower dynamic range which could be used for lower energy interactions.

I. THE ASIC

A. Overview

A portable gamma camera has been developed which will be used to detect both the position and isotope of material emitting gamma radiation. As part of this, a layered and pixellated CZT detector has been designed. Battery powered, the detector requires low power and low noise read-out electronics to detect and process the generated charge before it can be developed into an image.

Figure 1 shows a top level representation of the ASIC. The CZT detector is a 10x10 pixellated array which is gold stud bonded to a daughter card. The 100 channel read-out ASIC is wire bonded to the card and is DC connected to the detector via board routing. Within the ASIC are 100 channels of charge read-out and processing electronics (which can be stimulated using a calibration circuit), a 12 bit ADC, digital control logic, and bandgaps and voltage reference circuits. The ASIC is loosely based on the Nucam ASIC, a 128 channel read-out chip for CdTe Detectors [1-2].

Gamma radiation incident on the CZT detector generates charge proportional to the energy deposited. This charge is then read from the detector and processed by the ASIC. For every event above a defined energy level (the threshold is externally adjustable) the ASIC stores the channel number, amplitude, charge collection time, and the event time in digital form. Readout is data driven, and when data becomes available it is transmitted off-chip. Since charge generated within the CZT detector may be shared between several neighbouring pixels, data from these pixels is also read out as part of the same event.

Read-out from the chip through the Data Output is 1 bit serial and data driven. When data becomes available, the Data Valid signal goes high for the length of time the data is output. The data transfer speed is 32MHz and a data packet consists of 34 bits. Consecutive data packets are output without a break in the Data Valid signal or the Data Output.

There is no communication between read-out ASICs in the system. Each is wired point-to-point to an FPGA on the mother board. Therefore each ASIC must be addressed separately, and has a 5-bit hardwired address that is used when programming the on-chip control registers via the I2C-type interface. In addition, there is a channel mask register to mask any faulty channels from triggering the read-out logic.

B. Electronics

Figure 2 shows a block diagram of the electronic components which make up each channel of the ASIC, together with the on-chip read-out circuitry and control logic.
There are two branches to note. The analogue chain from input to output comprises of: Preamplifier, CR-RC Shaper, Peak-Hold, Analogue Multiplexer, ADC. In addition there is a second branch which comprises of: Differentiator, Comparator, Counter. These two branches will be explained below.

![Block Diagram of Electronics](image)

**C. Analogue Readout Channel**

1) **Charge Amplifier**

The preamplifier takes the charge generated within the detector and integrates it on a feedback capacitor to give a voltage. The charge to voltage gain is inversely proportional to the size of the feedback capacitor of which there are two sizes available. This is to allow two different input ranges. The largest capacitance gives an input range of approximately 400 000 electrons. The second gives an input range of 80 000 electrons and could be used with lower energy interactions. These two settings are accessed through the I²C interface.

The preamplifier has a leakage current compensation circuit [3] which can source a current of up to 150nA from the input of the preamplifier to the detector. The circuit also acts as a DC stabilising feedback across the preamplifier and also ensures the output from the preamplifier returns to its zero signal level thus avoiding pile-up saturation.

![Effect of Feedback Bias on Preamp & Shaper](image)

The rate at which this returns to zero depends on the bias current supplied to the leakage current compensation circuit (figure 3), and this is selectable from 0.25nA to 4nA using the I²C interface. This bias current affects the electronic noise of the preamplifier, with the lowest bias setting giving the lowest noise.

2) **Shaper**

The shaper is used to filter noise, improve two pulse resolution, and provides a convenient voltage pulse shape for processing. The form of shaping is a variable time constant CR-RC which can be programmed via the I²C interface. There are 4 bits of resolution, allowing shaping times from 0.5μs up to 7.5μs.

The amplitude of the voltage pulse from the shaper is proportional to the energy of the ionising event in the detector. The lowest energy that will be detected by the chip is defined by a comparator which is connected to the shaper output and to an external threshold voltage. When the shaper output voltage exceeds the threshold voltage, a digital signal is generated by the comparator which defines the event as a hit and the signal is processed and read out from the chip.

3) **Peak Hold**

The peak amplitude of the shaper output needs to be held long enough for the ADC to sample its value - signals arriving from the detectors by their very nature are random and asynchronous, while the ADC runs at a fixed sampling frequency. For this reason the peak value of the shaper voltage needs to be held until the hit has been detected and the ADC has sampled its value.

4) **Analogue Multiplexer**

Between each channel and the ADC is the analogue multiplexer. This circuit directs the output from the peak hold circuit onto the ADC input for each channel that has detected a hit. It runs continuously (provided there are events to read out) at the same sampling frequency as the ADC.

5) **Analogue-to-Digital Converter**

The ADC is a 12 bit converter, fully pipelined, and employing a fully differential architecture. It runs at a sample rate of approximately 0.94 MSamples/s. This value comes about due to the fact that the chip outputs a 34 bits frame of data at a clock rate of 32MHz, and the ADC is synchronised to the frame rate, which is 32/34 MHz.

**D. Rise Time Measurement**

A measure of the depth of interaction of the gamma radiation within the detector can be determined by measuring the charge collection time [4]. This is done by measuring the rise time of the preamplifier output. To achieve this, the preamplifier output is differentiated to give a pulse whose width is proportional to the rise time (figure 4). A comparator then cleans this signal up and is used to gate the clock of a counter to give a digital representation of the rise time.
By its very nature, differentiating an analogue signal is intrinsically noisy. Therefore, instead of using a standard differentiator circuit, some noise filtering was achieved by using a band-pass filter with very fast time constants. The output of the differentiator comparator was also used to generate a timestamp of when the signal occurred.

E. Digital Control Logic

The digital control logic performs several functions, by far the most complicated part comprises the Nearest Neighbour Logic. In addition, there are other functions and these are listed in the following sections.

1) Clock Division

The ASIC has a 32MHz clock input. However several different clock frequencies are required on-chip. The rise time measurement has a selectable 16 or 32MHz. The timestamp has a selectable 1,2,4 or 8MHz clock.

2) Data Synchronisation

The output from the ADC has to be synchronised with the outputs from the timestamp and the rise time circuits before being transmitted off chip. This is done using a bank of flip-flops.

3) Data Sparsification

Only data corresponding to hit pixels and their neighbouring pixels are readout. The control logic keeps the analogue data stored on the peak hold circuit until it can be read out through the analogue multiplexer. The multiplexer is synchronised to the ADC sample rate which is 0.94MHz.

4) Time Stamp Verification

If several ASICs are being used in a system it is necessary for them to remain in synchronisation with respect to the time stamp. To ensure this an extra channel (channel 0) has been reserved for time stamp verification. Channel 0 does not connect to any of the detector pixels, but during operation of the ASIC, the calibration circuit is programmed to point to channel 0. A calibration pulse can then be sent to all ASICs and the time stamp read out from all channel 0’s can be monitored.

5) Nearest Neighbour Logic

The charge generated by an ionising event within a pixel in the detector may be shared with the neighbouring pixels. This charge may be below the threshold set for registering as a hit and would otherwise be lost. To overcome this, the readout ASIC has been designed with nearest neighbour readout. The mapping of detector pixel to readout channel is shown in figure 5. This is hardwired into the ASIC and cannot be reconfigured.

When a pixel has a signal over threshold (hit), for example pixel 55 in fig. 5, then pixels 45,54,55,56 and 65 will all be read out. A “hit bit” in the data stream from the chip indicates which of the pixels registered the initial hit above threshold.

F. Interface & Control Registers

Using the I2C type interface it is possible to access the on-chip registers and to modify their default settings. There are two registers, and each register can be written to or read from via the interface. Table 1 shows the functions controlled by the two registers.

Table 1. Control Registers

<table>
<thead>
<tr>
<th>Bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Preamp</td>
<td>Shaping Time</td>
<td>Leakage Comp.</td>
<td>Bias</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REG 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REG 2</td>
<td>Rise</td>
<td>Time</td>
<td>Stamp</td>
<td>Chip Bias Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
G. Data Output Format

When data becomes available it will be immediately output from the chip, via a single serial output (LVDS). A data frame is 34 bits in length (figure 6) and contains the channel address (7 bits), the time stamp (8 bits) a hit bit (1 bit), the rise time measurement (6 bits) and the amplitude measurement (12 bits).

The channel address can range from 0 to 100, with channels 1 to 100 being the detector channels, and channel 0 used for time stamp verification. The hit bit identifies the event as occurring in that channel, in which case it is set high. If set low, the hit bit indicates the channel to be one neighbouring that in which the event occurred.

II. READOUT SYSTEM

As mentioned previously, the CZT detector is gold stud bonded onto a daughter card (figure 7) and the readout ASIC wire bonded to the daughter card.

Several daughter cards then connect to a mother board via flexible connectors. The mother board contains the FPGA used to control the ASICS and for data acquisition. Several daughter cards are aligned to form a compton camera.

III. STATUS

The present status of this project is that two versions of the ASIC have been fabricated on a standard 4-metal 0.35μm process (figure 8). The first version has been extensively tested. However, due to an error in the ADC which caused large blocks of missing code, the ASIC can not be used in a full compton camera system to image gamma radiation. However, all other functions of the ASIC were found to be operating.

Figure 6: Output Data Format

Figure 7: Daughter Card

Figure 8: Fabricated ASIC

Figure 9: Test of Nearest Neighbour Read-out

Figure 10: ADC Transfer Curve
Figure 10 shows the transfer characteristic of the 12-bit pipelined ADC on the first version of the chip. The non-linearity and blocks of missing code are caused by timing errors within the ADC. The cause of these errors is fully understood and has been corrected on the second version of the ASIC.

IV. CONCLUSIONS

A read-out ASIC for CZT detectors has been fabricated and tested. Tests have confirmed basic functionality but have also revealed problems due to a faulty ADC.

A second iteration has been fabricated and is undergoing testing. Initial tests have confirmed that the fault in the ADC has been corrected.

V. REFERENCES


Status Report on the LOC ASIC

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Abstract

Based on a commercially available 0.25 \(\mu\)m Silicon on Sapphire CMOS technology, we are developing the LOC ASIC for high speed serial data transmission in the front-end electronics systems of the ATLAS upgrade for the SLHC\(^1\). Evaluation of this technology for applications in the SLHC, based on a dedicated test chip, has been performed with irradiation tests in gamma (Co-60) and in 230 MeV proton beams. Test results indicate that this may be a candidate technology of ASIC developments for the SLHC. More thorough evaluation tests will be carried out under another R&D program supported through the Advanced Detector Research (ADR) from the Department of Energy. Characterization tests on the first prototype serializer, LOC1, have been carried out in lab. Based on the lessons learned from this chip, we propose a new architecture design of the second prototype, LOC2, aiming for a serial data rate in the range of 5 Gbps. Simulation on key components of LOC2 are being carried out and the results we have so far are presented in this note. LOC2 is scheduled to be submitted for fabrication in the first half of 2009.

I. INTRODUCTION

Detector and its readout system upgrades for the high luminosity upgrade of the LHC (SLHC) call for higher bandwidth optical links that withstand higher radiation levels. R&D activities for ATLAS Liquid Argon Calorimeter readout upgrade have taken place for several years. In this R&D program, we propose the LOC (link-on-chip) ASIC as a serializer based on a commercially available 0.25 \(\mu\)m Silicon on Sapphire (SOS) CMOS technology. The initial idea was to integrate “everything” into one chip, including the optical interface. Fiber would be coupled directly to the chip to spare high speed copper traces on the PCB. This project started out with the SOS technology evaluation. This work produced encouraging results which indicate that this technology may be a candidate of ASIC developments for the SLHC. More thorough evaluation tests grow out of the scope of the present R&D work for the ATLAS upgrade, and hence are to be carried out under another R&D program supported through the Advanced Detector Research (ADR) from the Department of Energy. The first prototype serializer, LOC1, was designed with collaborative effort between the electrical engineering and the physics departments at SMU. This first prototype provided valuable information on key components, especially the PLL and the serializer structure, for the LOC2 design. The second prototype, LOC2, is the one to be reported in detail in this note.

We begin our report on the SOS technology evaluation in radiation environment, in section II. In section III we briefly report the test results on LOC1. In section IV, we outline the design considerations for LOC2, based on lessons learned from LOC1. We also present the simulation results we have so far on key components of the LOC design. These simulation results indicate that a 5 Gbps serial data rate is hopeful. Conclusions and acknowledgements are in section V.

II. EVALUATION OF THE SOS TECHNOLOGY IN RADIATION ENVIRONMENT

The Silicon on Sapphire technology has been a choice for radiation tolerant electronics since the 1970s. With the insulating sapphire substrare, this technology eliminates the parasitic transistor in the bulk silicon substrate and hence removes the mechanism for circuit latch-ups. This insulating substrate also reduces the possibility of single event upset (SEU) because charged ions cannot travel as far in the components as in bulk silicon substrate [1, 2]. The only limiting factor of this technology in the past was that it was difficult to achieve high yields in volume production thus this technology was limited to very specialized applications in military and space programs. In the early 1990s, semiconductor manufacturers solved the problem of crystallization defects in silicon grown on sapphire [3] and brought this technology to market through the same equipment for the bulk silicon CMOS process. Thanks to the fast expansion in the wireless and broadband markets, the SOS technology, which finds a lot of applications in RF and mixed signal circuits there, is on a fast-growing path.

In order to evaluate this technology for ASIC developments for the SLHC, we designed a dedicated test chip in collaboration with the electrical engineering department at SMU, and conducted irradiation tests on the total ionization dose (TID) effect and the single event effect (SEE). A picture of this test chip is shown in Figure 1. The TID effect was measured through transistor I-V curves with the transistor array in the test chip. The SEE was measured with dynamic data transfer through the shift registers in the test chip under irradiation. Detailed report on this work has been published elsewhere [4]. We only summarize the key results here.

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\(^1\) The work reported in this note is supported by the US-ATLAS for the high luminosity upgrade of the LHC.
A. The total ionization dose effect

The TID tests were carried out with gamma irradiation (Co-60). The chip substrate was grounded during irradiation. Transistor I-V curves were measured repeatedly while the test chip was under irradiation. Radiation induced leakage current and threshold voltage changes were plotted as a function of total accumulated dose. The results are shown in Figure 2.

![Figure 2: Irradiation induced leakage current and threshold voltage change as a function of total ionizing dose. Plotted in a) are for the NMOS transistors, b) for the PMOS.](image)

There is almost no leakage current change measured. The small threshold voltage change happened at the very beginning of the irradiation and then remains almost unchanged with the increase of the total dose. This change is within the technology variation and is considered acceptable in ASIC designs.

B. Single event effect

Single event effect was measured through online monitoring of the data bits shifted through registers and logic latches in the test chip under irradiation of a 230 MeV proton beam with a flux of $7.7 \times 10^8$ proton/cm$^2$/s. No error was observed before, during and after the irradiation periods. The zero error result is translated into a cross section upper limit of $5.6 \times 10^{-15}$ cm$^2$ for all four tested units (standard layout shift registers, enclosed layout shift registers, resistively hardened shift registers, and latches).

We concluded from these tests that this technology may be a good candidate for ASIC development for SLHC and we decided to use it in our LOC development.

III. LOC1 TEST RESULTS

The first prototype serializer, LOC1, was designed in collaboration with the electrical engineering department at SMU. In this prototype, we planned to check four key components: the serializing unit, the PLL and clock unit, the electrical output CML driver and the VCSEL driver. Shown in Figure 3 is the block diagram of LOC1. A self-biasing PLL was chosen for the high speed clock generation. This choice was made based on this PLL’s good noise rejection and wide tuning range. Self-biasing PLL also has the reputation of independent of manufacturing process [5]. We measure a tuning range of the PLL in LOC1 from 0.8 to 2.4 GHz with a random jitter of about 4 ps at 1.25 GHz. Choice of static D-flip-flop for SEE immunity consideration led to a four-arm 5:1 shift serializer with two stage 2:1 multiplexer structure for the serializing unit. This design turned out to be a major source of the deterministic jitter (DJ) in the output serial bit stream. The CML driver did not work to the design specification but good enough for us to conduct measurements of this chip. We did not succeed in the VCSEL driver design.

![Figure 3: Block diagram of LOC1. Solid line boxes are implemented in the ASIC, dashed line boxes are implemented in FPGA for testing purposes.](image)

An eye diagram with a $2^{27}-1$ pseudo random input is shown in Figure 4. The data rate is 2.5 Gbps. Large DJ is observed and traced back to the serializing unit. This problem will be corrected in future designs.

![Figure 4: Eye diagram from LOC1 output with $2^{27}-1$ pseudo random input.](image)
A bit error rate bathtub curve at 2.5 Gbps is also measured. The best BER reached \(10^{-11}\), indicating the digital logic in LOC1 is correct.

Valuable lessons are learned in the LOC1 design and testing. This helps in our LOC2 design.

IV. DESIGN CONSIDERATIONS IN LOC2 AND SIMULATION RESULTS

In the process of the LOC development, several common projects at CERN have started to develop ASICs and subsystems for the SLHC upgrade. Among them the most relevant project, of which we are a collaborator, is the Versatile Link project. Please see reports on the Versatile Link in the joint ATLAS-CMS opto-electronics working group session in this conference. We decide to move the optical interface of the LOC ASIC into the Versatile Link and concentrate on the serializer design. On the input of LOC, we also realize that it is impossible to have one input interface that meets with demands from the upstream electronic systems from both ATLAS Inner Detector and Liquid Argon Calorimeter. With this we now re-define the LOC as a 16:1 serializer chip or function block, with CML output to be connected to the transmitter part of the Versatile Link. We move the user interface function, together with the framing/encoding function into another chip or function block. For the second prototype, LOC2, this is the combination of the two function blocks with some configure and control unit. This is shown as block diagram in Figure 6.

![Figure 6: LOC2 block diagram (in dashed line box). The output of LOC2 connects to the Versatile Link.](image)

The core part of the LOC ASIC, the 16:1 serializer can now be implemented as shown in Figure 8. The logic structure is then much simpler than a 20:1 serializer. The fundamental structure in the serializing unit is two D-flip-flops and a 2:1 MUX. In this cascade structure, only the last stage of the 2:1 multiplexing runs at 2.5 GHz for a 5 Gbps serial data output. Effort can then be concentrated on this stage to maximize the speed. The clock fan-out unit is also simplified to a “divide-by-2” chain. The key components in this design are the 2.5 GHz PLL, the static D-flip-flop and the final CML driver that works at 5 Gbps. In the following we will present the simulation results we have on some of the key components.

First of all, we used a simple inverter to adjust the PMOS/NMOS transistor ratio to equalize the delay from logic 1 to 0 and from 0 to 1. This ratio is found to be \(n(1.9/1.4)\), where \(n = 1, 2, 3, \ldots\). Both basic and multi-finger layouts are checked to maximize the speed. The delay of an inverter, when driving itself, is found to be 32 to 35 ps, corresponding to a frequency of about 30 GHz. This is comparable with speeds achieved in 0.13 to 0.15µm bulk silicon CMOS technology. For a comparison, we made a simulation of the same inverter in a 0.25µm bulk silicon CMOS technology and found that the delay time is 60 ps under the same condition, about a factor of 2 slower than the SOS CMOS technology.

Simulation on the D-flip-flop (DFF) started out with the C6MOS type as used in the GOL ASIC [6], but we soon moved to the TGDFD which is about 20% faster than the C6MOS DFF, and has at least the same SEE immunity [7]. Different transistor size, single and multi-finger layouts have been checked to minimize the delay or maximize the speed. The minimum decay is found to be 292 ps in the slowest (the SS corner) case. This indicates a 5 Gbps serializer possible because the time needed for the basic unit (DFF+MUX) is 400 ps.

The design work on the PLL and the CML driver is in progress and will have to be reported at a later time.
V. CONCLUSIONS AND ACKNOWLEDGMENTS

The LOC ASIC design evolves with time. We incorporate into our LOC design the development from the Versatile Link project and decide to move the optical interface from the LOC to the Versatile Link. The LOC now is proposed to be a 16:1 serializer as its core part. Different interface ASICs or function blocks will be developed according to the application of the LOC.

Technology evaluation on the 0.25µm SOS technology produced encouraging results and enables us to go ahead with the LOC design using this technology. More studies will be performed on this technology with support from the ADR program.

The design work for the present prototype, LOC2, is in progress. Simulations on critical components indicate that a 5 Gbps serial data rate is hopeful.

We would like to thank the US-ATLAS program which provides funds for this R&D effort. We also would like to thank many of our colleges who have been helping us in many ways in this project. The whole project benefits tremendously from the CERN GOL ASIC design. We would like to thank many people in the CERN microelectronics group, especially to Paulo Moreira for his very kind help in the LOC project. We also would like to thank Jim Kierstead at BNL and Ethan Cascio at MGH’s NPTC for their help in irradiation tests.

VI. REFERENCES


Evaluation of Two SiGe HBT Technologies for the ATLAS sLHC Upgrade


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Abstract

As previously reported, silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) technologies promise several advantages over CMOS for the front-end readout electronics for the ATLAS upgrade. Since our last paper, we have evaluated the relative merits of the latest generations of IBM SiGe HBT BiCMOS technologies, the 8WL and 8HP platforms. These 130nm SiGe technologies show promise to operate at lower power than CMOS technologies and would provide a viable alternative for the Silicon Strip Detector and Liquid Argon Calorimeter upgrades, provided that the radiation tolerance studies at multiple gamma and neutron irradiation levels, included in this investigation, show them to be sufficiently radiation tolerant.

I. INTRODUCTION

SiGe technologies are known for their high transconductance at low current. BiCMOS Silicon-germanium (SiGe) Heterojunction Bipolar Transistor (HBT) technologies are of interest for high luminosity applications in high energy physics because they have the benefit of requiring less power than standard CMOS technologies while still having low noise and fast shaping times even after exposure to high radiation levels [1]. The silicon microstrip detector and the liquid argon calorimeter for the ATLAS upgrade present rather large capacitive loads to the readout electronics (Si Strip Tracker: 5 pF to 16 pF; LAr: 400 pF to 1.5 nF). In order to maintain shaping times in the tens of nanoseconds, CMOS front-ends must increase bias currents to establish large enough transconductance. However, the extremely low base resistances of SiGe HBTs can accomplish this with relatively low bias currents thus affording possible power reduction. Their low base resistance also minimizes the intrinsic base resistance noise allowing a good signal-to-noise ratio.

Prototype readout circuits using the IBM’s 8WL SiGe HBT technology are currently planned for submission. The prototype circuits are designed to explore their possible use in the upgrade of the Silicon Strip Detector and Liquid Argon Calorimeter of the ATLAS detector as part of the Large Hadron Collider upgrade (sLHC) [2][3]. In these applications, power consumption is a critical parameter, which must be minimized. These preliminary circuit designs have been used to guide the assessment of relevant device parameters. The design of a low noise amp (LNA) with SiGe 8WL technology is presented.

In order to determine if SiGe technologies can survive the radiation environment of the upgraded ATLAS detector, an investigation was made to assess the radiation hardness of the two latest generation IBM SiGe platforms, 8WL and the 8HP. This is a follow up to a previous paper from this 2005 conference where only very early results were presented [4]. Previous IBM SiGe generations have already been reported to be quite radiation tolerant up to a high dose, showing post-radiation current gains well above workable limits [5][6][7]. Compared to 8HP, 8WL is a lower cost option, with 100 GHz peak fT versus 200 GHz for 8HP, and has reduced depth deep trench isolation, a thinner, implanted sub-collector, and a higher resistivity substrate. Both are available with a 130 nm CMOS technology to provide high-speed BiCMOS ASIC solutions.

This radiation study envelopes the predicted target radiation levels that will be reached at 60 and 20 cm radii in the upgraded ATLAS detector. There are no firm specifications yet for radiation levels, but based upon the simulation studies [8] and the working “strawman layout” [9], and consistent with the radiation levels to which the silicon sensor group is testing, we are presently targeting the following values (which include one safety factor of 2). For the silicon strip detector the current studies predict 30 Mrad(Si) of total ionizing dose (TID) and 6.8 x 10^15 cm^-2 1 MeV equivalent neutron fluence in the “short-strips” region, and 8.4 Mrad(Si) - 3.2 x 10^14 cm^-2 in the “long-strips” region, while the radiation levels for the liquid argon calorimeter (LAr) are expected to be in the order of 300 Krad(Si) total ionizing dose (TID) and a total 1 MeV equivalent neutron fluence of 9.6 x 10^17 cm^-2.
II. PROTOTYPE CIRCUITS

Three Integrated Circuits (ICs) are being designed to be submitted for fabrication in the 8WL, IBM’s SiGe 0.13 µm BiCMOS technology: a SiGe Silicon Tracker prototype readout test chip (SGST), a prototype LAr preamplifier and shaper, and a test structures chip.

The differences between the 8WL and the 8HP technologies are mainly that the 8WL is a cost-performance platform (100 / 200 GHz peak $f_T$ / $f_{max}$ vs. 200 / 285 GHz for 8HP); with much shallower implanted sub-collector versus a thicker epitaxially grown sub-collector in the 8HP technology; a lightly doped substrate (~ 40-80 Ω·cm vs. 8-10 Ω·cm for 8HP); and a “shallow” deep trench isolation (~ 3 µm vs. 8 µm for 8HP) [10]. A schematic cross-section of the two technologies can be seen in Figure 1.

A. Silicon strips tracker prototype

The general circuit schematic of the SGST can be seen in Figure 2. For the SGST the main circuit development goal is to minimize power and meet the SCT noise and 25 ns crossing specs. Threshold and bias adjustment for device matching skew is included in the design, using a different strategy than ABCD or ABCNext ICs, for lowered power rail to 1.2 V. Resistive front transistor feedback is used to reduce shot noise from a feedback current source. The size of this resistor is now optimized for long strips and may need a different optimization for a short strip load. The design allows the shaping time to be adjustable over a +/-15% range. Overall, SiGe allows significant current reduction in each analog stage as compared to 0.13 µm CMOS.

Two detector loads have been simulated, including strays, one of 5.5 pF for $V_T = 0.5$ fC and the other of 16 pF for $V_T = 1$ fC. This corresponds to 2.5 cm and 10 cm detector strip lengths. Although a final pure CMOS design is needed to quantify the power difference, as a result of the simulations the SGST prototype IC will consume 0.2 mW per channel for long-strips type load. This sets a comparison point with the CMOS prototypes being developed. Figure 3 shows the simulations results for the equivalent noise charge (ENC) at different circuit biases and for the interesting range of detector loads. The simulations include 600 nA of detector leakage. In Figure 4 can be seen that the 27 ns simulated impulse response at comparator for a 5.5 pF load meets SCT time walk specification of 15 ns for 1.25 fC to 10 fC signal interval. Nevertheless, the chip DAC shaping time adjustment allows tuning of the time walk desired, so that minimal extra power is used to overcome 8WL process variations.

B. Liquid Argon Calorimeter Prototype

A block diagram of the LAr front-end readout architecture can be seen in Figure 5 (top) together with a view of the chiplet design (bottom).

The preamplifier is based on the “super common base” architecture as is the one presently installed in the LAr front-end boards (FEB) [11]. Thanks to the SiGe low spreading base resistance it employs an input transistor of manageable size (emitter length 4x20 µm, 2 emitter stripe geometry) biased at 8 mA collector current. The preamplifier achieves an overall equivalent series noise of 0.26 nV/√Hz, while dissipating 42 mW. In the present prototype the fully
differential shaping stage is divided into two gain ranges, each dissipating about 100 mW. A fully differential gain x10 low noise stage amplifies the preamplifier signal for the high gain branch to limit second stage noise.

A third chip will be fabricated containing test structures of the 8WL technology. Standard design-kit devices are introduced, including individual SiGe bipolar transistors, configured in differential pairs, and resistors. The test chip also incorporates a pure CMOS test structure designed by the CERN Micro Electronics Group for the IBM 0.13 µm CMOS 8RF technology that has been ported to the 8WL technology for direct comparison of the CMOS modules of both technologies. A description of the composition of the bipolar section of the test structure can be seen in Table 1.

### III. Radiation Studies

Two IBM 0.13 µm BiCMOS SiGe technologies, the 8HP and the 8WL, are being evaluated for radiation hardness using “spare” test chips from IBM, until we have the newly designed test chip at our disposal. Gamma irradiations have been performed at the Brookhaven National Laboratory (BNL), USA. Three different total doses have been reached: 10, 25, 50 Mrads(Si). Neutron irradiations have been also performed in the TRIGA Nuclear Reactor, of the Jozef Stefan Institute in Ljubljana, Slovenia and also in the Fast Neutron Irradiation (FNI) Facility in the University of Massachusetts Lowell Research Reactor, USA. The 1 MeV neutron equivalent fluences reached are: $2 \times 10^{14}$, $6 \times 10^{14}$, $1 \times 10^{15}$, and $2 \times 10^{15}$ cm$^{-2}$. Gamma irradiations have been performed both with the devices shorted and biased in the forward active region, while for the neutron irradiations the devices had all their terminals shorted together. Cadmium shielding has been used in the neutron irradiations at the nuclear reactor in order to avoid excess damage from thermal neutrons [12].

The effects of both neutron and gamma irradiations on the characteristics of the SiGe bipolar transistors are an increase of the base current ($I_b$), which produces a reduction in the common emitter current gain ($\beta = I_C / I_B$). This base current increase has a strong dependency on the injection level in the transistor, as a result the performance degradation of the transistors is much more severe at lower collector currents than at higher currents, as can be observed in the example plot in Figure 7.

![Figure 5: LAr chiplet 1.8 mm$^2$, 2 preamp & shaper channels](image)

As in the present generation the shaper employs a CR-(RC)$^2$ transfer function. Including second stage noise, the front-end readout has an input-referred noise to signal, ratio ENI=72 nA rms, about 28% lower than the current generation.

Figure 6 shows simulation results, for a 0.5 mA to 5 mA range of LAr input current. The linearity is better than 0.2% over the full dynamic range.

![Figure 6: LAr circuit prototype response for Pre-Amp (PA), and Shaper after integration, (RC)$^2$, and at output (RC)$^2$.](image)

### Table 1: Composition of the radiation test chip

<table>
<thead>
<tr>
<th>Device</th>
<th>Dimensions</th>
<th>Quantity (pairs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiGe bipolar transistor</td>
<td>1 x 0.12 µm$^2$</td>
<td>4</td>
</tr>
<tr>
<td>SiGe bipolar transistor</td>
<td>8 x 0.12 µm$^2$</td>
<td>4</td>
</tr>
<tr>
<td>SiGe bipolar transistor</td>
<td>20 x 0.12 µm$^2$</td>
<td>4</td>
</tr>
<tr>
<td>SiGe bipolar transistor</td>
<td>1 x 0.12 µm$^2$</td>
<td>2</td>
</tr>
<tr>
<td>SiGe bipolar transistor</td>
<td>8 x 0.12 µm$^2$</td>
<td>2</td>
</tr>
<tr>
<td>SiGe bipolar transistor</td>
<td>20 x 0.12 µm$^2$</td>
<td>2</td>
</tr>
<tr>
<td>RP type resistor</td>
<td>2 kΩ</td>
<td>3</td>
</tr>
</tbody>
</table>

![Figure 7: Pre- and post-irradiation current gain of several 8HP transistors irradiated with neutrons at various fluences.](image)
reciprocal gain, \( \Delta(1/\beta) = 1/\beta_f - 1/\beta_0 \), is a widely used parameter in the literature of radiation effects on bipolar transistors, but we have also chosen the final post-irradiation gain \( (\beta_f) \) in order for the designers to have a more direct insight on the performance degradation of the transistors within the circuits. These figures-of-merit have been extracted for all the transistors irradiated with neutrons and gammas at a base-emitter voltage of 0.75 V, which corresponds to an injection level close to the actual injection level that these transistors are expected to work in the real circuits.

Figure 8 shows the change in reciprocal gain for the 8WL transistors irradiated with neutrons. As expected from the literature [13], there is a linear dependency of this parameter with the 1 MeV neutron equivalent fluence, although it seems that the damage starts to saturate at the higher fluence of \( 2 \times 10^{15} \) cm\(^{-2} \). The same plot but this time for the gamma irradiated 8HP transistors (Figure 9) shows a linear dependency in the log-log plot, resulting in a dependency of the type \( \Delta(1/\beta) = (\text{dose})^a \) where \( a \) is a constant, which we have also observed in the past for advanced bipolar transistors [14].

For a more direct knowledge of the suitability of these transistors for the ATLAS upgrade electronics, we can see the plots of their final current gain after irradiation. Figure 10 and Figure 11 show this parameter for neutron and gamma irradiations respectively. It can be seen that all transistors remain well over a minimum acceptable value for the current gain of 50 after irradiation up to our highest target fluence and dose. Some of the transistors irradiated with neutrons at higher fluences do show more marginal performance. Also, some dispersion in the results for the different transistors can be seen. We believe this is due to problems or variability in the test structure. In any case, as we do not really know the actual cause and we have no information about the fabrication conditions of these parts, we want to repeat these measurements with our own test chip made with design-kit transistors, as presented above, and fabricated within process specifications.

IV. CONCLUSION

The electrical characteristics of both IBM 8HP and 8WL SiGe technologies make them good candidates for the front-end readout stage for sensors that present large capacitive loads and where short shaping times are required, such as the upgraded ATLAS silicon strip detector (especially the long strip version) and the liquid argon calorimeter.

Three ICs have been designed to evaluate the suitability and radiation hardness of these technologies and their performance for the mentioned applications. Simulations show that the circuits will meet the requirements and allow considerable power savings to the systems.

The bipolar devices of the two SiGe BiCMOS technologies studied experience performance degradation from ionization and displacement damage. Nevertheless, the level of degradation is manageable for the expected radiation levels of the upgraded ATLAS LAr calorimeter and silicon strip tracker. The dispersion of final gains after irradiation may be a concern that warrants further investigation.

V. REFERENCES


Figure 10: Post-neutron irradiation of 8HP (a) and 8WL (b) transistors at an injection level of $V_{BE} = 0.75$ V.

Figure 11: Post-gamma irradiation of 8HP (a) and 8WL (b) transistors at an injection level of $V_{BE} = 0.75$ V.
The ABCN front-end chip for ATLAS Inner Detector Upgrade

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Abstract

We present the design of the ABCN front-end chip implemented in a CMOS 0.25 µm technology and optimized for short silicon strip detectors as foreseen for the ATLAS Silicon Tracker Upgrade.

A primary aim of this project is to develop an ASIC with full functionality required for readout of short silicon strips in the SLHC environment in a cost-effective and proven technology. Design efforts have been focused on optimizing noise and power performance of the front-end circuit for low detector capacitance, minimizing power consumption in digital blocks and on compatibility with new power distribution schemes being developed for future tracker detectors.

The architecture of the chip as well as critical and novel design aspects are discussed in the paper. The ABCN ASIC will serve as a basic test vehicle in an extensive program on development of sensors and modules for the ATLAS Silicon Tracker Upgrade.

I. INTRODUCTION

A primary challenge of tracking detectors being developed for the SLHC environment is a high occupancy, which affects directly the granularity of sensors and the number of electronic channels, to be about 10 times higher compared to the present SCT. As a result, power consumption in the readout ASICs is one of the most critical issues on top of usual requirements concerning noise and radiation resistance. These requirements have to be considered taking into account present and expected trends in development of industrial CMOS processes. In order to address all these aspects an R&D proposal has been initiated to develop a new ASIC for the ATLAS Silicon Tracker Upgrade [1].

Because of increased number of electronic channels in the Silicon Tracker Upgrade and the constraints on the space available for the power cables and other services an efficient power distribution scheme appears as one of the critical problems to be worked out. A scheme like the one employed in the present ATLAS SCT detector with each detector module being powered by an individual set of cables is not feasible at all. Various schemes for power distribution, like serial powering of modules or DC-DC step-down converters on the detector, are under investigation in the frame of another R&D project [2]. Thus, the new ASIC architecture has to be compatible with whatever power distribution scheme will be adopted in the future.

The basic concept and architecture of the ABCN follows the architecture of the ABCD3T ASIC implemented in BiCMOS DMILL technology and used in the present ATLAS SCT detector [3]. The basic features of this architecture are: binary front-end, pipeline for first level trigger latency, derandomizing buffer, zero suppression and data compression logic.

A new front-end circuit is based on the prototype developed earlier in a CMOS 0.25 µm technology [4] but it has been now optimized for readout of short strips. A primary goal was to reduce the power consumption while maintaining the required noise and timing performance of the circuit.

The architecture of the readout circuitry has to address two other aspects related to a new concept of the basic detector module. A new scheme for readout electronics assumes two additional stages of data concentration and multiplexing on the detector between the front-end ASICs and the off-detector electronics [5].

The ABCN prototype ASIC has been designed and manufactured in the IBM CMOS 0.25 µm technology, however, this is considered as an intermediate step towards implementation of this readout architecture in a more advanced process for the final design. Reasons for implementing the present prototype in the 0.25 µm technology were partially economical and partially technical concerning availability of a design kit allowing for using advanced design techniques for the digital part of the ABCN. Nevertheless, all critical aspects of the new architecture have been implemented in the present prototype and the ASIC will be used as a basic test vehicle in the program to develop detector modules for the ATLAS Silicon Tracker Upgrade.

II. ASIC ARCHITECTURE

A block diagram of the ABCN chip is shown in Figure 1. The ABCN ASIC follows the concept of binary readout of silicon strip detectors as implemented in ABCD3T ASIC [3]. It comprises 128 channels of preamplifier/shaper/comparator circuits with two memory banks, one used as a pipeline for the trigger latency and another one used as a derandomizing buffer. The front-end has been optimized for 5 pF detector capacitance (2.5 cm long silicon strip detector) and it is compatible with either detector signal polarity. The shaper is designed for 25 ns peaking time providing 75 ns double pulse resolution and comparator time walk less than 15 ns compatible with 25 ns BCO clock.
The power management block comprises two alternative prototype circuits of the shunt regulators needed if a scheme with serial powering module will be adopted, and a linear regulator, which delivers a clean and stable supply voltage for the analog front-end circuits. This linear regulator will be particularly important if a power distribution scheme with DC-DC step-down converters on the detector is adopted. Therefore, the design of the regulator is optimized for high rejection ratio so that it can operate with a noisy input power supply.

Since the ABCN chip will be used for the ATLAS Silicon Tracker Upgrade module development program, one of the basic requirements is the tolerance to ionizing radiation. For the IBM 0.25 µm process used, radiation tolerance up to a level of 100 MRad TID has been already demonstrated, provided that all NMOS devices are in enclosed geometry layout. In order to improve the immunity of the chip to Single Event Upsets (SEU) all configuration registers and the fast command decoder are designed with triple vote logic and auto correction. The SEU event flag can be read out from the STATUS register.

A. Design methodology

The analog blocks including the front-end circuits, Digital to Analog Converters, Calibration Circuit as well as RAM memory banks have been designed using full custom techniques, both for the schematic and the layout. After positive LVS verification, the post-extracted simulations were performed in order to check possible degradation of performance due to parasitic capacitances.

A significant reduction of the overall power consumption of the front-end part has been achieved by reducing the bias currents in the buffers, shaper and discriminator stages, which undesirably pronounced the influence of the parasitic capacitances on the overall shaping function of the front-end. The final adjustment of capacitances in the filtering stages was done with Spice simulations, taking into account all parasitic capacitances extracted from the layout of the chip.

The digital part was fully described in the Verilog HDL except pipeline and derandomizing memories, which were used as macro cells with well defined digital description. Verilog code was synthesized first time with the default timing library wireload model. In the following iterations the wireload model generated in the last step of the place and route (P&R) procedure was used. The scan chain was added to improve testability of the chip.

The P&R starting from the Verilog gate netlist was done using the First Encounter tool. The floorplan definition was highly constrained by the design and area of the memory blocks (they consume significant amount of the total area of the digital part). After each consecutive step of the P&R, clock tree synthesis (CTS), routing timing verification and set-up/hold optimization was performed. There are two independent clock trees, one slower for control and second one faster for data readout. Also the reset signal tree was built in the CTS phase.

Figure 1: The block diagram of the ABCN chip

Figure 2: The schematic diagram of the preamplifier, shaper and comparator stage.
After routing of connections the physical verification was performed. In principle the routing procedure should comply with the DRC rules automatically, however, the rules get sometimes violated due to e.g. routing problems. If such errors could not be corrected manually next run of P&R sequence with different parameters or a different floorplan definition was performed. The procedure was repeated several times until satisfactory performance was achieved.

Generation of the output files was the last step of the P&R procedure. The Verilog gate netlist changed during optimizations and CTS with SDF including delays were used for post-P&R Verilog simulations. The GDS file describing the layout of the digital part and wire load models were then used for next synthesis iteration.

The top level was assembled in semi-automatic way with the First Encounter used for routing and pad ring definition. The final DRC and LVS verification was performed on the complete design.

B. Front-End design

The schematic diagram of the front-end amplifier and comparator is shown in Figure 2. The preamplifier stage is built as a classical cascode stage with NMOS input transistor biased nominally with 140 µA and an active feedback circuit employing PMOS transistor working in saturation and biased with a current of 300 nA. Dimensions of the input transistor, width equal to 320 µm and channel length of 0.5 µm, are optimized for an input capacitance of 5 pF using the EKV model parameterization. A 90° phase margin for nominal bias conditions and input capacitances up to 15 pF is maintained by two, each of 70 fF, feedback capacitors.

The first section of the shaper consists of two stage voltage amplifier in common source configurations enclosed with a resistive feedback stabilizing the gain and together with feedback capacitance C2 defining the integration time constant. The pulse gain at the output of this stage is in a range of 34 mV/fC and peaking time is about 20 ns. The DC voltage at the output is controlled by the voltage Vfeed applied at the gate of preamplifier feedback transistor and it is optimized for positive or negative input signal polarity using one of the internal biasing DAC.

The second stage of the shaper is an AC coupled differential voltage amplifier with resistive load serving for two purposes. First, it amplifies, integrates and converts to differential mode the single-ended signal from the precedent section. Furthermore, it interfaces the threshold voltage of the comparator, which is applied differentially to the gates of the NMOS source followers. The offset correction voltage is generated as a voltage drop across the load resistor due to the trimming current. The ranges of five-bit trimming DACs are programmable and can provide the trimming steps from 0.5 mV to 3 mV (0.005 to 0.03 fC) depending on the threshold offset spread.

The gain at the differential discriminator input is 100 mV/fC and the intrinsic peaking time of the circuit is 22 ns what ensures 25 ns peaking time including the charge collection time in the detector. The simulated responses of the preamplifier-shaper-comparator stage to signals ranging from -2 to -10 fC are shown in Figure 3.

The front-end circuit can accept input signal of any polarity and provides good linearity (Integral Non Linearity less than 3%) for input charges up to +/-10 fC. For the nominal power consumption of 0.7 mW per channel, the calculated ENC for 5 pF detector capacitance is below 800 e’, which allows using this front-end with heavily irradiated silicon detectors. The ENC as a function of the input capacitance for the nominal bias condition and the maximum expected detector leakage current of 600 nA is shown in Figure 4.

The last stage of the signal processing chain is a leading edge comparator with the input stage built of NMOS differential pair loaded with resistors and PMOS transistors serving as swing limiters. This stage is supplied from analog power rails. The following two-stage CMOS amplifier with hysteresis providing amplification and differential to single-ended full swing signal conversion is supplied from the digital power supply lines. This solution ensures good separation between the analog and the digital part of the front-end chain. The simulated attenuation of interferences from digital power supply to the comparator input is better than 56 dB.

The time walk of the comparator depends only on the amplifier peaking time and for input charges from 1.25 fC to 10 fC is less than 15 ns for a threshold of 1 fC.
C. Digital part of the ABCN

The functionality of the digital part of the ABCN is very similar to the ABCD one used in the present ATLAS SCT detector. Some changes have been made to accommodate a simpler redundancy schema, which costs less in number of tracks on the hybrid, and is compatible with different readout rates. SEU detection and correction circuitry have been added. Because the power consumption of the digital part is becoming dominant, special features have been implemented to measure and control the power consumed by the digital blocks.

III. ON CHIP POWER MANAGEMENT AND DISTRIBUTION

The new design includes on-chip power management circuitry to make it compatible with recent developments in the area of power distribution for the Inner Detector Upgrade, namely DC-DC conversion schemes and serial powering scheme.

A. Compatibility with serial powering of detector modules

Serial powering of detector modules offer, in principle, an elegant solution to the power distribution problem, however, it introduces new aspects that have to be addressed in the front-end ASIC. The scheme requires that each module comprising 20 to 40 ABCN ASICs, depending on the module design, have to be powered through a shunt regulator. The shunt regulator can be either an external device, one per hybrid, or can be a distributed structure, i.e. each ASIC contains a shunt regulator, which are then connected in parallel on the module. Each solution has some advantages but none is free of difficulties. Furthermore, neither scheme has been used so far in particle physics detectors. Advantages of the distributed shunt regulator system are:
- power dissipated in the shunt regulators is distributed uniformly across the hybrid,
- no very high current devices are required,
- single point of failure is eliminated, compared to solutions with one regulator per hybrid,
- the hybrid design can be fully scaleable with respect to power distribution.

The ABCN design comprises two prototype circuits, which can be used alternatively. One circuit is a full shunt regulator. Another circuit comprises only shunt transistors, which are foreseen to be controlled by an external regulator, common for all ASICs connected in parallel on the module. The conceptual schematic diagram of the developed shunt regulator for connecting several shunt regulators in parallel on the hybrid is shown in Fig. 5. In addition to the conventional shunt regulator, the design comprises circuitry responsible for limiting the current flowing through the shunt transistor at a preset level and adjusting the reference voltage and so the output voltage of the regulator. The current of the shunt transistor is sensed and compared with six different reference currents. If the sensed current exceeds the given reference current a correction current source gets connected to the input of the auxiliary transresistance amplifier, which corrects the reference voltage such that it limits the shunt current in the corresponding shunt device. Simultaneously, other shunt devices connected in parallel sink more current.

It is worth noting that this is a one-step operation and after this operation the correction current source remains connected while the feedback loop between the shunt transistor and the correction circuit is interrupted. Such a solution ensures that the output impedance of the shunt regulator is not affected by the correction circuit.

The current threshold ITH in one of the six stages is set high, about 100 mA corresponding to maximum expected switching current. This stage works like an over current protection circuit in cases when no digital switching current is drawn by the ABCN chip and it has to be taken by the shunt device. The threshold is set by an internal resistor. Three resistors with terminals connected to external pads allow selecting an appropriate threshold according to the digital current draw.

Other five stages work according to the same principle, but their role is to redistribute the current between shunt devices in normal steady-state operation so that the shunt currents and the output impedances of the shunt devices connected in parallel are of the same order of magnitude. The nominal current thresholds Ith1 to Ith5 in the five stages are scaled with the following pattern: ×1, ×2, ×3, ×4, ×5. When the shunt current in the device exceeds given threshold the corresponding correction current is switched on and the reference voltage is adjusted accordingly.

![Figure 5: Conceptual schematic diagram of the shunt regulator with auxiliary correction amplifier.](image)

B. On chip linear voltage regulator

The on-chip any-capacitor stable linear voltage regulator provides the voltage supply for the sensitive front-end part of the chip. It is optimized for a high power supply rejection ratio, achieving 33 dB at 30 MHz with 100 nF decoupling capacitor. It provides immunity against the switching noise in case of the DC-DC converter power source is used and separates the analog power supply voltage from the common power supply provided for both the analog and the digital circuits by the shunt regulator in the case of serial powering.

IV. SUMMARY AND PERSPECTIVE FOR CMOS FRONT-END IN 130 NM PROCESS

Analogue specifications, functionality, as well as new power management features make ABCN a suitable test vehicle for SCT upgrade R&D program. The front-end circuit of the ABCN is expected to be radiation resistant with respect to TID due to intrinsic radiation hardness of the CMOS
process and by using NMOS transistors with enclosed gates. The architecture of the digital circuitry and its immunity to SEE is a compromise between the requirements for the error rate and power consumption increased by using triple vote logic with auto correction. Therefore its application is limited to most important part of the logic i.e. configuration registers and fast command decoder.

A final choice of the ASIC technology for the Atlas Silicon Tracker Upgrade is not decided yet. However, taking into account the LHC upgrade schedule and present trend for CMOS technology scaling, the final front-end chip for the Upgrade will be manufactured in a technology with the feature size below 250 nm. The two following figures illustrate expected numbers for the ENC and power consumption for the front-end circuits implemented in currently available 130 nm CMOS process from IBM.

![Figure 6:](image1.png) The expected ENC performance of the front-end implemented in IBM 130nm process optimized for short, 2.5 cm, silicon strip detectors. The input transistor bias is equal to 80 µA, the feedback transistor is biased with 300 nA and assumed detector leakage current is 600 nA.

![Figure 7:](image2.png) The expected ENC performance of the front-end implemented in IBM 130 nm process and optimized for long, 10 cm, silicon strip detectors. The input transistor is biased with 200 µA, the feedback transistor is biased with 700 nA and assumed detector leakage current is 1.3 µA.

From Figure 6 with Figure 4, the latter one obtained for 250 nm process, one can see that a comparable ENC performance can be achieved at significantly lower bias current used in the input stage of the circuit implemented in the 130 nm technology. There are three basic reasons for that. First one is a lower slope factor n, which decreases from 1.45 in the 250 nm process to 1.25 in the 130 nm process. As a result, the transconductance of NMOS devices biased in weak inversion region is only 25% lower than the transconductance of bipolar transistors biased with the same current. In parallel to this, moving from the 250 nm to the 130 nm process the transconductance parameter $g_{m_{N MOS}}$ increases from 300 µA/V to 750 µA/V, allowing for biasing of relatively small input devices closer to weak inversion region, which is more optimal from the noise performance standpoint of view.

Another important factor taken into account is the level of the excess noise usually present in transistors manufactured in submicron technologies with very short channels. Several measurements done for 130 nm IBM process confirm [6] that there is no excess noise for devices with channel length equal to or longer than 250 nm (for NMOS transistors in IBM 250 nm process excess noise $\gamma$ factor was around 1.3).

Further savings of power consumption for the 130 nm design can be expected in the shaper, buffers and comparator stages due to the availability of high value, 1.7 kΩ/square, polysilicon resistors providing low stray capacitances. The expected numbers on power, assuming 1.2 V supply voltage, are 160 and 300 µW for front-end optimized for short and long strips respectively.

A prototype demonstrator chip comprising the front-end circuits optimized for short and long strips will be manufactured next year in the 130 nm IBM process.

V. ACKNOWLEDGEMENTS

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VI. REFERENCES

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Parallel Session B1
Trigger 1
The Level 0 Pixel Trigger System for the ALICE Silicon Pixel Detector: implementation, testing and commissioning

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Abstract

The ALICE Silicon Pixel Detector transmits 1200 Fast-OR signals every 100 ns on 120 optical readout channels. They indicate the presence of at least one hit in the pixel matrix of each readout chip. The ALICE Level 0 Pixel Trigger System extracts them, processes them and delivers an input signal to the Central Trigger Processor for the first level trigger decision within a latency of 800 ns. This paper describes tests and measurements made on the system during the qualification and commissioning phases. These included Bit Error Rate tests on the Fast-OR data path, the measurement of the overall process latency and the recording of calibration data with cosmic rays. The first results of the operation of the Pixel Trigger System with the SPD detector in the ALICE experiment are also presented.

I. INTRODUCTION

The Silicon Pixel Detector (SPD) is the innermost detector of the ALICE experiment at the LHC [1][2][3]. The SPD is a double layer barrel pixel detector [1][4], constituted of 120 modules (half staves). The half staves are staggered on a carbon fiber support structure, 40 on the inner layer (r = 39 mm) and 80 in the outer one (r = 76 mm). Each half stave includes two 200 μm thick silicon pixel sensors with 160×256 pixels of 425×50 μm². The two sensors are bump bonded to 10 front end pixel chips operating at 1/4 of the LHC bunch crossing frequency, i.e. at ≈10 MHz. Each of the 1200 SPD readout chips has a prompt Fast-OR output. The Fast-OR signal is asserted within 300 ns from a particle hit in any of the 32×256 (8192) pixels read out by the chip. The readout chips of each half stave are connected to a Multi Chip Module (MCM) [5].

The MCM includes four custom ASICs and one custom optical transceiver module. The MCM implements the communication interface to the off detector electronics in the control room and provides bias and control signals for the pixel chips. Two optical links are used to transmit the LHC 40.0786 MHz bunch crossing clock and serial control to the MCM. The MCM uses a third optical fiber to transmit information to the readout electronics in the control room and to the Pixel Trigger System in the ALICE cavern. All optical fibers are single mode and the operating wavelength is 1.3 μm. The MCM transmits status and control feedback signals and the ten sampled Fast-OR bits every 100 ns. The pixel hit data are transmitted only during a readout sequence. The readout and transmission of hit data are initiated and controlled by the MCM upon receiving a positive trigger decision via the serial control.

The Fast-OR data are used in the ALICE first level (Level 0) trigger decision to improve background rejection in pp interactions and event selection in heavy ions runs. Various trigger algorithms based on topology or multiplicity of Fast-OR signals have been investigated [6]. All of them can be implemented as boolean logic functions of the 1200 SPD Fast-OR signals on field programmable devices.

The Pixel Trigger System (PIT) extracts the Fast-OR signals from the 120 SPD output data links and processes the selected pixel trigger algorithm. It has to provide the result to the ALICE Central Trigger Processor (CTP) where it contributes to the Level 0 decision. The total time from the particle collision to the transmission of the result to the CTP should be less than 800 ns. The system is independent from the SPD readout electronics located in the control room and is located in the experimental cavern, where a limited space of one 9U crate is available for the electronics boards. The design, earlier developments and implementation details of the Pixel Trigger System have been previously published [7][8][9]. In the following we review the system as it is presently installed in ALICE. Laboratory integration tests and measurements made before the installation are presented in detail. Finally, we discuss the commissioning and the first operation of the Pixel Trigger System with the SPD in the ALICE experiment.

II. THE ALICE PIXEL TRIGGER SYSTEM

Fig. 1 shows a diagram of the connections between the SPD, the readout electronics, the Pixel Trigger System and the CTP. The main clock and the trigger commands are distributed to all subsystems by the CTP via the local Timing Trigger and Control (TTC) distribution network [10]. The SPD readout electronics is located in a control room ~100 m far from the detector. The CTP and the PIT crates are in the experimental cavern, close to the ALICE apparatus. The 3 × 120 clock, serial control and data fibers are routed separately for the modules on the two symmetric halves (side A and side C) in which the SPD is divided by the plane orthogonal to the detector axis and passing by its center. The readout data fibers coming from the detector are connected to 120 passive optical splitters. One of the output branches forwards data to the readout electronics while the second one is connected to the Pixel Trigger System. The ten outputs of the PIT are connected to dedicated CTP inputs.

Following a collision in a bunch crossing, particles traverse the SPD and Fast-OR signals are transmitted to the PIT. The results of the Fast-OR processing are transmitted to the CTP for the trigger decision that is based on inputs from all the trigger detectors. In case of a positive decision a trigger command is transmitted to the readout electronics by the TTC link. A read-
The Pixel Trigger System electronics is constituted by ten optical receiver boards (OPTIN) and one processing mother-board (BRAIN). The ten OPTIN boards deserialize the received data and extract the 1200 Fast-OR signals from the data flow. The OPTIN board contains an FPGA¹ and is equipped with a custom 12-channel parallel optical fiber receiver module and twelve G-Link deserializer ASICs [11]. Each OPTIN board receives data fibers from 12 SPD half staves. The components are densely arranged on a 160×84 mm² 12-layer printed circuit board. The BRAIN electronic board (400×360 mm², 9U) hosts the Processing FPGA², a device with 960 user I/O pins and 110592 logic cells. The ten OPTIN boards connect as mezzanine boards on the BRAIN, five on each side. Fig. 2 shows a photograph of the BRAIN board with OPTIN boards plugged on two of the five locations on the visible side of the BRAIN. Fig. 3 shows the Pixel Trigger electronics partially inserted into the hosting crate.

The 1200 Fast-OR signals extracted every 100 ns in the OPTINs are transferred to the Processing FPGA on 600 striplines using 2× time multiplexing (Double Data Rate transfer). The Digital Source Impedance control feature of the FPFGAs is used to impedance match these lines. Several processing algorithms can be implemented in parallel in the Processing FPGA and the maximum number is limited only by their complexity and by the available logic resources. Ten LVDS lines are available to transmit the results to the CTP, limiting to ten the number of pixel algorithms that can be used in parallel by ALICE. All algorithms implemented in the firmware up to now complete in one clock cycle.

Figure 1: Simplified diagram of the control, readout and trigger connections between the Silicon Pixel Detector, the SPD readout electronics, the Pixel Trigger System and the Central Trigger Processor in the ALICE experiment.

Figure 2: A photograph of the BRAIN board. The Processing and Control FPGA are indicated. OPTIN boards are connected on two of the five visible locations. Five other locations are on the other side of the BRAIN board. The ALICE DDL-SIU mezzanine board is also visible.

The Control FPGA on the BRAIN board provides the control and communication functionalities. It manages a 32-bit shared bus that allows intercommunication between all the FPGA devices of the system. The custom bus protocol is a simplified version of the PCI protocol. The Control FPGA acts as the bus master, while the OPTIN boards FPFGAs and the Processing FPGA are the target devices answering to the read and write transactions governed by the Control FPGA. Parity checking and transaction acknowledgement are performed in the hardware.

The Pixel Trigger System is remotely controlled by a custom software driver executing on a dedicated computer [12]. The ALICE Detector Data Link (DDL) is used as communication layer between the computer and the electronics [13]. The DDL Source Interface Unit (SIU) front-end board is the DDL interface on the BRAIN board. It is connected to the Control FPGA that acts as a bridge between the the DDL link and the board shared bus. The driver uses the hardware functionalities to detect any failure of the parity checks or any mismatch between the requested and the actual length of the transferred data blocks. The state machines in the hardware recover safely in case of errors and return to an idle state, ready for subsequent read or write accesses.

The system gets the main clock from the TTC by the TTCrx and QPLL chips. USB and JTAG interfaces provide local access for hardware testing and debugging. Auxiliary high speed serial lines and optical transceivers are available for future upgrades requiring high bandwidth communication with the control room.

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¹Xilinx Virtex 4 LX60.
²Xilinx Virtex 4 LX100.
Figure 3: The Pixel Trigger System crate. The electronics board are partially extracted from the crate. Five OPTIN boards are connected on the visible side of the BRAIN board. One of the ten optical fiber fan-in cables and one optical patch panel are also shown.

III. LABORATORY TESTS AND MEASUREMENTS

A. Electrical tests and clock distribution

The current consumptions of the boards are given in Table 1. Power demand was lower than the design expectations because the FPGA operating currents had been overestimated. The total power of 200 W is a small fraction of the power that can be safely dissipated in a cooled 9U electronic crate. A peak temperature of 45 °C was measured on the boards. According to the thermal model used in the design phase, the voltage regulators of the OPTIN boards were the components reaching the highest temperature and therefore they were equipped with large aluminium heat sinks. Considering the temperature measured on the heat sinks during operation and the junction-ambient thermal conductivity, the junction temperature of the voltage regulators resulted of 72 °C, safely below the maximum rating of 125 °C for these devices.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>5 V</td>
<td>2.8</td>
<td>0.375</td>
<td>15.3</td>
</tr>
<tr>
<td>3.3 V</td>
<td>7.9</td>
<td>1.6</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td>36.1</td>
<td>5.4</td>
<td>198</td>
</tr>
</tbody>
</table>

Complete JTAG interconnect tests were performed on all the boards to detect missing connections or short circuits. Up to three JTAG chains were simultaneously driven and read during these tests, with the OPTIN board under test connected to one of the slots on the BRAIN. All the OPTIN boards and all the slots were tested in turn. The signal lines that are not accessible by JTAG were stimulated by driving circuitry inside the FPGAs and tested with a scope. The signal propagation delay measured on the boards was of 6.9 ns/m, slightly lower than the value of 7.8 ns/m estimated in the design phase. The phases of the clock signals of all the OPTIN FPGAs relatively to those of the Processing and Control FPGAs were measured. The resulting distribution showed an average shift of ∼3 ns and a RMS spread of ∼1 ns. Subsequently the internal clocks of the Processing and Control FPGAs were phase adjusted to compensate for the average shift and their transitions moved to the middle of the distribution of those of the OPTIN FPGAs.

B. Fast-OR data path Bit Error Rate tests

Bit Error Rate (BER) tests were done on the full data path of Fast-OR signals to qualify the integrity of the communication and processing chain. In general BER tests [14] are based on counting bit mismatches between transmitted data and data that are extracted at the receiver end of the communication channel under test. The number of mismatches counted during a transmission run allows to evaluate boundaries for Bit Error Rate, i.e. the probability that the bit received at the output is different than the transmitted one. Tests might require the transmission of very long sequences to gather sufficient statistics in a normal case with a very low error probability. An upper boundary for the BER can be determined even in case no bit mismatches are observed.

The setup used for our tests is shown schematically in Fig. 4. A hardware emulator of one MCM was used as data source. This included a Pseudo Random Bit Sequence (PRBS) generator, a serializer GOL chip [15] and a laser transmitter. The optical signal was attenuated to operate in limiting conditions and fed into a 1×16 optical splitter. One OPTIN board was connected to one of the slots of the BRAIN. Twelve of the sixteen fibers were connected to the OPTIN using the same optical fan-in cables that were later installed in ALICE. The twelve channels of the OPTIN were therefore receiving exactly the same optical signal. The optical power at the output of each fiber was 18.5 dBm with 50% Optical Modulation Amplitude, only 0.5 dBm above the minimum operating power required by the optical receiver module on the OPTIN.

The Fast-OR signals were extracted and transferred to the Processing FPGA. A set of bit comparators were implemented in the Processing FPGA and they compared the data words re-
ceived on pairs of adjacent channels. With this approach it was not necessary to reconstruct the transmitted word at the receiver end. The test was repeated an all the OPTIN boards in turn and connecting them to different slots. Table 2 summarizes the results of the tests. In all cases no word errors and therefore no bit errors were observed. In a typical run the Bit Error Rate was less than $8.1 \times 10^{-13}$. In two longer tests this figure improved by one order of magnitude.

Table 2: Fast-OR Bit Error Rate tests results. The typical test was made on eight OPTIN boards and lasted 1.5 hours. The entry labeled with Max refers to longer tests made on two OPTIN boards. BER upper bounds are evaluated at 99% confidence level.

<table>
<thead>
<tr>
<th></th>
<th>Hours</th>
<th>$N_{bits}$</th>
<th>Errors</th>
<th>BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical</td>
<td>1.5</td>
<td>$5.7 \times 10^{12}$</td>
<td>0</td>
<td>$&lt; 8.1 \times 10^{-14}$</td>
</tr>
<tr>
<td>Max</td>
<td>17.8</td>
<td>$7.7 \times 10^{13}$</td>
<td>0</td>
<td>$&lt; 6 \times 10^{-14}$</td>
</tr>
</tbody>
</table>

Another test was realized with ten OPTIN boards simultaneously connected to the BRAIN board. In this case the Fast-OR data were generated by internal sequencers implemented in the OPTIN FPGAs. Pseudo random bit patterns were generated in all the 120 channels of the OPTINs and simultaneously transmitted to the Processing FPGA on the 600 dedicated lines. As in the previous case the bit comparators in the Processing FPGA were used to detect and count possible bit mismatches between the words received on pairs of channels. The longest test lasted 15 h with $6.48 \times 10^{14}$ bits transmitted and received. No bit errors were observed, implying that the Bit Error Rate of the transmission between the ten OPTIN boards and the Processing FPGA is less then $7.1 \times 10^{-15}$ with 99% confidence level. This test ensured that no degradation of the Fast-OR data transmission is introduced by coupling noise when the 600 signal lines densely routed in the region of the Processing FPGA are simultaneously driven.

**C. Control Bus Bit Error Rate tests**

Dedicated tests were performed to qualify the custom control architecture. The software driver wrote, read back and checked blocks of random data from all the target devices on the Pixel Trigger System bus. All the produced OPTIN boards were tested in turn. A typical test lasted ~15 min and more than $6 \times 10^8$ bits were transferred during these runs. For two boards the tests lasted about 12 h and a total of $3 \times 10^{10}$ bits were exchanged in these cases. No bit errors were detected in all the trials. These tests qualified the reliability and robustness of the full control chain including the Alice DDL interfaces, the optical link, the communication interface blocks in the Control FPGAs and in the other eleven FPGAs of the system as well as the custom protocol of the shared bus and the Pixel Trigger System driver software.

**D. Latency measurement**

The integration of the SPD and of the readout electronics before their installation in the experimental cavern were done in a laboratory setup almost identical to the system installed in the ALICE experiment. This setup is currently used with spare SPD modules for the refinement of calibration procedures and for the development of hardware and software functionalities. It was also used to measure the Pixel Trigger System latency.

The test pulse input on the SPD pixel chip was activated to inject charge into the front end amplifier of the readout cells. This is equivalent to the passage of a particle across the sensor and activates the Fast-OR output of the chip upon the second following rising edge of the ~10 MHz clock. Due to synchronization with the clock, the Fast-OR output activates upon the same clock edge no matter when the injection precisely happens within one clock cycle interval of 100 ns. In our setup the test pulse was activated in correspondence of a clock falling edge, that is in the middle of the intrinsic uncertainty interval. A latency of 733 ns was measured between the charge injection and the activation of the Pixel Trigger output.

Signal connections present in the ALICE system but not included in the laboratory setup require 41 ns of propagation delay. Further uncertainty (±12.5 ns) is due to the phase relationship of the 120 MCM clocks with respect to the bunch crossing clock and to the PIT receiver clocks. Phase tuning of the SPD and PIT system clocks during LHC operation with particle collisions is required to minimize the previous contribution to the latency. Considering the intrinsic time accuracy of 100 ns, it follows that the latency of the Pixel Trigger System in the ALICE experiment can range between ~736 ns and ~836 ns in the worst case and between ~712 ns and ~812 ns in the best case.

**IV. COMMISSIONING IN ALICE**

**A. Synchronization and optical fibers routing**

The ~10 MHz clock signals of the readout chips are generated on the MCMs by 4× division of the received 40.0786 MHz clock. The MCM keeps the phase of the slow clock aligned to the serial control frames received from the readout electronics. The phases of the two clocks should be, in the ideal case, equal across all the half staves so that the Fast-OR signals are activated by collision events belonging to the same set of four consecutive bunch crossings.

To synchronize both clocks across the modules it is necessary that the ~40 MHz clocks and the serial messages are not only synchronously transmitted from the control room electronics but also synchronously received by all the half staves. For this purpose the lengths of the relevant fiber links were equalized. The measurements of fiber lengths are listed in Table 3. Assuming that the refractive index of SiO$_2$ at 1.3 $\mu$m is 1.447, the propagation latencies differ by 1.45 ns at most. The relative phases of a subset of clock signals were measured at the transmitter end of the clock links and the RMS spread was of ~0.475 ns. It follows that the rising transitions of the ~40 MHz clocks in the SPD modules are confined in a 4.3 ns time interval, that is about 17% of the clock period.

In order to synchronize the transmission phases of the 120 serial control streams from which the alignment of the divided clocks depends, a dedicated broadcast command was implemented on the local TTC system. This allows the simultaneous transmission of the synchronization command to all the 120 serial control channels. The command is issued during the system configuration phase before each data taking run.
The lengths of the data fibers between the SPD and the PIT were minimized to reduce the Fast-OR propagation delay and equalized to guarantee synchronous deserialization of the data stream in the PIT.

### B. Data frame synchronization

The MCM transmits Fast-OR, feedback and hit data using a custom protocol [16]. Four transmission frames repeat continuously as shown in Fig. 5. The first and second frames contain the ten Fast-OR bits of the half stave and feedback signals respectively. The third and fourth frame contain the pixel hit data during a readout sequence. The clock synchronization across the 120 half staves guarantees that the frame sequences are transmitted synchronously. However, they can be decoded in different clock cycles in the Pixel Trigger deserializer stages for two reasons. The first one is that the transmissions of modules with longer data fibers suffer a longer propagation delay. The second one is that the clock phases of the deserializers can be out of optimal alignment with respect to the clock reconstructed from the received signal. The latter situation can imply a further delay of one clock period added automatically by the OPTIN receiver ASICs and increasing the overall latency.

The Fast-OR packets related to the same ~100 ns time interval must be time aligned to be processed simultaneously. A time stamping functionality was implemented in the FPGAs for this purpose. Trigger commands are received simultaneously by all the SPD modules. The MCMs immediately acknowledge them retransmitting a dedicated word in the next feedback frame of their output stream. The time stamping functionality determines for each channel the clock cycle during which the trigger feedback signal is received. The relative alignment of the deserialized data streams is therefore measured by the circuit itself. The received sequences are then delayed accordingly to the measurements and aligned to the last arriving frame. The entire procedure is fully automated by the driver software.

After the installation in ALICE the phase of the Pixel Trigger System clock was fine tuned adjusting the length of the TTC fiber feeding the clock to the system and using the time stamping functionality previously described. As a result the received sequences were aligned across the two groups of sixty modules of each detector side. The sequences of the modules on side C were decoded one clock period earlier than those of side A, due to the different fiber lengths on the two sides (Table 3). A delay of one clock period was added to the sixty channels of side C, making the system ready for operation.

### V. First operation in ALICE

A cosmic ray coincidence logic was programmed in the Pixel Trigger Processing FPGA. The PIT output activated on the simultaneous presence of at least two active Fast-OR signals, one in the outer layer of the upper half barrel and one in the outer layer of the bottom half. Fig. 6 shows the SPD online monitoring display with a cosmic ray event. The trigger rate ranged from 0.09 Hz to 0.12 Hz depending on the number of active SPD modules. This was well in agreement with the results of a Monte Carlo simulation of the detector including the measured muon flux in the ALICE cavern. Cross checks of the recorded data showed that more than 99.5% of the events presented the cluster distribution required by the trigger algorithm, with at least two clusters in the detector outer layer.

![Figure 6: Cosmic ray event recorded by the SPD triggered by the Pixel Trigger System. Two muon tracks are visible, each generating four hits in the two layers.](image-url)

The cosmic trigger signal was extensively used to readout the SPD detector alone or together with other ALICE detectors. The recorded cosmic ray data proved extremely useful for the commissioning of the SPD, of the Inner Tracking System combined with the TPC and for the tuning of the detectors geometry in the offline reconstruction software. More than 65000 events with at least 3 hits in the SPD and more than 35000 with at least 4 were recorded to date, as well as several events with showers developing in the TPC and traversing the SPD with high occupancy.

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Table 3: Fiber lengths of the SPD detector. Data fiber lengths refer to the section between the SPD and the optical splitter. The uncertainty represents the minimum and maximum lengths.

<table>
<thead>
<tr>
<th>Link</th>
<th>SPD Side</th>
<th>Side A</th>
<th>Side C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clk</td>
<td>107.6 ± 0.15 m</td>
<td>107.6 ± 0.15 m</td>
<td>107.6 ± 0.15 m</td>
</tr>
<tr>
<td>Data</td>
<td>38.5 ± 0.2 m</td>
<td>36.6 ± 0.2 m</td>
<td>36.6 ± 0.2 m</td>
</tr>
</tbody>
</table>

Figure 5: Timing diagram of the MCM output transmission frames. The LHC bunch crossing clock is plotted for reference. In this example the sequence of the $k$-th half stave is deserialized one clock period later than those of other three half staves.
In August 2008 beam injection tests were made at the LHC, in the collider section preceding the ALICE cavern. The beam was dumped before reaching the cavern. The SPD was operated together with the Pixel Trigger System and various large occupancy events were recorded. Fig. 7 shows an example. The recorded events contain long straight tracks developing parallel to the beam axis for several centimeters in the 200 \(\mu\)m thick active volume of the silicon sensors. These were attributed to the muons originating in the beam dump. Some tracks in these events cross the gaps between adjacent sensors and adjacent readout chips. Finally, beam-gas interaction events were recorded during further LHC tests when the first beams were continuously circulated for several minutes in the LHC on 11 September 2008.

VI. CONCLUSIONS

The ALICE Pixel Trigger System allows to include the prompt Fast-OR outputs of the ALICE Silicon Pixel Detector in the first level (Level 0) trigger decision of the experiment. The Pixel Trigger System is a very compact electronic system with a large, parallel data flow architecture. It includes original developments and satisfies challenging requirements at the board level and at the system level. The system has been thoroughly qualified after production with several laboratory tests that were described in this paper. The fulfillment of the stringent constraint on the overall process latency has been experimentally verified as well as the reliability of the system operation. The Pixel Trigger System has been fully installed, commissioned and already operated in the ALICE experiment. The SPD equipped with the Pixel Trigger provided a reliable and extremely useful cosmic trigger during the commissioning of the ALICE detectors. Events related to beam dumping or beam-gas interactions were recorded during the first LHC injection and beam circulation tests. ALICE is the only LHC experiment that will include the vertex detector in the first trigger decision from startup.

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Performance and lessons of the CMS Global Calorimeter Trigger

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Abstract

The CMS Global Calorimeter Trigger (GCT) has been designed, manufactured and commissioned on a short time schedule of approximately two years. The GCT system has gone through extensive testing on the bench and in-situ and its performance is well understood. This paper describes problems encountered during the project, the solutions to them and possible lessons for future designs, particularly for high speed serial links. The input links have been upgraded from 1.6Gb/s synchronous links to 2.0Gb/s asynchronous links. The existing output links to the Global Trigger (GT) are being replaced. The design for a low latency, high speed serial interface between the GCT and GT, based upon a Xilinx Virtex 5 FPGA is presented.

I. INTRODUCTION

This paper is devoted to the challenges faced and lessons learnt during the development and commissioning of the GCT system and refers to the architecture of the design and the implementation of high speed serial links. Both are likely to be used in future systems and are of value to the larger LHC trigger community.

A detailed description of the GCT is beyond the scope of this paper and is covered in detail in the CMS Trigger TDR [1] and several subsequent CMS internal notes and conference proceedings [2,3].

The main challenge with the GCT and with most trigger systems is the high bandwidth requirements coupled with the fact that data often needs to be shared or duplicated, and done so with low latency. The GCT uses a mixture of high speed serial links and wide parallel busses. The high speed serial links are necessary to concentrate the data into a single FPGA, thus reducing data sharing requirements and making the processing efficient. The latency cost of these links is not negligible and thus wide parallel busses operating conservatively at 80MHz are used for the rest of the system.

The GCT is modular, which allowed multiple design teams to work in parallel in the initial stages of the product. It also simplified each board, thus reducing the layout and design time. It allowed the GCT-to-GT links to be replaced without requiring complex changes to the main 9U VME data processing card.

Figure 1: The GCT under test in the laboratory. The card on the left is the Concentrator card with 2 Leaf cards mounted on either side to process incoming electron data. The output to the Global Trigger (GTI card) is mounted at the base of the Concentrator. On the right is a Wheel card with 3 Leafs which process incoming jet data. In normal operation a second Wheel card would be mounted to the left of the Concentrator card to process jet data from the negative $\eta$ region of the detector. Wide parallel LVDS cables connect the Concentrator and Wheel cards. They are just visible towards the back of the crate.
II. SYSTEM OVERVIEW

The following description is simply to provide a brief overview of the GCT. A far more comprehensive guide is given elsewhere [2,3].

The GCT input interface with the Regional Calorimeter Trigger (RCT) consists of 63 Source cards. Each of these receive 2 cables with 32bit wide, 80MHz, differential ECL data. The data is retransmitted on 4 optical links, each with a data rate of 1.28Gb/s, 8B/10B encoding and CRC check. The links themselves were originally designed to run synchronously with the TTC (Timing Trigger & Control) clock at 1.6Gb/s, however they were subsequently modified to use a local oscillator and operate at 2.0Gb/s, asynchronously to TTC.

There are significant benefits of using optical links. The GCT is electrically isolated from the high power, ECL technology of RCT. The electron, jet and muon data arriving from RCT can be sorted into separate optical links and reassembled at an optical patch panel into a more appropriate grouping and form factor (12 way fibre ribbons) for GCT.

The electron data, transmitted on 54 optical links, are received by two Leaf cards mounted on the Concentrator card. The links are split across the 2 Leaf cards depending on whether they come from the positive or negative η region of the experiment. The Leaf cards determines the 4 highest rank isolated and non-isolated electrons and transmit the result to the Concentrator, which then performs the same task before transmitting the data to the Global Trigger.

The jet data, transmitted on 180 optical links, are received by 6 Leaf cards distributed across 2 Wheel cards (one for each η polarity). The jet data processing is more complex because substantial amounts of data must be shared between Leaf cards. The 3 Leaf cards are connected in a circular fashion so that each card processes data from a 120 degree φ segment, and can share data with the neighbouring Leaf cards. The same sharing requirement also arises at the boundary between positive and negative η because each half of the detector is processed by Leaf cards mounted on different Wheel cards. In this instance the data at the boundary is duplicated in the Source cards so that the Leaf cards on both Wheel cards have access to boundary condition data. After the jet clusters have been formed they are sorted in the Wheel and Concentrator rectangles) which are used as FIFOs to bridge between the two clock domains. The arrays of Configurable Logic Blocks (CLBs) that are used for general purpose logic are just visible (small grey marks).

III. INPUT LINKS

During commissioning in USC55 it was noted that occasionally one of the links on each Leaf card was generating CRC errors. This was a surprise given that there had been substantial testing in the laboratory before deployment to USC55. The main difference between the two tests had been that the laboratory system had used a local oscillator rather than the TTC clock. Furthermore, the TTC clock specification of less than 50ps peak-to-peak jitter was just outside the specification limit for the Xilinx Virtex II Pro.

Consequently, the original hypothesis was that the CRC errors were due to the quality of the TTC clock. The links were therefore modified to use low jitter 100MHz local oscillators on the Source cards and operate asynchronously to the TTC clock. A low latency clock bridge shifted the incoming parallel data on the Source card from the 80MHz TTC clock to the 100MHz local oscillator. Dummy words were inserted where necessary. The link speed jumped from 1.6Gb/s to 2.0Gb/s. Despite these measures the problem was not resolved.

The fault was eventually traced to firmware tools incorrectly routing the recovered Multi Gigabit Transceiver (MGT) clocks despite constraints to the contrary in the User Constraints File (UCF). Normally these clocks would not be used outside the MGT hard IP (Intellectual Property) block, but to achieve a fixed, low latency design, the elastic buffer, which bridges from the recovered serial link clock and the FPGA fabric clock had to be placed in the FPGA fabric [4,5,6].

The tools default to using global clocks when possible; however, there are only 8 true global clocks in a Xilinx Virtex II Pro and our design required up to 16 serial links, each with their own recovered clock, in addition to the main TTC clock in the FPGA fabric. In this situation, the FPGA can route small parts of the design using local clock routing in a dedicated part of the fabric.

![Figure 2: The correct local clock routing adjacent to two MGTs (not visible) along the top edge of the Virtex II Pro. Occasionally the local clock routing exceeded the boundary (dashed blue line). The local clock (solid red lines) connects to the SelectRAMs (large rectangles) which are used as FIFOs to bridge between the two clock domains. The arrays of Configurable Logic Blocks (CLBs) that are used for general purpose logic are just visible (small grey marks).](image)

The tools should have constrained the clock to the local clock region as shown in figure 2. The MGT local clock route is a 5 x 12 Configurable Logic Block (CLB) array on the top of the device and a 5 x 11 CLB array on the bottom. There are also two block SelectRAMs within each MGT local clock domain.

The local clock routing stayed within the routing boundary after two changes were made. The first was the removal of an asynchronous signal clocked in the TTC clock domain, but used in the local clock domain. The second was CRC check in the local clock domain. It is not understood why these changes made a difference, however the local clock routing now seems to respect the boundary. A similar problem was seen much later with the MGTs that were routed with global
clocks. This issue was simply fixed by forcing the use of a local clock with a constraint within the VHDL file. The firmware has now been synthesised, placed and routed several times and the problem has not recurred.

The system continues to operate with asynchronous links which has the benefit that we can use a very low jitter clock source and the latency is not affected because the increase in latency due to the clock domain bridge on the Source card is cancelled by the internal logic in the SERDES units operating faster.

IV. OUTPUT LINKS

The original GCT-to-GT interface was based on National Semiconductor DS92LV16 [7] electrical high speed serial links operating just beyond specification of 1.6Gb/s. In the revised GCT design, these legacy links were placed on a dual CMC daughter card; the Global Trigger Interface (GTI) card. The links are DC coupled and connect to the GT via 100Ω impedance InfiniBand cables with HSSDC2 connectors. The DS92LV16 chips serialize a 16bit word at up to 80MHz, bounding it with start/stop bits.

The interface was successfully tested with 3.0m cables manufactured by LEONI [8]; however, it was not possible to procure more from this company. An alternative supplier, Amphenol Interconnect [9], provided 1.5m cables. However, when new shorter cables were used for the GCT-to-GT links it was noticed that the SERDES links occasionally lost lock. This was traced to reflections from the receiver rather than any issue with the cable itself.

It was suspected that the degradation in the eye diagram was caused by the signal being reflected of the receiver, which was estimated to be ~7mm from the differential oscilloscope probe.

To confirm the hypothesis a signal consisting of just the start mark (defined as ‘1’), payload of ‘0x00’ and stop (defined as ‘0’) was repeatedly transmitted and measured across the receiver input termination.

![Figure 3](image3.png)

**Figure 3:** The eye diagram of the signal transmitted by the GTI card after it had traversed an HSSDC2 connector, 1.5m InfiniBand cable, a second HSSDC2 connector and then terminated with 100Ω. Horizontal scale = 100ps/div. Vertical scale = 150mV/div. Receiver switching threshold = +/- 100mV.

A good quality eye diagram (fig. 3) is measured when the signal transmitted from the GTI card is measured without the receiver, but with cable, connectors and 100Ω termination. This is not the case when the card is placed in loop back mode and the signal measured across the termination resistor immediately prior to the receiver (fig. 4). To rule out any PCB issue the eye diagram was measured in the same location, but on a separate unpopulated PCB (except for 100Ω termination resistor). The results were very similar to those in fig. 3.

![Figure 4](image4.png)

**Figure 4:** The eye diagram measured across the 100Ω termination resistor immediately prior to the receiver. The transmission path includes 1.5m InfiniBand cable and two HSSDC2 connectors. Horizontal scale = 100ps/div. Vertical scale = 150mV/div. Receiver switching threshold = +/- 100mV.

The start pulses are visible of the far left and right of fig. 5. A suspected reflection is visible approximately 3 divisions or ~4.5ns after the start pulse. The propagation delay of the 0.5m LEONI cable used here is unknown, but the nominal propagation delay of the comparable Amphenol cable is ~4.25ns/m. Consequently, the conclusion is that a reflection has travelled back to the transmitter and has been reflected again and thus when we measure it has traversed 1.0m. Soldering a 0201 package 100Ω resistor directly across the pins of the receiver did not improve the signal quality. The current system in USC55 is precarious and the intention is to replace it with the new GCT-GT interface described below as soon as possible.

![Figure 5](image5.png)

**Figure 5:** The signal measured across the 100Ω termination resistor immediately prior to the receiver. The transmission path includes 0.5m, InfiniBand cable and two HSSDC2 connectors. Horizontal scale = 1.5ns/div. Vertical scale = 200mV/div. Receiver switching threshold = +/- 100mV.
V. Optical Global Trigger Interface

The new interface to the Global Trigger is being built around a Xilinx Virtex 5 FPGA and 16 bidirectional optical links based on 4 POP4 transceivers. The Optical Global Trigger Interface (OGTI) will use the same dual CMC form factor as the original GTI card and will be capable of both transmitting and receiving data and thus be used at both GCT and GT end of the link. The GT will require a new motherboard to provide an interface to their custom backplane.

The Xilinx Virtex 5 (XC5VLX110T-3FF1136C) will operate up to 3.75 Gb/s, however the parallel POP4 optics manufactured by AvagoTech (HFBR-7934Z) and Zarlink (ZL60304) are specified for use up to 3.2Gb/s. Each POP4 contains 4 multimode transceivers operating at 850nm with multimode fibre interface. The baseline design is to run these links in the same asynchronous mode as those in the GCT-GT links, but at 2.4Gb/s rather than 2.0Gb/s to reduce latency. The latency from just the SERDES itself falls from 5.0bx at 1.6Gb/s to 3.3bx at 2.4Gb/s, and 2.5bx at 3.2Gb/s. It would therefore be useful to run the links as fast as possible. Initially the links will be filled with dummy words; however the possibility remains of being able to potentially transmit extra information to GT. Board layout is complete and it will be submitted for manufacture within the next few weeks.

VI. Conclusions

The high bandwidth available from high speed serial links and the integrated SERDES blocks within FPGAs make them attractive for high energy physics electronics; however, it should be noted that the two main hardware problems faced by the GCT project were both related to high speed serial links. This may, at least in part, be because the technology used was not as mature as it is now.

Operating the link in a semi-synchronous mode, in which data synchronised to the experiment wide TTC (Trigger Timing & Control) system is sent over an asynchronous, fixed and low latency link is not completely trivial. It has the advantage that the link reference clock can be provided by a low jitter local oscillator. The disadvantage is the complexity of the firmware, which must contain buffers to bridge the data from the link clock domain to the main TTC clock domain with a fixed and low latency. As local clock resources become a standard feature of FPGA fabric this should become easier.

VII. Acknowledgements

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Operation and Monitoring of the CMS Regional Calorimeter Trigger Hardware


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Abstract

The electronics for the Regional Calorimeter Trigger (RCT) of the Compact Muon Solenoid Experiment (CMS) have been produced, tested, and installed. The RCT hardware consists of one clock distribution crate and 18 double-sided crates containing custom boards, ASICs, and backplanes. The RCT receives 8-bit energies and a data quality bit from the HCAL and ECAL Trigger Primitive Generators (TPGs) and sends it to the CMS Global Calorimeter Trigger (GCT) after processing. Integration tests with the TPG and GCT subsystems have been successful.

Installation is complete and the RCT is integrated into the Level-1 Trigger chain. Data taking has begun using detector noise, cosmic rays, proton-beam debris, and beam-halo muons [1]. The operation and configuration of the RCT is a completely automated process. The tools to monitor, operate, and debug the RCT are mature and will be described in detail, as well as the results from data taking with the RCT.

I. INTRODUCTION

The Compact Muon Solenoid (CMS) is a general-purpose detector operating at the Large Hadron Collider (LHC). It is in the final stages of commissioning at the European Laboratory for Particle Physics (CERN) near Geneva, Switzerland. This large detector is sensitive to a wide range of new physics at the high proton-proton center of mass energy $\sqrt{s} = 14$ TeV [2]. First beam was seen September 2008 [1].

At the LHC design luminosity of $10^{34}$ cm$^{-2}$ s$^{-1}$, a beam crossing every 25 ns contains on average 17.3 events. These $10^9$ interactions per second must be reduced by a factor of $10^3$ to 100 Hz, the maximum rate that can be archived by the on-line computer farm. This will be done in two steps. The level-1 trigger first reduces the rate to 75 kHz, and then a High Level Trigger (HLT), using an online computer farm, handles the remaining rate reduction.

The CMS level-1 electron/phototon, $\tau$-lepton, jet, and missing transverse energy trigger decisions are based on input from the level-1 Regional Calorimeter Trigger (RCT) [3]. The RCT plays an integral role in the reduction of the proton-proton interaction rate ($10^5$ Hz) to the High Level Trigger input rate ($10^5$ Hz) while separating physics signals from background with high efficiency. The RCT receives input from the brass and scintillator CMS hadron calorimeter (HCAL) and PbWO$_4$ crystal electromagnetic calorimeter (ECAL), that extend to $|\eta|=3$. An additional hadron calorimeter in the very forward region (HF) extends coverage to $|\eta|=5$. A calorimeter trigger tower is defined as 5x5 crystals in the ECAL of dimensions $0.087 \times 0.087$ ($\Delta \phi \times \Delta \eta$), which corresponds 1:1 to the physical tower size of the HCAL.

II. RCT HARDWARE

A. PRIMARY RCT CARDS

Eighteen crates of RCT electronics process data for the barrel, endcap, and forward calorimeters. There is another crate for LHC clock distribution. There is another crate for LHC clock distribution. These are housed in the CMS underground counting room adjacent to and shielded from the underground experimental area.

Twenty-four bits comprising two 8-bit calorimeter energies, two energy characterization bits, a LHC bunch crossing bit, and 5 bits of error detection code are sent from the ECAL, HCAL, and HF calorimeter electronics to the nearby RCT racks on 1.2 Gbaud copper links. This is done using one of the four 24-bit channels of the Vitesse 7216-1 serial transceiver chip on calorimeter output and RCT input, for 8 channels of calorimeter data per chip. The RCT V7216-1 chips are mounted on mezzanine cards located on each of 7 Receiver Cards and the single Jet/Summary Card for all 18 RCT crates. The eight mezzanine cards on the Receiver Cards are for the HCAL and ECAL data and the single mezzanine card located on the Jet/Summary Card is for receiving the HF data. The RCT V7216-1 chips are mounted on mezzanine cards located on each of 7 Receiver Cards and the single Jet/Summary Card for all 18 RCT crates. The eight mezzanine cards on the Receiver Cards are for the HCAL and ECAL data and the single mezzanine card located on the Jet/Summary Card is for receiving the HF data. The V7216-1 converts the 1.2 Gbaud serial data to 120 MHz TTL parallel data, which is then deserialized, linearized, and summed before transmission on a 160 MHz ECL custom backplane to 7 Electron Isolation Cards and one Jet/Summary Card. The Jet/Summary Card receives the HF data and sends the regional $E_T$ sums and the electron candidates to the Global Calorimeter Trigger (GCT). The GCT implements the jet algorithms and forwards the 12 jets to the Global Trigger (GT).

The Receiver Card (shown in Figure 1), in addition to receiving and aligning calorimeter data on copper cables using the V7216-1, shares data on cables between RCT crates. Lookup tables are used to convert the incoming calorimeter energy into several scales and set bits for
electron identification. Adder blocks begin the energy summation tree, reducing the data sent to the 160 MHz backplane.

The Electron Isolation Card (shown in Figure 2) receives data for 32 central towers and 28 neighboring trigger towers via the backplane. The electron isolation algorithm is implemented in the Electron Isolation ASIC described below. Four electron candidates are transmitted via the backplane to the Jet/Summary (J/S) Card. The electrons are sorted in Sort ASICs on the J/S Card and the top 4 of each type are transmitted to the GCT for further processing.

To implement the algorithms described above, five high-speed custom Vitesse ASICs were designed and manufactured, a Phase ASIC, an Adder ASIC, a Boundary Scan ASIC, a Sort ASIC, and an Electron Isolation ASIC [4]. They were produced in Vitesse FX™ and GLX™ gate arrays utilizing their sub-micron high integration Gallium Arsenide MESFET technology. Except for the 120 MHz TTL input of the Phase ASIC, all ASIC I/O is 160 MHz ECL.

The Phase ASICs on the Receiver Card align and synchronize the data received on four channels of parallel data from the Vitesse 7216 and check for data transmission errors. The Adder ASICs sum up eight 11-bit energies (including the sign) in 25 ns, while providing bits for overflows. The Boundary Scan ASIC copies and aligns tower energies for e/γ algorithm data sharing and aligns and drives them to the backplane. Four 7-bit electromagnetic energies, a veto bit, and nearest-neighbor energies are handled every 6.25 ns by the Electron Isolation ASICs, which are located on the Electron Isolation Card. Sort ASICs are located on the Electron Isolation Card, where they are used as receivers, and are located on the J/S Cards for sorting the e/γ candidates. All these ASICs have been successfully tested on the boards described, and procured on in the full quantities needed for the system, including spares. The boards described have been produced using these ASICs and sufficient quantity has been obtained to fill 18 crates and create a stock of spares.
Zero (BC0), and other CMS control signals via an optical fiber from a TTCi (TTC input card) which can internally generate or receive these signals from either a Local Trigger and Control board (LTC) or the CMS Global Trigger.

The MCC includes a Clock Input Card (CIC) with a LHC TTCrm mezzanine board [5] to receive the TTC clocks and signals via the fibre and set the global alignment of the signals. The CIC feeds fan-out cards, a Clock Fan-out Card Midlevel (CFCm) and a Clock Fan-out Card to Crates (CFCc) to align and distribute the signals to the individual crates via low-skew cable. Adjustable delays on these 2 cards allow fine-tuning of the signals to the individual crates.

III. INPUT AND OUTPUT OF THE RCT

A. Trigger Primitive Generators - Input

The HCAL Trigger Readout (HTR) Boards and the ECAL Trigger Concentrator Cards (TCCs) provide the input to the RCT using a Serial Link Board (SLB), a mezzanine board with the V2716-1 mounted on it. The SLB is configurable, with two Altera Cyclone® FPGAs for data synchronization at the V2716-1, Hamming code calculation, FIFOs, and histogramming. The clocking for the SLB is separate from the HTR and TCC primary clocking to ensure data alignment at the RCT. The HTR can have up to 6 SLBs and receives data from the front end on fibres into its front panel. The TCC has up to 9 SLBs and also receives front-end data via a fibre to its front panel.

B. GCT Source Cards – Output

Each RCT crate is connected to GCT Source Cards, which convert the parallel ECL output of the RCT to optical, so that it may be sent easily to the lower floor of USC55. They are located in the RCT racks, directly above the RCT crates.

IV. OPERATION AND MONITORING

A. Commissioning the RCT at CMS

Installation of the RCT is complete. The RCT has 10 racks that hold a total of 21 RCT crates, 6 GCT Source Card Crates, and a crate for clock distribution to the SLBs (See Figure 5). The MCC and eighteen of the 20 standard RCT crates are part of the final system. The remaining 2 RCT crates will be used for local testing and storage.

B. Detector Slow Control and Rack Monitoring System

A custom monitoring system has been installed in each RCT rack. This system, at the heart of which is a Rack Monitor Card (RMC), monitors the status of the power supplies, fans and crate temperatures. A serial port on the card is attached to a serial-to-ethernet connection. PVSS [6], an object-oriented process visualization and control system, is used for the software interface to the RMC. Figure 6 shows a sample control panel for one of the racks. This software provides Detector Slow Control (DCS) and on-line monitoring of the system. System variables, such as current and temperature are histogrammed and stored in a database for later access. The entire system is integrated with CMS’s central DCS and the alarms and alerts are sent and recorded at a global level.
by hand. Figure 7 shows the panel for key input and the state machine.

Figure 7: RCT Trigger Supervisor window for programming the RCT based on a pre-defined key (middle). The state machine is on the right.

The RCT Trigger Supervisor also monitors the system status (Figure 8). Link and clock error states are checked and can be masked if needed using database or flat file. Error history is stored in a database. Alerts and alarms are implemented in an expert mode for now, but a system to send alerts and alarms to CMS Run Control is currently in development.

Figure 8: RCT Trigger Supervisor window for monitoring the RCT links and clock states. Problems appear highlighted in red, and are on a per-card basis. Holding the pointer over a specific error type provides information about which link is in error.

D. RCT Intercrate Tests

The RCT is able to cycle the addresses of its LUTs on the Receiver and Jet/Summary Cards to emulate up to 64 LHC bunch crossings. To debug the internal connections of the RCT all 18 crates are programmed and the GCT Source cards are used to capture the output.

A pattern is chosen, written to the LUTs, and the output is captured. This pattern is also fed to the Trigger Emulator (next section) and the output predicted is compared to the output captured and errors logged.

The bulk of the tests done so far have been internal, testing the timing of data sharing in and between the RCT crates. Patterns like walking zeros and ones, random, and simulated data were used. A number of small problems were found and fixed, and the timing was refined.

Currently this is a stand-alone program, but it will be integrated into the Trigger Supervisor. Expansion of the tests to use the pattern capability of the HTR and TCC boards to test the links is also underway.

V. DATA QUALITY

A. Trigger Emulator

The trigger emulator is a software package designed to reproduce the hardware response of the trigger exactly. It replicates all of the on-board logic including all configurable options such as hardware registers and Look Up Tables (LUTs). It is used for hardware validation and monitoring, and is currently in use during calorimeter trigger commissioning.

The trigger emulator is very versatile and can either use real data or pattern files to predict output. The files used by the HCAL and ECAL can be used as input to their TPG pattern generators and files of data captured by the RCT, GCT, and GT as output can be compared directly. In this way errors are tracked down in the software, hardware, and firmware. In reverse, the validation of the algorithms can be done by injecting physics patterns into the hardware pattern generators and verifying the output. Additionally, the Look Up Tables (LUTs) are generated by the emulator using input from the HCAL and ECAL TPG emulators, saved to files, and written to the physical LUTs via the Trigger Supervisor.

B. Global Runs and Data Taking

In order to get the detectors, all electronics, and data acquisition systems ready for data taking, there have been a series of “Global Runs” with increasingly more of the CMS detector included. In order to not interfere with the ongoing commissioning of CMS, these were designated periods of a week to a few days. They started in the fall of 2007 and continue up to and after first beam in fall 2008.

Various subsystems participated in the early runs, depending on their commissioning status. The RCT was able to participate in most runs after the commissioning of the GCT e/γ source cards. The flexibility of the RCT LUTs enabled the RCT to send either the HCAL or ECAL TPGs to the RCT e/γ path, and these were triggered on at the Global Trigger level. Separate keys for the Trigger Supervisor were created for each LUT configuration. Data was studied offline and later checked online to validate algorithms and detect any problems (next section).

C. RCT Data Quality Monitoring

1) Online Data Quality Monitoring (DQM)

In order to monitor the RCT as data is taken, real-time histograms are created and filled in the CMS High-Level-Trigger filter farm during data taking at a rate of about 10 Hz. A small set of selected histograms allows the shift...
crews to see if any problems have arisen. These include data validity checks with the emulator and comparisons to reference histograms that are highlighted if in error. One can also retrieve older runs with the same tool. A screenshot is shown in Figure 9.

Figure 9: Online DQM browser window for a recent run. Calorimeter triggering was with the ECAL barrel. Two ECAL modules were out for the run and can be seen as white space in the two occupancy plots. Each RCT region is a single square.

2) Offline DQM

For more detailed analysis of the RCT performance, offline DQM is very valuable. Access to a greater number of events is possible, and more histograms and a data array are stored for more detailed analysis. DQM can be run on CMS online machines for a near real-time analysis.

The trigger emulator is fed the TPGs from the data and the RCT response is predicted, providing efficiencies at the RCT region level (Figure 10). Plots of energy distributions and additional one-dimensional plots are able to show subtle differences and problems with triggering thresholds (Figure 11 and 12). In this way problems can be traced back to the hardware that caused them.

Figure 10: Non-isolated e/γ candidate efficiency for HCAL barrel as a function of eta index (horizontal, η=0 at 10 and 11 boundary) and phi index (vertical) of the RCT regions.

Figure 11: Non-isolated e/γ candidate rank (bits) as seen by the GCT. Threshold was at rank 15, and the rank from other triggers is seen below that.

Figure 12: Non-isolated e/γ candidate efficiency plotted on a one-dimensional scale (each bin is an RCT region). Smaller drops can be seen more clearly. This was a very early run and only a small portion of HCAL was included in the calorimeter trigger.

VI. FUTURE OPERATIONS AND PLANS

VII. CONCLUSIONS

The commissioning of the Regional Calorimeter Trigger at CMS is complete. A suite of tools for operation and monitoring the RCT has been developed and is mature. With DCS, internal testing, basic operation and configuration with the Trigger Supervisor, and analysis of the incoming data with the Trigger Emulator and DQM, this toolbox is essential for the RCT and its operators.

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Analysis of the initial performance of the ATLAS Level-1 Calorimeter Trigger

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Abstract

The ATLAS first-level calorimeter trigger is a hardware-based system designed to identify high-$p_T$ jets, electron/photon and tau candidates and to measure total and missing $E_T$ in the calorimeters. The installation of the full system of custom modules, crates and cables was completed in late 2007, but, even before the completion, it was being used as a trigger during ATLAS commissioning and integration. During 2008, the performance of the full system has been tuned during further commissioning and cosmic runs, leading to its use in initial LHC data taking. Results and analysis of the trigger performance in these runs will be presented.

I. INTRODUCTION

The Large Hadron Collider (LHC), the new CERN proton-proton collider, is designed to run at 7 TeV per beam and a nominal luminosity of $10^{34}$ cm$^{-2}$s$^{-1}$. With such a luminosity, each bunch crossing will generate 23 collisions, leading to a rate of $10^{9}$ interactions per second. However, most of these events will be minimum bias and not so interesting in the search for new physics. On the other hand, processes such as the Higgs boson production are 10 orders of magnitude below the proton-proton inelastic cross section, meaning that stringent selections will have to be applied to access such rare events.

Another constraint comes from the data storage performance, limiting the rate of data that can be recorded to tape to 300 MB/s. With an average ATLAS event size of 1.5 MB, the acquisition rate has to be reduced from the LHC bunch crossing rate of 40 Mhz down to 200 Hz, while keeping only the most interesting events. To achieve such a goal, ATLAS has designed a three-level trigger strategy as shown on figure 1.

![Figure 1: Overview of the overall architecture of the ATLAS Trigger system [1].](image-url)

The Level-1 Trigger (L1) [1] is composed of dedicated electronic boards and gets its input from the calorimeters and muon systems. It looks for basic physics signatures to take a trigger...
decision in less than 2.5 \( \mu s \) and it must reduce the trigger rate to a maximum of 100 kHz. At each Level-1 decision (L1A), the region-of-interest (RoI) event information is sent to the Level-2 Trigger.

The Level-2 Trigger (L2) \cite{1} accesses the regions of interest (RoI) generated by Level-1 using the full detector granularity. A large computer farm runs more detailed software algorithms to select events to reduce the trigger rate to 2 kHz with an average processing time of 40 ms.

The last trigger stage, called Event Filter \cite{1} (EF), has access to the full event information, and also to the calibration constants, to run offline-like reconstruction algorithms in order to limit the final recording rate to tape to a maximum of 1 kHz. At each Level-1 trigger decision (L1A), the event information is sent to the downstream Cluster Processor (CP) and Jet/Energy-sum Processor (JEP). Both of these processor systems run sliding window algorithms on the input matrix of trigger tower energies, looking for physics signatures. The Cluster Processor system identifies and counts \( e/\gamma \) and \( \tau \) candidates, while the Jet/Energy-sum Processor system counts jets candidates and also computes the missing and total transverse energy sums.

A set of Pre-processors (PPR) boards digitize the signals from the 7168 trigger towers using a 10-bit Flash-ADC, at a sampling rate of 40 MHz and add a pedestal of 40 ADC counts. The main role of the Pre-processors is to determine the final transverse energy value and to assign it to the correct bunch crossing (bunch crossing identification - BCID). The BCID mechanism uses a finite impulse response (FIR) filter to extract the signal amplitude and a peak finder algorithm to perform the signal peak identification, in either the linear or saturated regime. The coefficients of the FIR filter will be determined in order to maximize the signal/noise ratio. The output of the FIR filter is then passed to a look-up table (LUT) which is used for the pedestal subtraction, to perform noise suppression and to convert the final energy from ADC counts (10 bits) to GeV (8 bits).

The Pre-processors send the energy data from each trigger tower to the downstream Cluster Processor (CP) and Jet/Energy-sum Processor (JEP). Both of these processor systems run sliding window algorithms on the input matrix of trigger tower energies, looking for physics signatures. The Cluster Processor system identifies and counts \( e/\gamma \) and \( \tau \) candidates while the Jet/Energy-sum Processor system counts jets candidates and also computes the missing and total transverse energy sums.

II. LEVEL-1 CALORIMETER TRIGGER ARCHITECTURE

The Level-1 Trigger system is composed of three sub-systems: the Calorimeter Trigger \cite{2}, the Muon Trigger and the Central Trigger Processor (CTP), as shown in figure 2. Potentially interesting events are selected by identifying and counting the multiplicities, per \( p_T \) threshold, of \( e/\gamma \), \( \tau/\text{hadron} \), jets or \( \mu \) candidates, and also various energy summations. The CTP receives and synchronizes all these information from the Level-1 Calorimeter and Level-1 Muon and decides whether or not to generate a L1 trigger decision, according to a pre-defined trigger menu.

![Figure 2: Overview of the ATLAS Level-1 Trigger.](image)

The Level-1 Calorimeter Trigger (L1Calo) system is a digital pipeline partitioned into three sub-systems, as shown in figure 3. It receives signals from the electromagnetic and hadronic calorimeters, but works on a coarser granularity, based on trigger towers of size \( \Delta \eta \times \Delta \phi = 0.1 \times 0.1 \) in the barrel region.

![Figure 3: Overview of the ATLAS Level-1 Calorimeter Trigger system.](image)

In the case of the Cluster Processor system, the identification of physics signatures requires the sliding window algorithm to be applied in overlapping windows of \( 4 \times 4 \) trigger towers, from both electromagnetic and hadronic calorimeters, as shown on figure 4. To process each trigger tower, the physics algorithm must examine the neighboring trigger towers. The consequence is that a very large amount of information has to be duplicated...
between the processing units, modules and crates. For each window, the CP algorithm considers a $2 \times 2$ tower core region and an isolation ring around it in each of the electromagnetic and hadronic layers. Several energy thresholds are defined in the trigger menu to specify a minimum energy deposit in the electromagnetic core region or in the hadronic core one to distinguish between $e/\gamma$ and $\tau$ candidates. Thresholds are also set in the isolation ring for trigger items requesting an isolation criterion.

![Figure 4: The $4 \times 4$ trigger tower area (electromagnetic & hadronic) being considered by a Cluster Processor module when running its sliding window algorithm.](image)

The processor system is designed to provide real time output information to the Central Trigger Processor, where the ATLAS Level-1 trigger decision is taken. It also provides readout data at the L1A rate to the Data Acquisition system (DAQ) and generates the Regions of Interest information for the Level-2 Trigger system.

### III. COMMISSIONING

The Level-1 Calorimeter trigger system has been fully installed in the ATLAS electronics cavern since the end of 2007, when the production of the electronic boards was completed and the last modules were installed and cabled. The Level-1 Calorimeter system then entered an intense commissioning phase. A lot of systematic hardware, as well as software checks were performed. The system has been operating either in stand-alone or combined mode, together with the calorimeters, making effective use of their calibration systems (electrical or optical).

The Level-1 Calorimeter trigger was also involved in all the integration and data taking campaigns that have taken place over the last year. The data taking periods consisted mainly in looking at and recording muons produced in cosmic ray showers. This activity proved to be very useful to understand the data acquisition chain and to check further the analogue and digital parts of the system. The recorded information was also used for detailed comparisons with the calorimeter’s precision readout. The regular overnight runs were helpful to assess the system stability over a long period of time. In parallel a serious effort was made to set up the timing across the whole system and several calibration procedures have been developed for that purpose [3].

In the end it demonstrated that the Level-1 calorimeter system was behaving as intended and was able to generate reliable trigger decisions for the ATLAS detector.

#### A. Pedestal & noise level

To provide a robust trigger decision, the system has to have good control over the pedestals applied at the Pre-processor level and the amount of noise in the trigger towers.

Calibration procedures [3] have been developed to set up the pedestal levels at their nominal value of 40 ADC counts under control of DACs. However that procedure cannot set the pedestals to the desired value with a precision better than a few ADC counts. Therefore dedicated pedestal runs have to be recorded to measure the real pedestal level, check their stability and to monitor any possible shifts that would have important consequences on the trigger rates. Results of such a run are shown in figure 6. The average value of the pedestals over the 7168 trigger towers is close to the nominal value with a reasonable dispersion of few ADC counts.
The noise level for each trigger tower can be observed in figure 7. These graphics include the intrinsic Level-1 Calorimeter trigger noise but also the contributions from the calorimeters electronics. When the calorimeter electronics is switched off, the intrinsic Level-1 Calorimeter noise is about 1.4 ADC counts. Switching on the calorimeter typically raises this level to 3 ADC counts (with receiver gains set to 2). With the gains set at the expected level for \( E_T \) correction, the noise level is of the order of 400 MeV, varying with eta. It is possible from figure 7 to distinguish the regions where the calorimeter electronics were switched on, because of the higher noise level in the corresponding trigger towers. In the electromagnetic layer, only the barrel part (\(|\eta| < 1.4\)) was active, while in the hadronic layer the tile calorimeter barrel (\(|\eta| < 0.8\)), extended tile calorimeter (0.8 < \(|\eta| < 1.4\)), and hadronic end-cap (1.4 < \(|\eta| < 2.5\)) were active. It is also possible to spot on that figure a few temporary problems, like power supply issues in one of the Tile calorimeter drawers or in a liquid argon front end crate.

Less than 1% of the trigger towers (about 20 trigger towers) appear to be misbehaving, with either a pedestal level significantly different than expected or channels being abnormally noisy. Such channels are disabled to prevent fake trigger decisions while the origin of these problems is being understood and fixed.

**B. Correlation with calorimeters**

The Level-1 Calorimeter Trigger data path being independent from that of the calorimeters, it is extremely important to make sure that, for a given event, both systems reconstruct the same energy information.

Figure 8 shows such a correlation between the Level-1 Calorimeter Trigger readout and the calorimeter precision readout, from an overnight cosmic run. The transverse energy reconstructed by the Level-1 Calorimeter Trigger matches reasonably the readout from the calorimeters. Though not perfect, the correlation achieved is quite satisfactory, considering that the calibration constants used were far from being optimized.

In addition, the Level-1 Calorimeter system has been designed to work synchronously with the 40 MHz LHC clock, which is not the case when triggering on cosmic muons, which hit the detector asynchronously. It is therefore impossible to set the fine timing so that all cosmic muons are sampled correctly, which causes additional spread in the transverse energy reconstruction.
Figure 8: Correlation between the transverse energy $E_T$ (GeV) reconstructed by the Level-1 Calorimeter Trigger system and that from the calorimeter precision readout for the electromagnetic (top) and the hadronic (bottom) layers. The calorimeter transverse energy is computed as the $E_T$ sum of all the calorimeter channels belonging to the relevant trigger tower.

**C. $E_T$ thresholds & trigger rates**

Figure 9 shows the $E_T$ spectrum for $e/\gamma$ and $\tau$ hadron candidates found by the Cluster Processor system from a cosmic run. The different colors represent the $E_T$ thresholds, corresponding to different trigger items (1EM5, 1TAU5...), passed by the candidates. Up to 8 thresholds can be configured for the $e/\gamma$ candidates and another 8 for the $\tau$ ones. Different pre-scale settings can be applied individually to the trigger items to decrease arbitrarily the corresponding trigger rate. This is the case for example for the 1TAU10, 1TAU20 and 1TAU30 items shown in the $\tau$ graphic. Specific algorithms running at the Level-2 trigger or higher can also be used to reduce the trigger rate. This is the case in the $e/\gamma$ graphic of figure 9 for the 1EM5 trigger item, for which the number of candidates recorded is far smaller than for the trigger items requesting higher $E_T$ thresholds.

The study of long overnight cosmic runs showed that the trigger rates were most of the time stable, at a reasonable level of a few hertz, confirming the capability of the Level-1 Calorimeter Trigger system to trigger on genuine events. However, from time to time some calorimeter channels can become temporarily noisy and have to be masked out of the trigger decision. The tools to spot such noisy channels and to promptly disable them are being developed. Understanding the possible noise sources from the calorimeter is not an easy task but it is crucial to keep the trigger rates under control.

**IV. CONCLUSIONS**

The Level-1 Calorimeter Trigger has been running a complete system since the end of 2007. A big effort has been put into the commissioning of the system and its integration with the other ATLAS sub-detectors. The L1Calo has been part of the regular data taking periods for more than one year, recording signals from cosmic muons with an increasing involvement. The accumulated experience over the past months has allowed for better control over the system in term of stability and trigger rates. The Level-1 Calorimeter trigger is now fulfilling its main role to provide reliable trigger decisions to the ATLAS detector.

Waiting for the first collisions, the focus is on the development of the calibration procedures [3] (timing, energy calibration...) to improve the overall system performance and the trigger efficiency. Another important work area concerns the corrections to be applied for misbehaving or dead channels. This is a non-trivial task that will require further studies.

**ACKNOWLEDGEMENTS**

We wish to acknowledge the work of the ATLAS TDAQ community in providing the underlying online software and infrastructure for triggering, read-out and dataflow. We would also like to thank the ATLAS calorimeters communities for their effort to provide genuine input signals to the trigger. Finally the successful installation of the infrastructure and cabling would have been impossible without the careful work of many technicians connected to the institutes involved.

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Digital Signal Integrity and Stability in the ATLAS Level-1 Calorimeter Trigger

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Abstract

The ATLAS Level-1 calorimeter trigger is a hardware-based system with the goal of identifying high-$p_T$ objects and to measure total and missing $E_T$ in the ATLAS calorimeters within an overall latency of 2.5 $\mu$s. This trigger system is composed of the Preprocessor which digitises about 7200 analogue input channels and two digital processors to identify high-$p_T$ signatures and to calculate the energy sums. The digital part consists of multi-stage, pipelined custom-built modules. The high demands on connectivity between the initial analogue stage and digital part and between the custom-built modules are presented. Furthermore the techniques to establish timing regimes and verify connectivity and stable operation of these digital links will be described.

I. Introduction

The ATLAS trigger system consists of the hardware-based Level-1 trigger and two software-implemented high level trigger stages for further event selection. The ATLAS Level-1 trigger system provides a trigger decision within 2.5 $\mu$s and reduces the LHC bunch-crossing rate of 40.08 MHz to a rate less than 100 kHz. The Level-1 selection of interesting and rare events is based on reduced granularity calorimeter and muon detector data. The Level-1 trigger determines Regions-of-Interest (RoI) from which the algorithms of the next high level trigger are seeded. The high level triggers reduce the data rate to about 200 Hz for data storage. Trigger information is processed by the Level-1 calorimeter trigger and the Level-1 muon trigger. In the case of the Calorimeter trigger, the complete hardware components were tested in 2007 and finally installed in the end of 2007. This calorimeter trigger identifies electron/photon-like, tau-like and jet-like clusters above programmable transverse energy thresholds and compares the calculated energy sums against programmable thresholds. The results of the Level-1 trigger subsystems are combined in the central trigger processor (CTP) [1] which decides about the acceptance or rejection of an event. The latency of 2.5 $\mu$s is the maximum allowed time to transmit the signals from the calorimeter, to find high-$p_T$ objects and to receive the acceptance signal (L1A signal) from Level-1 trigger at the front-end electronics. The data transmission takes up most of this time. The architecture and the algorithms have to be simple enough to process over a large number of input signals in this limited time. The physics algorithms are performed by FPGAs which are flexible and fast. The algorithms use the mechanism of overlapping, sliding windows which requires transfer and sharing of a large amount of digital data between electronic modules. The different stages of processing data in the system need to be properly connected and timed in to allow optimal performance of the system. The system tests on the duplication and transmission of data within the digital part of the system and the timing procedure to ensure stable operation will be reported.

II. The ATLAS Level-1 Calorimeter Trigger

The basic architecture of the system is documented in [2]. A simplified schematic of the calorimeter trigger is shown in Figure 1. The real time data path consists of three subsystems: Preprocessor (PPr), Cluster Processor (CP) and the Jet/Energy-sum Processor (JEP). The Preprocessor which contains 124 modules is the initial analogue stage of the system. The PPr digitises the input channels and provides the input data for the CP and the JEP. The PPr consists of eight crates of 9U VME modules.
Their input data are analogue pulses mostly corresponding to a $0.1 \times 0.1$ in eta/phi space (so called trigger towers), separately for the electromagnetic and hadronic calorimeter compartments. The data is then sent downstream to the CP and JEP systems using LVDS 400 Mbit/s serial link chipsets. The Cluster Processor (CP) consists of 56 Cluster Processor Modules which locate and count electron/phonon and single tau/hadron candidates. The final results are then summed by the Common Merger Modules (CMM) and sent to the CTP. The Jet/Energy-sum Processor (JEP) consists of 32 Jet/Energy Modules (JEM) which count and identify jet candidates and calculates total and missing transverse energy. Their final results are also summed by CMMs. This digital part of the system occupies 6 custom-built processor crates with a high density backplane with 22000 pins to support the transfer of a very large amount of data. The read-out and Region-of-Interest data is handled by 20 Readout Driver modules (ROD). These receive the data on optical links running at a maximum speed of 800 Mbit/s. These reformat the data to standard ATLAS data fragments and transmit them using the ATLAS standard S-Link protocol.

The connections of the Preprocessor to the system processors CP and JEP are crucial issues for a working system. These connections consist of more than 1800 LVDS cables each carrying 4 separate input signals and additional data duplication links due to the sliding window algorithms. The read-out of the systems need to be properly aligned to ensure to read-out the correct event with its bunch-crossing identification. In the next section the tests for these connections and read-out links will be explained and the results for the system presented.

### III. Digital Signal Integrity and Stability

This section will concentrate on the results from the timing calibrations and the stability tests of the system. The system will be divided into three parts. These parts are illustrated in Figure 2. The sliding window algorithm [3] requires sharing and duplicating of the data in eta and phi. This overlap in eta and phi is created in two steps in the system indicated in the Figure 2. The incoming data is transmitted to both processor systems. These connections are LVDS 400 Mbit/s serial links between the Preprocessor crates and the JEP/CP custom crates, the so called inter-crate connections. The trigger towers are digitised to 8-bit transverse energy as input data for the CP system and 4 trigger towers are summed up to build 9-bit jet elements for the JEP system. The input data to both processors needs to be timed in (input timing scan). Furthermore within the processor systems data is shared via fan-in/fan-out between neighbouring modules with up to 160 Mbit/s in one crate and sent to the CMMs over a custom made high density backplane including VME connections. To latch the fan-in/fan-out data correctly and synchronously into the FPGAs for processing we need to calibrate the timing of each module. These connections are labelled as inter-module connections in Figure 2. The data is afterwards read-out via Glink optical fibres with a maximum of 800 Mbit/s (read-out links) and transmitted to the RODs.

Now the tests and timing procedure for these three type of connections will be described in detail.

#### A. Inter-crate Connectivity

The inter-crate connectivity is established by LVDS serial links which enter the modules through the backplanes. The LVDS cables transmit the input data to the CP and JEP systems. Every channel and every cable needs to be tested to verify the correct data transmission between the subsystems and also every input channel requires its own time settings. Because of device and cable skew all serial links operate on different phases. This connectivity is tested with the help of firmware integrated checks on status of the link and parity errors. Furthermore the data reception and processing can be tested with the help of the comparison between the simulation and the read-out of the hardware. The correctness of the cable mapping can be checked with a specific test pattern unique for every channel. These checks can find misconnected cables and hardware problems of cables, source or receiver modules and backplanes. These cabling problems were found at the 0.5% level, and these problems have been identified and fixed. The CP and JEP systems are driven by 2 deskew clocks (so...
called deskew 1 and 2) derived from the overall bunch clock (40.08 MHz). These clocks deskew the bunch clock to a sub-nanosecond accuracy to compensate delays of the input signals and to time in the fan-in/fan-out signals. These clocks have an adjustable delay of 240 steps each 104 ps long. The deskew 1 clock is responsible for the input synchronisation and these signals are latched into the FPGAs on one of two clock phases derived from the global LHC bunch clock (see Figure 3). This is the coarse time setting for the input signals. An additional offset in phase by a full tick would then need to be determined by diagnostic spy memories. This can then be corrected by applying programmable length pipelines in the FPGA to delay input data by a full tick.

The time settings for phase and delay of the input channels are established in a calibration run with synchronous data patterns by passing through all 240 steps of the deskew clock and reading out the parity error counters for each step. The delay is determined by calculating the misalignment between the data in each channel in units of clock ticks. The choice of the phase is made by analysing the number of parity errors in each phase and to choose the one with less errors. Such input timing scans are shown in Figures 4 in case of the JEP and in Figure 5 in case of the CP.

B. Inter-module Connectivity

This connectivity creates the overlap regions on every module to support algorithms based on sliding windows. Every module duplicates 3 out of 4 input channels and transmits them to its right and left neighbours. Figure 6 shows a schematic drawing of the traffic on the backplane for this purpose. The data is transmitted via the backplane connectors with a speed up to 160 Mbit/s. The backplanes have about 22000 pins.

The bars in Figure 4 and 5 represent the sampled parity errors for each time step. Some channels and serializers show slightly different behaviour because they are receiving data from different quadrants with a different timing (fan-out channels). These Figures show that the system has a good time margin of 15 out of 25 ns. So one chosen phase always will have valid data. This calibration procedure discovered a variety of hardware problems of which none was serious and all have been revised. Very few problems were found on the CP and JEP processor modules and a couple of problems on the Preprocessor modules.
latched in the FPGAs error-free. The time settings are determined by a fan-in/fan-out timing scan. This procedure enables 10-bit counters on each module, steps through each deskew 2 clock setting and samples parity errors for each clock step. This data is then analyzed to find a valid time window for processing the input data and the shared data. The JEP system works with a fan-in/fan-out data speed of 80 Mbit/s and the CP system works with twice this speed. One would expect that the valid time window is therefore about half of that from the JEP system.

Figure 7: Fan-in/Fan-out timing scan of one crate of the JEP with a signal speed of 80 Mbit/s

In Figure 7 a result of such a fan-in/fan-out timing scan is shown. The dark regions in the Figure mark where parity errors occurred. The actual time setting is then determined by choosing the point which is as far as possible away from the error bars. In general such a window would have a size of 5-7 ns which was proven to be sufficient for a error-free transmission. The CP system is similar but the data speed is 160 Mbit/s. The result of the timing scan shows four valid time ranges for different phases. One valid window size is about 2-3 ns. The timing procedure is equivalent and Figure 8 shows the result of a fan-in/fan-out timing scan of one CPM.

These procedures discovered hardware problems of the backplanes where connections were missing. These problems were caused on the one hand by difficulties at the production stage and on the other hand by damage during installation. All backplanes were additionally computer-scanned via a microscope in 2007. Each backplane had an average of 1-2 faults. In Figure 9 a bent pin which was damaged by module insertion can be seen. These problems were all fully solved.

Figure 8: Fan-in/fan-out timing scan of one CPM with a signal speed of 160 Mbit/s

Figure 9: Bent pin of a production backplane at CERN after module insertion

C. Read-Out links

The read-out links are running at a maximum of 800 Mbit/s using the Agilent G-Link protocol [5]. The read-out is initiated if the processors receive an acceptance signal from the CTP. For a functional read-out one needs to determine the so called read-out pointers for each subsystem to fetch the correct event which was accepted from the data buffers in the processors. Figure 10 illustrates this correlation.

Figure 10: Schematic of the data buffers in a subsystem

Offline analysis of special data can provide the correct time
settings for the read-out pointers. To determine these a standalone run with playback data is needed in which a fake L1A rate forces a read-out. The playback data only contains one event which is unequal to zero. The read-out always includes 5 adjacent time slices and therefore looking at the data stream provides you with information of the alignment of the system. This is illustrated in table 1.

<table>
<thead>
<tr>
<th>Default</th>
<th>0</th>
<th>0</th>
<th>data</th>
<th>0</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware output</td>
<td>0</td>
<td>data</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

These settings are necessary to match the data to a bunch crossing and are automatically checked in every read-out. In the commissioning phase the read-out was tested with random triggers up to 60 kHz and the result was that the event synchronisation was stable during a long running time.

IV. CONCLUSION

The hardware of the Level-1 calorimeter trigger was completely installed by December 2007. The years 2007 and 2008 was dedicated to the installation and commissioning of all components. The signal integrity was tested and proven by establishing and verifying the inter-crate and inter-module connectivity and read-out pointers. In detail the cabling and processors were fully tested and backplane connections are completely functional. The read-out pointers were confirmed in various data analysis. The procedures for establishing correct data processing were presented. Each subsystem is calibrated with respect to input data and fan-in/fan-out data. The system is has been exercised by taking cosmic-ray data for a long time, and is now ready for taking first collision data.

ACKNOWLEDGMENTS

We wish to acknowledge the work of the ATLAS TDAQ community in providing the underlying online software and infrastructure for triggering, read-out and data flow. We would also like to thank the ATLAS calorimeter communities, in particular those working on the trigger tower builders and receivers, for their efforts to provide genuine input signals to the trigger. Finally the successful installation of the infrastructure and cabling would have been impossible without the careful work of many technicians connected to the institutes involved.

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Evaluation of Multi-Gbps Optical Transceivers for Use in Future HEP Experiments

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Abstract

Future experiments at the European Organization for Nuclear Research (CERN) will increase the demand for high-bandwidth optical links. Custom developments for deployment within the detector volumes might be based on commercially available optical transceivers (TRxs).

We present our evaluation of Commercial Off-the-Shelf (COTS) multi-Gbps optical TRxs. This serves as the basis to evaluate the performance of the future Versatile Transceiver (VTRx) that is being developed at CERN in the context of the Versatile Link project. We describe the devices evaluated, the experimental set-up for parametric testing, and our analysis of the performance data.

I. INTRODUCTION

High Energy Physics (HEP) experiments, such as the ones currently undergoing commissioning at the Large Hadron Collider (LHC), require tens of thousands of optical links each in order to extract raw data from the detector and to distribute clock and control data to the front-end electronics. An upgrade of the current LHC (super LHC or SLHC), planned for 2016-18, is expected to increase the luminosity by an order of magnitude to $10^{35}$/cm$^2$/s, which implies more data to be transmitted (assuming more complex detector systems) and higher radiation doses. Since the optical links are also required to have low power dissipation and to reduce the mass inside the detector, the solution is to increase the bandwidth of each individual link.

Optical Links for SLHC are being developed in collaboration between CERN and other institutes [1]. This effort is divided into the GigaBit Transceiver (GBT) project and the Versatile Link (VL) project. The former covers the design of radiation-hard Application Specific Integrated Circuits (ASICs) and the implementation of the custom GBT protocol in an FPGA. The latter covers the system architectures and the basic building blocks required for the implementation of future single-mode (SM) and multi-mode (MM) optical links across the various SLHC experiments. A system outline is shown in Figure 1.

One of the main building blocks is the Versatile TRx module for on-detector deployment that will be available in both 850nm and 1310nm versions. The VTRx modules must operate in the innermost regions of a detector, where the magnetic field can reach up to 4T and the radiation field will be dominated by particles with energies around 300MeV at fluxes of maximum $10^8$ particles/cm$^2$/s [2]. In addition, the VTRx modules are required to work at multi-Gbps speeds, to have small size/mass and dissipate low power. To build the VTRx on the packaging know-how of the optoelectronics industry, the VTRx will be based on commercially available multi-Gbps optical TRxs by customizing only those aspects that are absolutely necessary.

To aid the selection of a TRx type for VTRx customization and to be able to evaluate and qualify the VTRx prototype modules we have developed test methods based on commercially available parts. We have set up test equipment, developed software tools and specified the evaluation criteria and test procedures. In the process, we have established performance benchmarks to which the VTRx modules can be compared.

This paper is structured as follows: Section II describes the parts that were evaluated. The test set-up and the metrics are the focus of section III. Section IV deals with the analysis of the performance data. Section V details the main conclusions of this work.

Figure 1: Radiation-Hard Optical Link for Experiments system outline.
II. DEVICES UNDER TEST

There are several families of commercial optical TRxs that target telecom and datacom applications. The bitrates of some of the standards are shown in Figure 2.

![Figure 2: Selected TRx families and their corresponding bitrates.](image)

Since the GBT protocol proposes a single lane running at a non-standard 4.8Gbps, there are only a few families of TRx modules that could be used for VTRx customization. Taking dimensions and power dissipation into consideration, we decided to evaluate three families: Small Form Factor Pluggable (SFP), Enhanced SFP (SFP+) and 10 Gigabit SFP (XFP). These module types are hot-pluggable serial-to-serial data-agnostic multirate optical TRxs used to implement SM or MM links. A picture of the modules is shown in Figure 3.

![Figure 3: Three modules from the selected TRx families.](image)

The maximum power dissipation found in SFP modules is 1.0W and the SFP+ specification allows for two power levels: up to 1.0W and up to 1.5W. Both the SFP and the SFP+ require the host board to provide a +3.3V supply. XFP modules must meet one of four power levels: up to 1.5W, up to 2.5W, up to 3.5W and higher than 3.5W. The XFP specification requires the host board to provide three supplies: +1.8V, +3.3V and +5V and allows for an optional -5.2V.

The SFP+ SFF-8431 [3] specification is an expansion of the original SFP INF-8074i [4] specification plus the SFF-8472 [5] specification for Digital Optical Monitoring (DOM). As a consequence, both modules types have the same basic components: the Transmitter (Tx) has a Laser Diode Driver (LDD) and a Transmitter Optical Sub-Assembly (TOSA); the Receiver (Rx) has a Receiver Optical Sub-Assembly (ROSA) and a post-amplifier (AMP). The TOSA includes a Laser Diode (LD) and a monitor photodiode; the ROSA includes a Photodiode (PD) and a Transimpedance Amplifier (TIA). There is also a microcontroller and a memory inside the module for serial ID, Digital Optical Monitoring (DOM) and to control the module operation. The block diagram of an SFP/SFP+ module is shown in Figure 4.

![Figure 4: Block diagram of an SFP/SFP+.](image)

The XFP [6] differs from the SFP/SFP+ by requiring a signal conditioner – Clock and Data Recovery unit (CDR) – in both Tx and Rx paths which resamples the data and resets the jitter, but also restricts the bitrates. The signal conditioner in the Rx path may include an amplifier to reduce the number of Integrated Circuits (ICs). The Serializer/Deserializer (SerDes) must be on the host board for all three modules.

During the course of this work we evaluated twelve commercial TRx modules. The devices and their main characteristics are shown in Table 1. The receivers of these TRx modules are all PIN-based and the 850nm semiconductor lasers are VCSELs. The 1310nm semiconductor lasers are either Distributed Feedback (DFB) diodes or VCSEL diodes.

III. TEST SET-UP AND PERFORMANCE METRICS

To evaluate an optical TRx we must collect a set of metrics capable of quantifying the performance of its Tx and Rx parts [7]. We should also measure the power dissipation of the entire TRx module. Thus, the evaluation of an optical TRx module was divided in three parts: Tx performance, Rx performance and TRx power dissipation.

For each of the three TRx types we used a specific testboard in which a module is plugged. A picture of a testboard used for SFP+ modules is shown in Figure 5.

![Figure 5: Testboard used for SFP+ modules.](image)

Table 1: List of evaluated transceivers and their main characteristics.

<table>
<thead>
<tr>
<th>Device #</th>
<th>TRx Type</th>
<th>Wavelength [nm]</th>
<th>Max Bitrate [Gbps]</th>
<th>LD/PD type</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SFP</td>
<td>850</td>
<td>4.25</td>
<td>VCSEL/PIN</td>
<td>1/2/4GFC; 1000BASE-SX</td>
</tr>
<tr>
<td>2</td>
<td>SFP</td>
<td>1310</td>
<td>4.25</td>
<td>VCSEL/PIN</td>
<td>1/2/4GFC; 1000BASE-LX10</td>
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<tr>
<td>3 and 4</td>
<td>SFP+</td>
<td>850</td>
<td>10.5</td>
<td>VCSEL/PIN</td>
<td>2/4/8/10GFC; 10GBASE-SR</td>
</tr>
<tr>
<td>5 and 6</td>
<td>SFP+</td>
<td>1310</td>
<td>10.5</td>
<td>DFB/PIN</td>
<td>2/4/8/10GFC; 10GBASE-LR</td>
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<tr>
<td>7</td>
<td>XFP</td>
<td>1310</td>
<td>10.3</td>
<td>DFB/PIN</td>
<td>10GBASE-LR/LW</td>
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<tr>
<td>8 to 12</td>
<td>SFP+</td>
<td>1310</td>
<td>10</td>
<td>VCSEL/PIN</td>
<td>Prototype for 10Gbps over SM fiber</td>
</tr>
</tbody>
</table>
Figure 5: SFP+ testboard with TRx module and cables.

A. Tx Evaluation

When evaluating the performance of an optical Tx we are interested in the characteristics of its optical output signal. For the purpose of our study we focused on power levels and general waveform characteristics. This information can be extracted from the Tx optical eye diagram using Set-up A shown in Figure 8.

The clock synthesizer is a Centellax TG1C1-A, the pattern generator is a Centellax TG2P1A and the scope is a LeCroy SDA100G with an SO-10 optical sampling module. A PRBS7 pattern whose characteristics are known is provided to the Tx input via the testboard and the Tx output is then measured by the sampling scope. No signal is provided to the Rx input and its output is terminated in the testboard.

Figure 6: Tx eye diagram and definition of selected measurements.

We wrote a LabVIEW program that controls the instrumentation and automates the data acquisition. It runs through a list of bitrates (from 0.5Gbps to 12.5Gbps) and saves the performance data. This comprises the raw eye diagram, the jitter bathtub curve [8] and the values of various measurements (including rise/fall times and jitter). We then process the eye diagram to extract a few additional measurements: average power, OMA, ER and vertical eye closure in the 20% center window. The details are shown in Figure 6.

In Table 2 we propose a Tx performance specification for the module operation at 5Gbps, which is slightly faster than the current GBT protocol (4.8Gbps). It is based on the 4G Fibre Channel (4GFC) [9] specification with some values adjusted to the higher bitrate. The Tx maximum jitter is the 4GFC Tx jitter budget, not including the jitter of our test set-up.

Table 2: Tx specification proposal for 5Gbps operation.

<table>
<thead>
<tr>
<th>#</th>
<th>Spec.</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>OMA</td>
<td>300</td>
<td>μW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>ER</td>
<td>3</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Eye Closure</td>
<td>60%</td>
<td>% of OMA</td>
<td>65 ps</td>
<td>20%-80%</td>
</tr>
<tr>
<td>5</td>
<td>Fall Time</td>
<td>65 ps</td>
<td>20%-80%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Total Jitter</td>
<td>0.25 UI</td>
<td>@BER=10^{-12}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Det. Jitter</td>
<td>0.12 UI</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Tx Mask M.</td>
<td>0</td>
<td>%</td>
<td>Figure 7</td>
<td></td>
</tr>
</tbody>
</table>

Point 8 of the specification in Table 2 is a mask margin test. The Tx relative mask defines an area that the optical eye diagram must not cross and is used to keep the overshoot/undershoot/ringing under control. The mask in Figure 7 is based in the 4GFC Tx mask with slope adjusted to the previous specification and to the jitter of our test set-up. The arrows define the expansion of the mask from 0 to 100% to quantify the mask margin.

Figure 7: Tx eye diagram and Tx mask definition.

B. Rx Evaluation

To evaluate the performance of an optical Rx we measure the Bit Error Rate (BER) curve and extract the Rx sensitivity (minimum OMA for a BER of 10^{-12}). We also measure the electrical swing and the jitter of the Rx output. Figure 9 shows the two set-ups required for this evaluation.

Figure 8: Set-up to evaluate the Tx part of a TRx module.
Figure 9: Set-ups used to evaluate the Rx part of a TRx module.

The electrical signal from the PRBS generator or the FPGA is first converted to optical by a reference Tx and then its power is controlled and measured by an Optical Level Attenuator (OLA) and a Power Meter (PM). The attenuated signal is then fed to the Rx input and its electrical output is finally sampled by a LeCroy SDA100G with an electrical module (ST-20) or compared with the original electrical signal generated by the FPGA.

To automate Set-up B we wrote a LabVIEW program that runs through a list of bitrates/attenuations and stores the following data: Optical input power, raw eye diagram and jitter bathtub of the electrical output and several additional measurements (including the jitter components). In Set-up C the BERT was implemented on an FPGA board from Xilinx using their reference design. A LabVIEW program automates this set-up by running through several attenuations and saving the BER data.

In Table 3 we propose a specification for the Rx operation at 5Gbps. The Rx maximum jitter is the 4GFC Rx jitter budget. The OMA of the input signal for the jitter measurement and the Rx sensitivity are mid values between the 4GFC requirements for MM and SM links.

Table 3: Rx specification proposal for 5Gbps operation.

<table>
<thead>
<tr>
<th>#</th>
<th>Spec.</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
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<tr>
<td>9</td>
<td>Total Jitter</td>
<td>0.26</td>
<td>UI</td>
<td>@BER=10^-12, OMA=90 µW</td>
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</tr>
<tr>
<td>10</td>
<td>Det. Jitter</td>
<td>0.11</td>
<td>UI</td>
<td>OMA=90 µW</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Rx Mask Pass</td>
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<td></td>
<td>Figure 10</td>
<td></td>
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<tr>
<td>12</td>
<td>Sensitivity</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 10: Rx eye diagram and Rx mask definition.

The absolute mask of Figure 10 defines the limits for the electrical swing and is based on the SFP+ high-speed specification (XFI) with the horizontal limits adjusted to the previous jitter specification and to our test set-up. This is a simple pass/fail test and we do not quantify the margins.

C. TRx Power Dissipation

The TRx power dissipation is evaluated by measuring the current being supplied to the testboard when the TRx is operating in optical loopback. The testboard is required to be a clean board (no electronics) or we must be able to subtract the current supplied to the testboard electronics.

As point 13 of our specification, we propose a maximum of 600mW of TRx power dissipation (end-of-life value and across all operating temperatures). Our experience with commercial TRxs tells us that this specification might be too demanding for non VCSEL-based modules.

IV. RESULTS

The previous test set-ups can generate a very large data set and we will focus on the TRx performance at 5Gbps. We flagged the devices that do not meet our specification proposal for 5Gbps operation and we developed a Figure of Merit (FoM) to combine all the performance data into three numbers: TxFoM for the Tx, RxFoM for the Rx and PwrFoM for the TRx power dissipation.

The FoM numbers are defined in the following three expressions, in which the weight factors were chosen to reflect our assessment of the relative performance of all twelve devices. The Tx mask margin has a value between 1 and 2 if the eye passes the mask test and a value lower than 1 if it does not. If the TRx performance equals the specification in every point then the FoM value is 100, but a value higher than 100 does not necessarily mean that the device complies with all points of the specification.

\[
Tx_{FoM} = \frac{100}{15} \times \left( \frac{OMA}{OMA_{spec}} + \frac{\text{Rise}_{spec}}{\text{Rise}} + \frac{\text{Fall}_{spec}}{\text{Fall}} + \frac{3 \times \text{Rise}}{Tj} + \frac{3 \times \text{Fall}}{DJ} + \frac{\text{Closure}}{\text{Closure}_{spec}} + \frac{\text{ER}}{\text{ER}_{spec}} + \frac{\text{FallMask}}{\text{3 \times CenterMask}} \right)
\]
The FoM results for our twelve devices under test are shown in Figure 11. The upper graph is the Tx performance, the middle is the Rx performance and the lower is the TRx power dissipation. The vertical scale is in arbitrary units and dashed gray bars indicate that at least one of the specification points has not been met.

The FoM results for our twelve devices under test are shown in Figure 11. The upper graph is the Tx performance, the middle is the Rx performance and the lower is the TRx power dissipation. The vertical scale is in arbitrary units and dashed gray bars indicate that at least one of the specification points has not been met.

V. Conclusions

The future VTRx modules will be built from radiation-qualified optoelectronic components by customizing a commercial TRx with ASICs sourced by the GBT project. Using commercial devices we have developed test methods for TRx testing and a FoM that allows a quick and easy comparison of different modules. This enabled us to select a TRx type for VTRx customization and will allow us to evaluate the performance of the future prototype VTRx modules.

The results from our evaluation of twelve commercial TRxs show that the SFP+ is the most suitable candidate for VTRx customization and that we should target a VCSEL-based VTRx to achieve low power dissipation. Our evaluation of TRxs also shows that, although 1310nm VCSELs are not yet a mature technology, there are diodes capable of being operated at 5Gbps with sufficient performance.

REFERENCES

Experiences with the ATLAS Pixel Detector Optolink and Researches for Future Links

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\textbf{Abstract}

The ATLAS Pixel detector has been installed in its final place into the ATLAS cavern in July 2007. After providing all the necessary connections, the final testing and commissioning has been performed before the first beam was circulated through the LHC in September 2008.

The connection between the 1744 detector modules and the readout electronics in the counting room is done via optical links, that have to be commissioned and tuned in order to be able to send commands to and receive data from the modules.

Tests for optical and electrical functionality of components during production and assembly sorted out failing parts. The commissioning work on the installed detector showed more than 97\% of the system being functional.

The procedure of the commissioning work and observed issues on the system layout and function are discussed and brought into an outlook for future optical link designs.

I. THE ATLAS PIXEL OPTICAL READOUT

The optical readout of the ATLAS Pixel detector ([1], [2]) is a per module connection between the off-detector readout systems and the on-detector optical components, containing several custom made components both on- and off-detector ([3]). The off-detector components of the optical link are located on the Pixel Back of Crate (BOC) Cards, whilst the on-detector components make up the optoboards.

The 132 BOC cards are located in the Pixel readout crates in the counting room USA15, around 80m away from the detector itself. Each BOC card is paired to a Readout Driver (ROD, [4]) and interfaces it to the modules, and the readout buffers. The optical to electrical conversion is done on small plugins assembled to the BOC cards, the Tx- Plugins for the downlink and the Rx-Plugins for the uplink.

The optoboards are mounted to service panels in around 1m distance to the detector modules and connected to them electrically. Each optoboard is connected to 6 or 7 modules, which belong to a half stave in the barrel region or a sector in the disks. It serves one downlink to each module and one or two uplinks. The optoboards are mounted on service panels, which are mounted to the detector and form the patch panels nearest to the detector.

The downlink into the detector sends clock, trigger, command, and configuration signals (Timing, Trigger, and Control TTC) into the detector. The link is DC-balanced using a BiPhase Mark (BPM) encoding in order to send clock and data via a single line into the detector. This was found to be particularly useful, since the encoder only adds about 65 ns latency to the command stream, which is acceptable for the trigger latency. The receiving chip on-detector is the Digital Optical Receiver Integrated Circuit (DORIC), localized on the optoboards. The threshold for recognizing bits is automatically set to 50\% of the incoming input signal by the receiver circuit. Afterwards the BPM signal is decoded into clock and data and sent to the pixel detector modules. The decoding is done per channel, such that each module receives individual clock and command. Inside the BPM encoder, each stream can be delayed individually in steps of 320ps. The individual phase shift with respect to the LHC Bunch crossing clock increases the efficiency for the detection of low charge hits.

The optical uplink is composed of an on-detector transmitter, the VDC (VCSEL Driver Circuit) driving a Vertical Cavity Surface Emitting Laser (VCSEL), and an off-detector receiver integrated circuit, the DRX. Data are sent as an NRZ stream to the off-detector electronics, thus no active decoding is needed. The signal is not DC-balanced, hence no automatic threshold adjustment can be performed here. Instead the threshold must be manually set between 0 and 255 uA. Phase adjustment of the returned data happens manually on the BOC, using PHOS4 integrated circuits (0 to 24 ns Phase adjustment with 1 ns step size).

The optical fibres are a spliced combination of radiation hard and radiation tolerant fibres, bundled into 8-way ribbons. Only 6 or 7 channels of this connection are used, depending on which geometrical units are read out. The eighth connection is disabled by design on the optoboard, but is usable in the off-detector electronics.

ATLAS Pixel modules have two data outputs which can be set to work at different modes: 1x40, 1x80, 2x40 and 2x80 Mb/s. Depending on their physical location and the corresponding occupancy expected during runtime, the data is given to the optoboards at different bandwidth and on either one or two channels.

Depending on the detector occupancy, there are two flavours of optoboards with either 8 or 16 inputs, which are
transmitted via either one or two ribbons to the same number of RX-Plugins.

The ROD, that receives the data from the BOC Card and builds an event fragment out of them, can only cope with 40 MBit/s inputs, therefore all 80 Mbit/s data streams are split into two 40 Mbit/s streams inside a logic built into the Pixel BOCs. This needs particular attention when adjusting signal phases.

II. IMPLICATIONS OF THE CHOSEN LAYOUT

The choice of the hardware was driven by the position in the setup and the accessibility during runtime, leading to different properties for on- and off-detector components:

A. On-Detector

The on-detector components ([5]), incorporated into the optoboard are inaccessible during runtime, therefore a lot of features were included to make them operable under harsh conditions and without user intervention.

The automatic threshold adjustment of the DORIC is meant to work from an average input current of 4000 uA down to less than 40 uA, thereby basically allowing any light input to drive the system in stable conditions. It cannot correct for wrong input duty cycles, which directly influences the output clock quality. These are adjusted on the signal itself by the sending instance, the BPM.

There is only one parameter for transmission, the laser forward current generated by the VDC. \( V_{\text{set}} \), the voltage controlling the light output power of an optoboard, is adjusted for all 8 or 16 channels at a time via an external voltage set by the Detector Control System (DCS). Since the lasers have slightly different thresholds and the connection quality varies per channel, it is normally not possible to find an ideal setting for all channels. The best average tuning has to be chosen instead. Foreseeing possible degradation of the lasers due to irradiation, high power versions were chosen, which give a fibre coupled output power of 3mW peak in average, but might about 7mW peak amplitude for some channels (cf. [6]).

B. Off-Detector

The off-detector components are located in the ATLAS counting rooms. They can be accessed during the life time of the detector. The BOC cards and RODs are controlled via single board computers, of which one is installed in each readout crate. The optimization of the parameters for the optical link can be done remotely by performing and analysing tests for the installed detector and optical link.

The transmission parameters to be adjusted for each channel are the laser forward current, two different delays in the transmission line, coarse and fine, and the Mark-to-Space Ratio (MSR). The on-detector clock reconstruction is based on transitions of the incoming signal and thus depends on the mark-to-space ratio of the signal. If not tuned properly, two clock modes with different periods exist on detector (see Figure 1), one between rising and falling edge of the BPM stream and another one between falling and rising edge. The adjustment of the mark-to-space ratio influences the phase of the on-detector clocks. Adjusting the fine-delay of the signal influences the mark-to-space ratio, which needs to be taken into account, when tuning the system for optimal transmission parameters.

Reception parameters are the threshold applied to the incoming PiN current and the phase adjustment to the incoming signals, such that all received signals on a single BOC can be registered with a common clock.

The current response of the PiN diode has a characteristic slow component, generated by a low-field region inside the PiN volume, when fed with a light pulse. Therefore the signal response does not have perfectly steep edges and with higher signals, a higher noise floor is introduced. The DRX is only capable of applying a maximum threshold current of 255 \( \mu A \), which is typically over-steered with an input signal swing of about 2mA. This again translates into a fibre coupled light power of \( \sim 3\text{mW} \) reaching the PiN diode. Higher signals can lead to a situation in which the system is not able to reconstruct data, because the DRX input contains only of the noise floor.

III. COMMISSIONING WORK

A. Installation and Testing

The electronics and fibres were extensively tested during production, where individual testing was possible. The full link was then commissioned on site by either communicating with the detector or with special tools, like loopback fibres and an Optical Time Domain Reflectometer (OTDR).

OTDR measurements have shown that most of the fibres are in good shape even though the installation conditions, e.g. time and space constraints, were not as good as in standard telecommunication fields.

Loopback fibres identified misaligned TX-Plugins and malfunctioning TTC channels. The I/C curves resulting from the loopback tests were recorded using low level software running directly on the crate (Example see Figure 2).

The complete Pixel detector package was tested including the operation of the optical link in a connectivity test at the surface and in the cavern. The correct connection and the capability to address each detector module has been tested and verified.

B. Tuning of Parameters

Tuning of all parameters is done via software from the Data Acquisition System (DAQ), as these can communicate with the modules, take data with the system, and control most
of the transmission parameters directly via communication inside the readout crates. Only the optoboard light power is to be adjusted via DCS. Tuning $V_{\text{Iset}}$, RX-threshold and RX-delay is compulsory, since they are needed to reconstruct data returned from the pixel detector modules. For a complete tuning of the optical link all the parameters have to be addressed, which will be described in the next sections (see also [7]).

The optimizing of the mark-to-space ratio is done by configuring the detector modules to send back half the incoming clock (20 MHz clock-like data signal). Now in the RX-path on the BOC the incoming positive pulse width can be measured by sampling the data with a 20 MHz clock and adjusting all possible phases between 0 and 49 ns. Flipping the BPM signal versus returned clock phase by sending a single one (without affecting any other parameters), the on-detector clock modes are exchanged so that the returned positive pulse width correspond to the other on-detector clock mode (see Figure 4). The ideal setting can now be found by adjusting the MSR to give the smallest difference between the two measured pulse widths (cf. Figure 5).

$V_{\text{Iset}}$ tuning has to be performed for all channels connected to the same optoboard at the same time. Since low power channels prefer higher settings of $V_{\text{Iset}}$, while high power channels prefer lower ones due to the saturation effects in the RX PiN diodes, the recent tuning algorithms for $V_{\text{Iset}}$ incorporate a measure for the quality of RX-threshold tuning at the corresponding $V_{\text{Iset}}$, which directly reflects the light power incoming to the RX-Plugin. The target is set to have an average threshold tuning of more than 200 µA, such that the output signals from the optoboard are reasonably high and stable, as the lasers are driven well above their threshold currents.

RX-thresholds are tuned such that the range of delay settings, which can be used, is maximal, meaning the return bit width is equal to one clock cycle. This effectively gives a threshold below 50% of the returned signal size, since the lasers have a non-negligible turn-on time and the PiN-diodes response function gives signal edges a smaller slope. The intersection of rising and falling edges thus happens at thresholds lower than 50% of the signal size. In case a

![Figure 2: Loopback test result showing different increases in fibre coupled light power with increase of laser forward current setting.](image)

![Figure 3: PiN currents produced by all TTC-lasers in use in the ATLAS pixel detector](image)

![Figure 4: Flipping the phases between BPM stream and returned half clock](image)

![Figure 5: Resulting plot from Mark-to-Space Ratio tuning showing the difference between adjacent clock cycles on-detector - The ideal setting is the closest to zero difference.](image)
The threshold is tuned to the maximum allowed setting and the signal is still wider than 27.5 ns it is counted as an overshoot for the tuning of $V_{\text{iset}}$ causing it to be decreased.

RX delay is set such that the sampling point for registering data off-detector is about 5 ns before the edge transition from one bit to another. Signals have proven to be more stable after settling for a few ns, whereas right after the transition, the amplitude fluctuates, depending on the number of previously sent ones and zeros. (See Figure 6 - Transitions happen from right to left Time is invers to RX-delay)

TTC-delays have generally not been adjusted yet. They will optimize physics performance (see [8]) by shifting the timing of the Pixel detector to have a sampling window for one bunch crossing start right when the first charges arrive. The detector is slower in receiving low charges and thus might shift these into the next sampling cycle. The optimal setting is obtained when the timing window starts at the arrival time of the highest readable charge.

Bandwidth adoptions are done inside the BOC. After switching the decoding mode from simple forward 40 Mb/s to demultiplexing (80/160 Mb/s), all that needs to be done is readjusting the signal delay, to be on average 3ns less, because the decoding introduces an extra 3ns delay inside the BOCs integrated logic.

**IV. Environment Control**

The optoboards are cooled via the same evaporative cooling system used for the modules of the Pixel detector. This cooling provides an operation temperature of about 5°C measured on the optoboards. The lasers used on the optoboards are optimized for an operation temperature of 20°C and some of them give no more light output when operated at temperatures much lower than that (measurements during production showed basically no light output at -25°C). Therefore a heating system was added, to heat the optoboards up to a programmable temperature.

Operating the optoboards without this cooling system still gives reasonable output for most optoboards, when operated with a 50% link occupancy as is used for tuning the system (half-clock return signal from the module). Switching to calibration scans that have a lower link occupancy, the average light output power drops due to the local induced heat inside the lasers not being high enough. Hence the tuning of the link succeeds, but leaves the system in a state unusable with lower link occupancies. This problem is called Slow turn-on, because the light power level increases during operation of the laser and heats the device. To avoid loosing the first bits the heaters are used to heat up the lasers to a higher temperature and therefore keeping them in a more stable operating condition.

**A. Production Issues**

When operating the system during commissioning of the ATLAS Pixel detector in its final position (installed inside of ATLAS and connected to the final readout system) single TTC channels started failing by not transmitting any light. This behaviour was shown to be compatible with ESD damage during early production of the TX-Plugins. The ones that were damaged by ESD died after a limited operation time, sometimes up to some month.

**Figure 6: RX-delay versus RX-threshold (fast) BocScan. White regions received an expected number of one and zeros during the scan (Comparable to a single phase eyepattern)**

The ESD damage cannot be tracked down in the system, as the only hint before losing light output power is a change in the IV-characteristics of the laser diodes: the knee voltage of the affected laser drops slightly whilst the slope beyond threshold rises. An example curve is shown in Figure 7.

A new batch of Tx-Plugins is been produced under stricter precautions against ESD. The intensive handling, which is necessary during the production of the plugins, is a point of high risk in the production procedure and must be controlled intensively.

**V. Research for future links**

The experiences, which have been made in the production and the operation of the present optical link, should be introduced into a design of a new optical link for the next generation detectors. Many points hidden in the details can be improved and make the life for the experts and operators of the optical links easier and more convenient. We want to describe some of them in this last chapter.

**A. Layout Improvements**

The layout of the optical transmission path can be improved by some modifications on both ends. The TTC link...
sending from the counting room to the detector is working very robust and stable. This suggests to include some of the features of the TTC link into the data link.

A DC-balanced transmission, as it is implemented in the present TTC path is to be part of the next optical data path as well, since it gives the possibility to automatically set up the input threshold as well as the phases of the signals. Instead of measuring the phase of on-detector clocks by scanning in order to get timing information, one could have the phase be measured by the system all the time, hence delivering stability information. This would solve two basic tune steps, the adjustment of the receive threshold for recognizing the incoming data and the generation of one or two clocks to register the data correctly before passing it to further parts of the readout system.

This means of course that on the off-detector side as well as on the on-detector part the components of the link have to be revised to include the wished features,

Packaging has already been a major design aspect in the recent optical link, and will be for the next one. As could be seen from features like the slow turn-on, the thermal behaviour is not fully under control. Thus packaging needs to get a higher thermal conductance and the behaviour of lasers needs to be carefully checked whilst setting up components for the next optical link. The adoption of the operating temperature to the one, which is the best for operating the lasers, is crucial. For this the requirements of packaging, board design, and material choosing is to be conciliated. Important tests of the system under the real conditions which will appear in the final detector place are very important and should be enforced to take place as early as possible.

**B. (Electrical) Features to be added**

The ESD failures seen during commissioning of the recent link are the result of a post-mortem analysis showing a difference for different lasers. A control mechanism inside the system does not exist and the sanity status of the separate components can only be determined by judging the complete transmission chain behaviour. Features inside the individual components or on the cards where they are located can help to investigate the status and sanity of the single parts.

Embedding a possibility to measure IV curves of the used lasers in-situ would give a handle on recognizing a possibly damaged laser before it dies and estimating needs for replacements. Since the lasers are localized on off-detector boards which can serve an additional circuit to be able to measure this kind of parameters, it is worth to include this feature. The on-detector situation is different due to the space limitations. An external measurement circuit will not be introduced, but including an ADC which controls voltages and currents might be possible inside a chip itself.

Another feature to be introduced is the possibility of checking the correct data transmission. In the present design, the TTC signals can only be transmitted in encoded form. A data check needs therefore always a decoding part. On top of a only data or only clock transmission mode a possibility to loop back the signal for test purposes at several places would be very useful. To check the data before the electrical to optical conversion or after the optical transmission by sending it directly back can help to debug and qualify the data transmission quality in situ.

The last point is to increase the transmission speed of the link, which opens many possibilities. Either to include the data of several modules into one stream or to include error checking encodings into the data to be able to judge only on the transmitted bits and bytes.

To be able to meet the requirements for a solid data transmission in faster machines as the LHC is and transferring more data in shorter time, the future optical links have to include higher speed components and operate at higher frequencies than the machine frequency. It is to be study in time if there are disturbing effects on the data taking and performance of the detector and accelerator machine.

All in all the present Pixel detector optical link is a good basis to develop transmission systems for future detectors and the commissioning and operation has given and will give a good reference for further developments.

**VI. Acknowledgements**

Our thanks is to the community who developed, produced, tested, installed and commissioned the Pixel detector. Many people contributed to the work which is described in short was in this paper. Without the help of a large group of people the successful start of operation of the detector and its optical data transmission system would not have been possible.

**VII. References**


Single-Event Upsets in Photodiodes for Multi-Gb/s Data Transmission

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Abstract

A Single-Event Upset study has been carried out on PIN photodiodes from a range of manufacturers. A total of 22 devices of eleven types from six vendors were exposed to a beam of 63 MeV protons. The angle of incidence of the proton beam was varied between normal and grazing incidence for three data-rates (1.5, 2.0 and 2.5 Gb/s).

We report on the cross-sections measured as well as on the detailed statistics of the interactions that we measured using novel functionalities in a custom-designed Bit Error Rate Tester. We have observed upsets lasting for multiple bit periods and have measured, over a large range of input optical power, a small fraction of errors in which an upset causes a transmitted zero to be detected as a one at the receiver.

I. INTRODUCTION

Single Event effects have been widely documented to occur in the photodiodes typically used in modern high-speed serial communications [1, and references therein]. At CERN, we are currently designing the next generation of optical data transmission link for reading-out and controlling particle physics detectors to be operated at CERN’s upgraded Large Hadron Collider (Super LHC). Such links will operate at multi-gigabit per second data-rates. The innermost regions of the detectors will encounter a radiation environment dominated by high-energy pions with a most-probable energy around 300 MeV, at fluxes of $10^9 \text{ – } 10^8 \text{ particles/cm}^2/\text{s}$, depending upon position with respect to the beam (see Figure 1).

![Figure 1: Extrapolation of expected fluxes for Inner Detectors from CMS data at 500 fb-1 (LHC) to 3000fb-1 (SLHC).](image)

The control information flowing into the detectors from shielded control rooms is critical for maintaining the synchronization of the data-taking system, both internally and with respect to the bunched beams circulating in the SLHC. It is therefore of critical importance that this control information be transmitted error-free and, with the knowledge that Single Event Upsets (SEUs) will occur within a photodiode placed in such an environment, the use of Forward Error Correction (FEC) coding will be mandatory. Validation of any choice of FEC code depends upon a detailed knowledge of the statistics of the errors that are expected to be encountered and the test reported in this paper aims to gather that knowledge.

In order to gather as much information as possible, we performed a small survey of the radiation-response of several different devices. InGaAs PIN photodiodes operating at 1310nm, GaAs PIN photodiodes operating at 850nm were combined in this test with Receiver Optical Sub-Assemblies (ROSA) where the Transimpedance Amplifier (TIA) is mounted in the same TO-can as the photodiode. Again, both 1310nm InGaAs and 850nm GaAs ROSAs were included.

II. SEU TEST METHOD

A. Irradiation test setup

The irradiation was carried out at the PIF-NEB proton irradiation facility at the Paul Scherrer Institut (PSI), Villigen, Switzerland [2] using a 63 MeV proton beam. Every second the flux was measured by ionization chambers and its value stored in a file by the control software of the irradiation facility for later analysis.

The DUTs were mounted on a rotating axle that allowed the angle of incidence of the proton beam on the optoelectronic receivers to be varied between normal (0°) and grazing incidence (90°) by remote control from outside the irradiation bunker. Measurements were taken at 0°, 10°, 80° and 90°.

Data were generated inside the FPGA-based Bit Error Rate Tester (BERT) described below, that was sited below the beamline inside the irradiation bunker, but shielded with a combination of Aluminium and Polyethylene. Serial data was passed on to a laser driver and laser diode for conversion to an optical signal (see Figure 2). This signal passed through 25 m of optical fibre to the control room, where an optical attenuator and power meter were used to control and measure the amplitude of the light returning, via an optical splitter and another 25 m of optical fibre cable, to the DUTs in the irradiation bunker.

The signals from the photodiodes require amplification in order to be sent over coaxial cables to the shielded Bit Error Rate Tester (BERT). Combined TIA/Limiting Amplifiers from Maxim Semiconductor (MAX3866) were mounted in very close proximity to the photodiodes on the test board. The electrical signals from the ROSAs were further amplified using a Limiting Amplifier (LA), also from Maxim Semiconductor (MAX3748B). The amplifiers were shielded from the pro-
ton beam by 6.5 mm of brass, sufficient to stop 60MeV protons. In addition, each set of eight DUTs was accompanied by two reference photodiodes and TIA/LAs that were also shielded. These references, one SM and one MM, were provided to measure any possible noise induced by external sources within the irradiation bunker.

![Illustration of the irradiation setup](image)

**Figure 2:** Setup for the proton irradiation test.

**B. FPGA-Based Bit Error Rate Tester**

A custom BERT was implemented (see Figure 3) based upon the Transceiver Signal Integrity Development board available from Altera for the Stratix II GX family of FPGAs, which include embedded high-speed transceivers capable of operating at data-rates up to 6.375 Gb/s [3].

The primary testing goal of measuring error statistics was achieved through the use of an error log memory that could hold up to 8K 20bit words. For every received word, the XOR of the transmitted and received data is evaluated and if one or more bit errors are encountered this error pattern is stored in the memory along with a timestamp for later analysis. In addition, basic Bit Error and Word Error counters were implemented.

A second memory of 8K 20bit words contained the pattern cyclically sent by the transmitter. In our case this memory was filled with random data, 8B/10B encoded offline for line-balancing and with commas inserted every 64 words to aid synchronization in the receiver. The received data were compared “as-is”, i.e. not decoded, to measure the raw BER due to SEU errors only and not errors due to decoding problems.

Firmware was developed that would allow operation at the three data rates used in the test (1.5, 2.0 and 2.5 Gb/s) by simply supplying a different frequency base clock to the FPGA.

Ten optoelectronics receivers were simultaneously tested on each irradiation board and all of the boards contained both SM and MM devices. Each FPGA supports a maximum of four full speed electrical transceivers, and therefore three FPGA platforms were required for our test. On each FPGA a maximum of one transmitter channel was active, because only one SM and one MM laser source were employed in our setup. Each FPGA board can work independently or can be connected with a second one in master-slave mode.

![Simplified diagram of the BERT implemented in firmware](image)

**Figure 3:** Simplified diagram of the BERT implemented in firmware.

**C. Devices tested**

Devices were selected based upon current availability from six vendors. One device type (Man. 4, Mod. 1) was included to provide a comparison with previous work carried out at CERN [4] at lower data-rates. Table 1 shows the devices tested and some relevant parameters.

The devices were arranged across three test boards that were exposed in succession to the proton beam.

<table>
<thead>
<tr>
<th>Family</th>
<th>Wave-length (nm)</th>
<th>Device Type (# tested)</th>
<th>Active diameter (µm)</th>
<th>Responsivity measured (µV/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN 1310</td>
<td>Man. 1, Mod. 1 (2)</td>
<td>30</td>
<td>0.7 A/W</td>
<td></td>
</tr>
<tr>
<td>PIN 1310</td>
<td>Man. 1, Mod. 2 (2)</td>
<td>60</td>
<td>0.8 A/W</td>
<td></td>
</tr>
<tr>
<td>PIN 1310</td>
<td>Man. 1, Mod. 3 (1)</td>
<td>60</td>
<td>0.75 A/W</td>
<td></td>
</tr>
<tr>
<td>PIN 1310</td>
<td>Man. 1, Mod. 4 (2)</td>
<td>80</td>
<td>0.8 A/W</td>
<td></td>
</tr>
<tr>
<td>PIN 1310</td>
<td>Man. 2, Mod. 1 (2)</td>
<td>60</td>
<td>0.8 A/W</td>
<td></td>
</tr>
<tr>
<td>PIN 1310</td>
<td>Man. 3, Mod. 1 (2)</td>
<td>—</td>
<td>0.75 A/W</td>
<td></td>
</tr>
<tr>
<td>PIN 1310</td>
<td>Man. 4, Mod. 1 (3)</td>
<td>80</td>
<td>0.8 A/W</td>
<td></td>
</tr>
<tr>
<td>PIN 850</td>
<td>Man. 5, Mod. 1 (3)</td>
<td>100</td>
<td>0.6 A/W</td>
<td></td>
</tr>
<tr>
<td>PIN 850</td>
<td>Man. 6, Mod. 1 (2)</td>
<td>90</td>
<td>0.5 A/W</td>
<td></td>
</tr>
<tr>
<td>PIN 850</td>
<td>Man. 6, Mod. 2 (2)</td>
<td>65</td>
<td>3.0 mV_W/µW</td>
<td></td>
</tr>
<tr>
<td>ROSA 1310</td>
<td>Man. 6, Mod. 3 (2)</td>
<td>90</td>
<td>2.2 mV_W/µW</td>
<td></td>
</tr>
</tbody>
</table>

*(Man: Manufacturer; Mod.: Model)*

**Table 1:** Devices Tested. 1310nm devices are Single-mode, 850nm devices are Multi-mode.

### III. RESULTS: OVERALL TRENDS

For every combination of the selected data rates and angles, attenuation scans monitoring the BER were systematically performed both with the beam on and off, to be able to distinguish in every case errors caused by protons from those due to electrical and environmental noise.

As an example, we show the effect that turning on the beam has on the BER performance of two devices in Figure 4. In this figure and throughout the paper, the Optical Modulation Amplitude (OMA) is measured at the input of the optoelectronic receivers. When the beam is on, the range of OMA can be divided in two regions, one where performance is dominated by noise and one where it is dominated by radiation in-
duced errors. The almost perfect matching in the noise dominated region between the plots with beam on and off shows the good reproducibility of the results.

In the following, most results will be presented in terms of the Bit Error Cross Section, defined as the quotient between the number of bit errors occurring during the testing time and the accumulated fluence. This cross section is only defined and presented in the SEU dominated region.

Plots similar to that of Figure 4, comparing the BER with beam off and on, were analysed for the reference photodiodes at all incidence angles. These have shown that the shielding was not working perfectly at all angles; specifically, some upsets could be observed in the reference photodiodes near grazing incidence.

**A. Device Families**

We compare the Bit Error Cross Section of every model used in our test under a common set of conditions, 2.5 Gb/s and grazing incidence (90°), in Figure 5. For a given value of OMA the difference in cross section among devices spans more than two orders of magnitude, but the plots for all models exhibit the same general shape. The variety of active diameters, packaging materials and manufacturing processes among devices from different manufacturers makes general trends difficult to observe.

Nevertheless, photodiode Model 1 from Manufacturer 1, which happens to have the smallest active diameter among all the devices tested (30 microns), stands out as remarkably better than the rest. Since the path of the protons through the active volume is minimised, so is the BER, especially the contribution due to direct ionization.

The ROSAs do not rank among the devices with worse performance (especially for the single mode case), even though in these devices we are observing the combined effects of SEUs in the photodiode and in the unshielded TIA (The LA is shielded).

**B. Angular dependence**

We confirm the observation made in previous tests by other authors [1] and our own team [4]: that the maximum of the cross section as a function of the incidence angle occurs near 90° (grazing incidence) and it is minimum for 0° (normal incidence), as shown in Figure 6. This is expected, as 90° corresponds to the longest ionizing path of the protons through the active volume of the photodiode.

We were expecting a very selective peak of the cross section around 90°, as shown for instance in [1] or [4]. However that is not exactly what we observe in Figure 6, where the plots corresponding to 0° and 10° should be closer to one another, and closer to that of 80°, to agree with this expectation. This deviation from the expected behaviour could be explained by partial shadowing of the DUTs by the optical fibres and connectors attached to them, which could degrade the energy of the beam for angles near normal incidence.
C. Data Rate dependence

For a given device and angle, when plotting the BER as a function of the received optical power for the three data rates measured, we observe that - within the limits of the experimental error - they superimpose almost perfectly, indicating that there is no dependence of the SEU induced BER on data rate (see Figure 7).

With this in mind, using the relationship below:

\[
\text{BER} = \frac{\sigma \times \text{flux}}{\text{data rate}}
\]

between BER, Bit Error Cross Section (\(\sigma\)), data rate and average flux, and taking into account the good stability of the proton beam used, we conclude that there is a linear dependence of the cross section with data rate, at least in the range from 1.5 to 2.5 Gb/s. This contrasts with results presented by other researchers [5], who have shown a linear relationship at low data rates, but a greater than linear dependence at the higher end of their measurement range (1.2 Gb/s).

IV. Results: Error Log Analysis

The error logging mechanism implemented in the custom FPGA BER Tester allow us to obtain a very detailed analysis of the error statistics: burst length histograms, Error Free Interval (EFI) histograms, pattern dependence, as well as correlation of errors with the transmitted pattern.

In order to characterise an error burst, not only is its length important, but also the value of the Error Free Threshold (EFT) used in the analysis [6][7], defined as the maximum number of successive correct bits allowed inside a burst. The value of the EFT must be carefully selected, examining simultaneously its effect both on the EFI histogram and on the burst histogram. We have selected an EFT of 10 bits, implying that any two bit-errors separated by 10 or less correct bits are considered part of the same burst and have obtained satisfactory results.

A. Error Classification

We have used the results from the error log analysis to classify the errors according to the following criteria:

- **Error length.** We distinguish between single (isolated) errors and burst errors. For reason that will become clear later, we further subdivide burst errors in short (length between 2 and 20 bits) and long bursts (length over 20 bits).
- **Fraction of 0-to-1 errors.** We can correlate the logged burst error patterns with the transmitted sequence to find out what fraction of the bit errors are due to sent 0’s being mistaken at the receiver by 1’s, and vice-versa.
- **Burst occupancy** (sometimes also termed burst density): is computed as the number of bits that were actually flipped in a burst divided by the length of that burst.

![Figure 7](image-url): Bit error cross section as a function of received optical power for three different devices at 2.5, 2.0 and 1.5 Gb/s; grazing incidence.

![Figure 8](image-url): Two-dimensional burst histogram for a 30 µm SM photodiode (Man.1 Mod.1) tested at 2.5 Gb/s and grazing incidence. EFT = 10 bits.

![Figure 9](image-url): Two-dimensional burst histogram for a SM ROSA (Man.6 Dev.2) tested at 2.5 Gb/s and grazing incidence. EFT = 10 bits.
gram, for which we show two examples in Figure 8 (for a photodiode) and Figure 9 (for a ROSA). A circle is represented at point \((x, y)\) if one or more bursts of length \(y\) bits are present in the 1D-burst histogram for a received power level of \(x\) (dBm). The size of the circle is logarithmically proportional to the BER contribution due to all bursts of length \(y\) at this power level. The colour of the circle gives information about the average 0-to-1 fraction (Figure 8) or burst occupancy (Figure 9), following the colour scale shown to the right of the figure. The upper part of each plot shows the dependence of the total BER on OMA for comparison to data shown previously.

Making a global classification of the errors required the careful examination of this kind of 2-D histogram for all devices and test conditions, but the two examples presented here are representative of the general behaviour of photodiodes and ROSAs, respectively.

We can classify the errors induced by SEU in three groups:

1. **Single errors**: this is by far the most frequent type of error. Independently of the device, data rate, angle or power level, the bin of length 1 dominates all burst length histograms. Almost all single errors are due to 0-to-1 bit flips. However, even for very low attenuation values, for which the probability of a noise-induced error is virtually zero, 1-to-0 bit flips still occur at the level of a few per cent (photodiodes) or a few per mille (ROSAs) as shown in Figures 10 & 11.

2. **Short bursts (2-20 bits)**: For this type of error the conclusions differ slightly between ROSAs and PINs:
   - For photodiodes there is a strong correlation between the optical power at the receiver input and the occurrence of this type of bursts: the lower the power, the higher the number of bursts, and also the more important their contribution to the total BER. With respect to the 0-to-1 fraction, similarly to what happened for single errors, it is very close to 1. Many of the photodiodes show an anomaly by which all short bursts have a high 0-to-1 fraction except bursts of length 2. This is for example the case for the SM device in Figure 8, for which most double errors are in fact pairs of 1's mistaken in the receiver as pairs of 0's.
   - For ROSAs, there is also a high correlation of the short bursts with the power level, but it is more irregular and, contrary to photodiodes, a few short bursts are still present for very high values of the received power. With respect to the 0-to-1 fraction, in the ROSAs it is higher than for photodiodes, almost exactly equal to 1. There is no anomaly affecting the 0-to-1 fraction for double errors.

   It is especially interesting that for both type of devices the occupancy of these bursts is close to 100% (for double errors it is exactly 100%). This is the first direct measurement of multiple-bit bursts in photodiodes reported in the literature.

   We have also observed, both for photodiodes and ROSAs, that the contribution of short bursts to the total BER is strongly correlated with angle: short bursts occur more often at 90° than at 80°, and more often at 80° than at 10°; they almost disappear when the angle approaches 0°.

3. **Long bursts (length > 20 bits)**, which are almost ex-

---

![Figure 10: Different contributions to the BER for a 30 µm SM photodiode tested at 2.5 Gb/s and grazing incidence.](image)

![Figure 11: Different contributions to the BER for a SM ROSA tested at 2.5 Gb/s and grazing incidence.](image)
clusively present in the ROSAs. The main characteristic of this type of error is that the burst occupancy is low, around 30-40%. The 0-to-1 fraction is very close to 1, as was also the case for single errors and short bursts in the ROSAs.

Long bursts are to some degree correlated with the received power level, as shown by the plot of their contribution to the total BER in Figure 11. However, a quick look at Figure 9 also reveals that long bursts can basically occur for any value of OMA.

We have also observed some dependence on angle: many fewer long bursts occur at 0° than at other angles.

In Figure 9 we see that the distribution of burst lengths is more or less continuous, without a gap between short and long bursts. Short bursts actually occur in ROSAs more frequently than long ones, but even so the contribution of the long ones to the total BER is much more important (Figure 11). This is because, despite their low occupancy, long bursts can last up to a few hundred bits. In contrast, bursts longer than 10 bits are virtually absent in photodiodes.

As for the reference devices, we almost exclusively observed single errors, and a few short bursts at very low power levels, induced by noise. The very few short bursts occurring at higher power levels can be explained by the fact that the shielding was not working perfectly for angles near grazing incidence, as mentioned in Section III.

B. Hypothesis for the origin of bursts

We hypothesise that the long bursts occurring in the ROSAs are due to upsets taking place in the TIA, rather than in the photodiode. The fact that long bursts are almost exclusively present in the ROSAs, where the TIA cannot be shielded, supports this hypothesis; on the other hand, the very few long bursts that appear on photodiodes could still share the same origin because the shielding was not completely effective.

Another fact that backs up this theory is that the median length of long bursts, when expressed in absolute time units (ns, rather than bit periods), turns out to be fairly independent of the data rate. It takes values around 50-60 ns. These events are very long compared to the speed of the TIA, so probably the errors are not due to hits in the signal path but to hits in other nodes of the circuit with much longer time constants.

In contrast, we favour the hypothesis that short bursts are indeed related to upsets in the photodiodes, since we observed a very marked dependence on the received power level and on the incidence angle, the occupancy of these bursts is quite high and the majority of the bit flips correspond to 0’s turning into 1’s.

V. Conclusions

Results of an ambitious SEU test with protons of a large selection of PIN photodiodes and ROSAs operating at high data rates have been presented. Tests at various incidence angles have confirmed that the highest error cross sections are obtained for angles near grazing incidence. The SEU induced BER turned out to be independent of the data rate in the measurement range, from 1.5 to 2.5 Gbps.

The use of a custom BER tester allowed us to obtain detailed statistics of the error events. For instance, isolated errors in which a transmitted 1 is detected as a 0 at the receiver have been observed at power levels where they cannot have been induced by electrical noise.

We have also shown that multiple bit errors can occur in optoelectronic receivers. Short error bursts spanning up to a dozen bits, were observed in the photodiodes and longer bursts, up to a few hundred bits in length, have been measured in the ROSAs. To the best of our knowledge, this kind of behaviour, where an SEU can upset several successive bits, has not been previously reported in SEU tests performed with photodiodes at other data rates. Short bursts could be originated by upsets in the photodiodes, but long bursts in the ROSAs are most probably related to proton hits in the un shielded TIA. In either case, burst errors will have to be mitigated using FEC coding in future optical links to be used inside Super LHC detector systems. The detailed statistics collected during this test will prove essential in the design and validation of an appropriate FEC scheme.

VI. Acknowledgments

The authors would like to thank Dr. Wojtek Hajdas for his help during irradiation at PSI. We would also like to acknowledge the fruitful discussions held with Dr. Federico Faccio, Dr. Paulo Moreira, Dr. Jorgen Christiansen, Dr. Philippe Farthouat, Dr. Alessandro Marchioro and Mr. Csaba Soos at CERN.

VII. References

Design and Radiation Assessment of Optoelectronic Transceiver Circuits for ITER

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Abstract

The presented work describes the design and characterization results of different electronic building blocks for a MGy gamma radiation tolerant optoelectronic transceiver aiming at ITER applications. The circuits are implemented using the 70GHz f\textsubscript{T} SiGe HBT in a 0.35µm BiCMOS technology. A VCSEL driver circuit has been designed and measured up to a TID of 1.6 MGy and up to a bit rate of 622Mbps. No significant degradation is seen in the eye opening of the output signal. On the receiver side, both a 1GHz, 3kΩ transimpedance and a 5GHz Cherry-Hooper amplifier with over 20dB voltage gain have been designed.

I. INTRODUCTION

One of the most challenging environments with respect to ionizing radiation current electronic designers are facing is ITER (International Thermonuclear Experimental Reactor). In this nuclear fusion reactor, the requirements of integrated electronic circuits with respect to radiation tolerance are very severe. One of the applications in ITER where the radiation conditions are extreme is the maintenance of the diverter. This periodic task will need to be performed by remotely operated robots and its functionality could be improved by adopting a significant amount of on-board electronics. Several systems and circuits will need to remain operational even after exposure to a TID (Total Ionizing Dose) in the order of MGy. The anticipated gamma radiation levels are similar to those expected in the S-LHC. The design of these circuits is clearly very challenging. This paper will focus on the potential use of a bidirectional fiber optic communication link between the robotics operated inside the reactor vessel and the control room. More specifically we will present and discuss our recent results on the design and assessment of the radiation hard optical transceiver electronics. All circuits are designed in a 0.35µm BiCMOS technology.

Fig. 1 shows the schematic of a typical fibre optic link including the analogue front-end circuitry for both the transmitter and the receiver side. In previous work we designed and assessed a discrete driver for a VCSEL [6] on the transmitter side of the link. Even though this driver was sufficiently tolerant to radiation, it featured several shortcomings owing to its discrete nature: the inherent frequency performance is limited due to large circuit board parasitics, the complete circuit is rather area consuming which may complicate the mounting of the transmitter and the poor matching performance between the devices in circuit blocks like a differential pair and a current mirror limits the predictability and hence, the reliability of the driver.

The following transmitter section describes the design, simulation and measurement of a new and integrated VCSEL driver in a 0.35 µm SiGe BiCMOS technology which no longer suffers previous shortcomings. The driver will operate at a power supply of 3.3 V and is intended to be used in combination with a 1550 nm VCSEL. The design is based on SPICE simulations using the model provided by the manufacturer but modified to include the dose dependent effects of gamma irradiation on the devices’ DC parameters. In the case of the driver, where only HBT’s are used, the model describes the influence of radiation on the base current of the SiGe HBT. Details on the model adaptations for this device are available in [12]. The model itself is based on a similar approach for a discrete SiGe HBT presented in [5].

On the receiver side several electronic building blocks have been designed in the same 0.35µm BiCMOS technology. The TIA (TransImpedance Amplifier) is the first block after the photodiode and converts the diode current into a voltage, sufficiently high above the noise floor of the subsequent PA (PostAmplifier). The TIA features a transimpedance gain of 3kΩ for a 1GHz bandwidth. The equivalent input noise current given by the integrated output noise voltage divided by the transimpedance gain is 0.6µA. The circuit was
designed taking transistor radiation effects into account. We included the previously measured degradation in the simulation via a DC SPICE model extension of the bipolar transistors. For the PA a sequence of differential bipolar Cherry-Hooper amplifiers was designed with a simulated bandwidth of 5GHz and a gain of 20dB per stage. These receiver circuits are currently being processed.

II. OPTICAL TRANSMITTER

For the transmitter side a driver was implemented for a long wavelength (1550 nm) VCSEL (Vertical Cavity Surface Emitting Laser). The schematic of the integrated VCSEL driver circuit is shown in Fig. 2 and is based on the discrete driver presented in [6]. The current through the VCSEL is composed of a constant DC current, to which we add a pulsed modulation current provided by the driver. A dummy resistor is placed symmetrically with respect to the VCSEL which improves the AC balance of the circuit since Q1a and Q1b now drive a similar load. Transistor Q2 acts as a current source which is biased by Q3 in diode configuration, hence creating a current mirror. Rci is an external potentiometer which allows to set the modulation current to the required level. This was done only once and no adjustment during irradiation is required. The supply is set at 3.3 V.

![Fig. 2: Schematic of the integrated SiGe VCSEL driver.](image)

The circuit was monitored before, during and after several Co60 gamma irradiation experiments up to a TID of 1.6 MGy. Fig. 3 shows the relative increase of the modulation current as a function of the accumulated dose. The modulation current displays a limited variation in the order of 0.1 % up to a dose of 600 kGy. The initial decrease is attributed to an increase in base current for the different transistors as evidenced by separate measurements on identical stand-alone transistors. For Q3 and Q2 the additional base current reduces the collector current for both transistors and hence decreases the modulation current through the driver.

The output current through the VCSEL is not only degraded by changes in the base current of Q2 and Q3. A fraction of the current is also lost in the base of Q1b. The initial decrease in modulation current is followed by an increase which is caused by the observed in-situ recovery of the devices during irradiation [12].

The design of the driver could principally be improved to render an even more stable output current, even during irradiation. The influence of the base current of Q2 and Q3 on the output current can be reduced by using an extra emitter follower Q4 in the current mirror to deliver the base current of both Q2 and Q3. This solution is depicted in Fig. 4. The influence of the base current changes of Q1a and Q1b could be counteracted by using a Darlington pair to substitute both transistors. The obvious downside of this solution is the effective doubling of the input transistors base-emitter voltage.

![Fig. 3: Modulation current through the VCSEL, measured as a function of the accumulated dose.](image)

The measurement data have been confirmed with SPICE simulations based on the model described in [12]. The same initial decrease and subsequent increase in modulation current is observed. Note that the minimum in the modulation current, occurring at a dose of 80 kGy does not correspond to the maximum in base current, just before the onset of recovery. This difference may be attributed to a difference in measurement conditions. For the separate devices the pins were grounded between two consecutive measurements during irradiation. This was not possible for the driver where the connections to the different contact switches are much more complex. Also the driver continuously draws a current of a few mA when it is being measured where the devices were measured for a large current range which makes the
average current lower.

Fig. 5: Eye diagram of modulation current through the VCSEL after a dose of 1.6 MGy at 622 Mbps.

A second irradiation experiment has been performed to verify the operation of the driver up to a TID of 1.6 MGy and up to a bitrate of 622 Mbps. The resulting eye diagram is shown in Fig. 5. A photograph of the integrated driver, within a ceramic DIL40 package is depicted in Fig. 6.

![Photograph of an integrated SiGe VCSEL driver.](image)

Fig. 6: Photograph of an integrated SiGe VCSEL driver.

**III. OPTICAL RECEIVER**

Two crucial building blocks in the design of the receiver (Fig. 1) will be discussed: a differential bipolar transimpedance amplifier and a differential bipolar Cherry-Hooper amplifier which is used to construct the postamplifier.

Fig. 7 shows a simplified schematic of the transimpedance amplifier. It consists of a common-base input stage, formed by Q₁ which decouples the input capacitance (including the diode capacitance and parasitic capacitance related to the connections to the IC) from the transimpedance feedback loop. This stage presents a current gain of almost 1. The second stage consists of a common-emitter stage formed by Q₂ with shunt-shunt feedback resistor Rₐ. The transimpedance gain of the circuit can be approximated by 2Rₑ. The bandwidth of the circuit is determined by the base node of Q₂. On this node, the resistance needs to be sufficiently high to keep the GBW (gain bandwidth) of the loop sufficiently below the output pole of the open loop system in order to guarantee the system stability:

\[
BW = \frac{1 + g_{m2}R_f}{2\pi C_{gs} \left( R_f \parallel R_i \right)}.
\]

Notice that both for achieving high gain and good stability the value of Rₐ will be chosen sufficiently high. The low frequency noise contributions referred to the input of the circuit are given by

\[
\overline{i_{n,\text{in}}}^2 = 2kT\Delta f \left( \frac{1}{R_e} + \frac{1}{R_i} + \frac{r_{bh}}{R_f} \right),
\]

where \( r_{bh} \) is the parasitic base resistance of Q₁. This expression shows the main drawback of adding a common base input stage as it reduces the noise performance by the first three terms in equation (2). Even though Rₑ can be chosen larger the overall noise performance will still be degraded.

![Bode diagram of the closed loop transimpedance gain of the circuit for total ionizing dose going from 0 to 300 kGy.](image)

Fig. 8: Bode diagram of the closed loop transimpedance gain of the circuit for total ionizing dose going from 0 to 300 kGy.
Fig. 8 shows the simulated transimpedance gain of the circuit as a function of frequency for TID values going from 0 to 300 kGy. The DC gain is seen to stay constant at 70 dBΩ, or roughly 3.2 kΩ. As the ionizing dose increases the bandwidth of the circuit reduces with about 6% from 1.05 GHz to 990 MHz. After 200 kGy it increases again. The main origin of this behavior lies in the reduction in current through Q2 by an increased base current drawn from the current mirrors as described earlier for the VCSEL driver.

![Fig. 8: Simulated transimpedance gain vs. frequency for TID values ranging from 0 to 300 kGy.](image)

Fig. 9: Rms integrated output noise voltage of the transimpedance amplifier for TID values from 0 Gy to 300 kGy. The rms integrated output noise voltage for increasing frequency is depicted in Fig. 9. The upper curve shows the curve before irradiation. As the total dose increases the integrated noise reduces mostly owing to the reduction in bandwidth described previously. The sensitivity of the circuit can be evaluated by dividing the total integrated output noise voltage by the transimpedance gain of the circuit. An input current sensitivity of about 2 µA is achieved for a SNR of 10 dB.

![Fig. 9: Rms integrated output noise voltage.](image)

A combined noise transient simulation was used to verify the behavior of the driver at different dose levels and for different currents. No significant degradation is observed in these simulations. An eye diagram of the output signal is shown in Fig. 10, where the input was a 1 Gbps 2^7-1 PRBS current of 30 µA.

![Fig. 10: Eye-diagram of the output voltage.](image)

Fig. 11 depicts the simplified schematic of a differential bipolar Cherry-Hooper stage proposed as building block for the post-amplifier in the receiver. The circuit shows many similarities with the transimpedance amplifier discussed previously. The construction of a Cherry-Hooper amplifier is based on a transconductance stage followed by a transimpedance stage. The reduced input impedance of the transimpedance amplifier ensures a high circuit bandwidth albeit with a moderate amplifier gain. In the presented circuit the transconductance stage is formed by Q1 in common-emitter configuration and is followed by Q2, also in common-emitter configuration and with negative shunt-shunt feedback provided by emitter-follower Q3 and Rf. The sensed feedback voltage is divided from the output voltage in order to reduce the loop gain. This in turn increases the overall closed loop gain of the entire circuit:

\[ A_v = \frac{g_{m1} R_f}{2 \pi C_{b2} R_f} \left( 1 + \frac{R_1}{R_2} \right) \]

The bandwidth of the circuit is mostly determined by the pole at the base node of Q2 and can be approximated by

\[ BW = \frac{1 + g_{m1} R_2}{2 \pi C_{b2} R_f} \]

This equation reveals the drawback of adding the resistive divider as R2 must be chosen smaller since part of the DC voltage drop is now taken by Rf. Basically this technique allows to trade gain for bandwidth and vice versa.
Fig. 12: Bode diagram of the closed loop voltage gain of the Cherry-Hooper circuit for total ionizing dose going from 0 to 300 kGy.

Fig. 12 shows the voltage gain of the amplifier stage as a function of frequency for total ionizing dose levels from 0 Gy up to 300 kGy. With respect to the bandwidth of the circuit, the same behavior is observed as described for the transimpedance amplifier, i.e. an initial reduction followed by recovery owing to a reduced current through the amplifying device. In this circuit however also a minor gain degradation is observed owing to the dependence of the gain on $g_{ml}$ and hence on the current through $Q_1$ which is degraded in the same manner as $Q_2$. The gain remains between 21.5 dB and 22 dB and the bandwidth stays larger than 5 GHz inspite of radiation.

A noise transient analysis was performed on the cascade of the transimpedance and Cherry-Hooper amplifier and a typical result is shown in Fig. 13. The same input current of 30 µA was used as for the TIA alone. Notice by comparison with Fig. 10 that the SNR of the signal is almost not degraded by the post-amplifier owing to the large gain of the TIA. Results with increasing dose levels are similar.

IV. CONCLUSION

We have presented recent design and characterization results on the most critical electronic building blocks in a MGy radiation tolerant optoelectronic transceiver for application in ITER. All circuits were designed in a 0.35µm SiGe BiCMOS technology using only the npn HBT devices. Simulations were performed using the model provided by the manufacturer but adapted to include their radiation dependent current gain degradation.

At the transmitter side, a VCSEL driver has been designed, simulated and measured before, during and after irradiation up to 1.6 MGy. No significant degradation is seen up to these dose levels and for a bitrate up to 622 Mbps.

At the receiver side a fully differential transimpedance amplifier has been designed and simulated. The circuit features a gain of 3.2 kΩ, a bandwidth of 1 GHz and an input current sensitivity of 2 µA at an SNR of 10 dB. The TIA is followed by a Cherry-Hooper based differential amplifier with a voltage gain of more than 21 dB and a bandwidth surpassing 5 GHz. Both circuits feature a degradation of only a few percent for a gamma dose up to 600 kGy.

V. REFERENCES


Wednesday 17 September 2008

Plenary Session 5
**COMMISSIONING OF THE LARGE HADRON COLLIDER**

Emmanuel Tsesmelis & Thijs Wijnands
CERN

Topical Workshop on Electronics in Particle Physics
17 September 2008

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**INTRODUCTION**

- Why a circular machine?
- Why protons?
- Why a superconducting machine?

---

**Acceleration**

Acceleration of a particle by an electrical potential

\[ \Delta E = \int \mathbf{F} \cdot d\mathbf{s} = \int q \mathbf{E} \cdot d\mathbf{s} = q U \]

Energy gain given by the potential:

\[ U = \int \mathbf{E} \cdot d\mathbf{s} \]

For an acceleration to 7 TeV a voltage of 7 TV is required.

---

**Energy loss for charged particles by synchrotron radiation**

\[ P_s = \frac{e_0 \cdot \epsilon_0 \cdot m_0 \cdot c^2 \cdot E^4}{4 \pi \cdot \rho^2} \]

with \( E = \) energy, \( m_0 = \) rest mass, \( q_0 = \) charge, and \( \rho = \) radius.

---

**Energy loss for electrons in LEP vs. protons in LHC**

- **LEP:**
  - \( E_{lep} = 100 \text{GeV} \)
  - \( U_{lep} = 3.844 \times 10^9 \text{eV} \)
  - Total power of synchrotron radiation:
    - Number of electrons in LEP: \( N_{lep} = 10^{12} \)
    - Total power of synchrotron radiation:
      - \( P_{total,lep} = N_{lep} \cdot \frac{E_{lep}^4}{\rho^2} \)
      - \( P_{total,lep} = 1.27 \times 10^7 \text{W} \)
  - Energy loss for one particle per turn:
    - \( U_{lep} = 8.121 \times 10^3 \text{eV} \)

- **LHC:**
  - \( E_{lhc} = 70000 \text{GeV} \)
  - \( U_{lhc} = 8.121 \times 10^3 \text{eV} \)
  - Total power of synchrotron radiation:
    - Number of protons in LHC: \( N_{lhc} = 10^{14} \)
    - Total power of synchrotron radiation:
      - \( P_{total,lhc} = N_{lhc} \cdot \frac{E_{lhc}^4}{\rho^2} \)
      - \( P_{total,lhc} = 2.699 \times 10^3 \text{W} \)

The power of the synchrotron radiation emitted at the LHC is very small, but the radiation goes into the superconducting magnets at 1.9 K...20 K.

---

**To get to 7 TeV: Synchrotron — circular accelerator and many passages in RF cavities**

- Maximum technically possible: ~20 MV per meter
- RF system LHC: 16 MV per meter

---

**Commissioning the LHC Accelerator and its Physics Programme**

Emmanuel Tsesmelis & Thijs Wijnands, CERN, Geneva, Switzerland
emmanuel.tsesmelis@cern.ch thijs.wijnands@cern.ch
The particles are trapped in the RF voltage; this gives the bunch structure.

The force on a charged particle is proportional to the charge, the electric field, and the vector product of velocity and magnetic field:

\[ F = q \left( \mathbf{E} + \mathbf{v} \times \mathbf{B} \right) \]

- Maximum momentum 7000 GeV/c
- Radius 2805 m fixed by LEP tunnel
- Magnetic field required \( B = 8.33 \) Tesla
- Iron magnets limited to 2 Tesla, therefore superconducting magnets are required
- Deflecting magnetic fields for two beams in opposite directions

The LHC is a two-ring superconducting proton-proton collider made of eight 3.3 km long arcs separated by 528 m Long Straight Sections.

While the arcs are nearly identical, the straight sections are very different.
There are 8 sectors:
- Utilities and machine technical systems are sectorised
- Assembly and commissioning almost independent
- Each system and utility tested and qualified independently prior the Sector Test
- Leak and pressure test
- Preparation for cool-down (flushing, filling, repairs...)
- ELQA at warm
- Cool-down and ELQA at cold
- Power test / power converters connected to the magnets for the first time and tested up to the nominal current

The objective is to validate:
1. the warm elements of the circuits
   - the power converters,
   - the energy converter system,
   - the powering interfaces,
   - the normal conducting cables
2. the utilities
   - demineralised water for cooling,
   - ventilation,
   - AC current supply and cables

LHC Sector 78 – First cooldown
- From 30K to 80K precooling with LN₂. 1200 tons of LN₂ (64 trucks of 20 tons). Three weeks for first sector.
- From 80K to 4.5K. Cooldown with refrigerator. Three weeks for the first sector. 4700 tons of material to be cooled.
- From 4.5K to 1.9K. Cold compressors at 15 mbar. Four days for the first sector.

Radiofrequency Cavities
400 MHz system:
16 sc cavities (copper sputtered with niobium) for 16 MV/beam were built and assembled in four modules.
Synchronization of the LHC's clockwise beam transfer system and the rest of CERN's accelerator chain achieved.

- Single bunch of a few particles was taken down the transfer line from the SPS accelerator to the LHC through the TI8 transfer line.
- After a period of optimization, one bunch was kicked from the transfer line into the LHC beam pipe and steered about 3 kms around the LHC itself on the first attempt.
- On Saturday, the test was repeated several times to optimize the transfer before the operations group handed the machine back for hardware commissioning to resume on Sunday.
Synchronisation of LHC Counter-Clockwise Beam (IP8)

- 22-23-24 August 2008:
  Synchronisation of the LHC’s counter-clockwise beam transfer system and the rest of CERN’s accelerator chain achieved.
  - The second test of the LHC beam synchronisation system tests allowed the LHC operations team to inject the first beam into the LHC through TIB.
  - Friday evening of 22 August, a single bunch of a few particles travelled down the transfer line from the SPS to the LHC.
  - After a period of optimization, one bunch was kicked from the transfer line into the LHC beam pipe and steered counter-clockwise about 3 km around the LHC.
  - Also again beam to point 3 to check optics

Injected Beam to LHCb

- LHCb events with beam on TED!
- BPTX 5L ~ 2 x 10^9 protons
- BPM 5L CMS Calorimeter andMuon System Recording Beam Dump on TCT in 5L

Measured Particle Density in ALICE Pixel Detector

- T2 Injection test Sunday August 24th 2008, Beam through ALICE all sheets from 15:02:17 first shot through ALICE to 15:09:40
- Measured with T2-BERT-2012-INV_BNL_EXTR1

3rd Synchronisation Test 6-7 September 2008

- BPTX 5L ~ 2 x 10^9 protons
- BPM 5L

3rd Synchronisation Test

- CMS Calorimeter and Muon System Recording Beam Dump on TCT in SL
10 September 2008

- 10:26 hrs Beam 1 (clock-wise beam)
- First & second turn only
- Beam 1 simultaneously detected by all 4 experiments

First Circulating Beam

ALICE Pixel Detector

September 11:
- Access to 4 points whole day
- Cycle and set machine
- Roll back to settings from Wednesday 10/9
- Beam 2 inject and dump after 10 ms
- Established 10 min circulating beam

September 12:
- Same things for beam 1
- Matrix response measurements for orbits (H/V & B1/2)
- 23:30 Transformer point 8 broken. Short on coil. Need replacement
- Cryogenics reacting to try to keep helium.

September 13-14:
- Access 8 6 4 and experiments
- TS/EL looking for a transformer, found and repaired
- Cryo lost in 45 and 56
- Vacuum problem RB and L1

September 15:
- Hardware commissioning consolidation
- Access as required
Collisions

ATLAS sees 11 22 33 44
CMS sees 3 3 4 4
ALICE sees 1 1 2 2
LHCb sees nothing
(DDELPHI 12 3 4 1)

Parasitic collisions in 2 and 8

Beam - gas
Both beams

3 on 3 normal, 1 on 1 displaced 75ns

ATLAS sees 11 22 33 44
CMS sees 3 3 4 4
ALICE sees 1 1 2 2
LHCb sees 12
(2 2 at ± 11.25m)

LHCb sees nothing

Parasitic collisions in 2 and 8

Beam - gas
Both beams

2 on 2, with 1 bunch displaced 75ns

ATLAS sees 11
CMS sees 31 (and 2 2 at ± 11.25m)
ALICE sees 21
LHCb sees 12

Parasitic collisions in 1 and 5

Beam - gas
Both beams

2 on 2, clean collisions everywhere

4 \times 10^{10} \text{ per bunch}
400 \text{ GeV} 11m
\sim 10^{27} \text{ cm}^{-2} \text{ s}^{-1}

ATLAS sees 11
CMS sees 31
ALICE sees 21
LHCb sees 12

Beam - gas
Both beams

First collisions (450 GeV)

- LHC performance committee
  - Rate of few 100Hz good for starters
  - Luminosity ~ 10^9 cm^{-2} s^{-1}
  - Few hours of collisions (couple of night shifts)
  - 2x2 without parasitic collisions is the preferred scheme
  - Prefer beam-gas over parasitic collisions
  - Prefer both beams giving beam-gas, rather than a single beam
  - Solenoids and toroids should be ON, dipoles OFF
  - ALICE would like one run with solenoid OFF

- Machine
  - Need bunch to bucket synchronization working
  - Need 450 GeV machine under control
  - Orbit, dispersion, tune, chromaticity, coupling
  - Then bring solenoids on
  - Need separation bumps on?
  - Need 10^8 per bunch to hit 10^9

Complementary scheme 1 on 3 if needed
**2008**

- Energy of the 2008 run: Agreed to be 10 TeV. The machine considers this to be a safe setting to optimize up-time of the machine until the winter shut-down (likely starting around end of November). Therefore, simulations can now start at 10 TeV.
- Why only 10 TeV? To avoid the need to train the dipoles to 7 TeV.
- The winter shut-down will then be used to commissioning and train the magnets up to full current, such that the 2009 run will start at the full 14 TeV design energy.

**Beyond Initial Run**

**2008**

- Stage A
- 5 TeV operation
- 43 bunches operation
- 25ns ops
- Commissioning
- Hardware commissioning
- Machine checkout
- No beam
- Beam

**2009**

- Stage A
- 5 TeV operation
- 25ns ops
- Commissioning
- Hardware commissioning
- Machine checkout
- No beam
- Beam

**Summary and Conclusions**

- On 10 September 2008, Beam-1 and Beam-2 were successfully steered around the 27-km LHC ring for the first time.
  - “It’s a fantastic moment,” said LHC project leader Lyn Evans. “It now opens up new ways of understanding about the origins and evolution of the universe.”
  - “The LHC is a discovery machine,” said CERN Director General Robert Aymar, “its research programme has the potential to change our view of the Universe profoundly, continuing a tradition of human curiosity that’s as old as mankind itself.”
  - The LHC is the most powerful instrument ever built to investigate properties of particles and the physics results from the LHC will determine the future course of high energy physics.
  - …but…LHC does not start up easily, a big amount of work still ahead of us!

**Stage A physics running for ALICE and LHCb**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Basin levels</th>
<th>Rates in 2</th>
<th>Rates in 3</th>
<th>Rates in 6</th>
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<td></td>
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<tr>
<td>IP 3 &amp; 63 &amp; 156 &amp; 36 &amp; 1.7 &amp; 0.1</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

All values for nominal emittance, 10 m $\beta\gamma$ point 2.

**43 bunch filling scheme**

Easiest to displace a 3 or 4 bunches operated by LHCb

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Rates in 2</th>
<th>Rates in 3</th>
<th>Rates in 6</th>
</tr>
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<td></td>
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</tbody>
</table>

LHCb 444 344 244

**Proton Commissioning Strategy**

<table>
<thead>
<tr>
<th>Stage A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware commissioning</td>
<td>Machine checkout</td>
<td>Beam commissioning</td>
<td>No beam</td>
</tr>
</tbody>
</table>

- Pilot physics run
  - 43 bunches, no crossing angle, no squeeze, moderate intensities.
  - Push performance
  - Performance limit: 10$^{32}$ cm$^{-2}$ s$^{-1}$ (event pileup)

- 75ns operation
  - Establish multi-bunch operation, moderate intensities
  - Relax machine parameters (squeeze and crossing angle)
  - Push squeeze
  - Performance limit: 10$^{33}$ cm$^{-2}$ s$^{-1}$ (event pileup)

- 25ns operation
  - Nominal crossing angle
  - Push squeeze
  - Increase intensity to 50% nominal
  - Performance limit: 2$\times$ 10$^{33}$ cm$^{-2}$ s$^{-1}$

- Push towards nominal performance

- Easy to displace 3 or 4 bunches operated by LHCb

- 444 344 244
Abstract

There is no question that 3D integrated circuit design will play an important role in the continuing development of high performance integrated circuits. This paper will provide a brief introduction to the markets for 3D integrated circuits and the technologies that are used, followed by a review of 3D activities in High Energy Physics (HEP). The paper will review the first 3D chip for HEP and conclude with discussion of a collaborative effort to use a commercial vendor to fabricate 3D ICs as a path forward to meet the next challenge for electronics designers in HEP.

I. OVERVIEW OF 3D/VERTICAL INTEGRATION

A. Introduction

The just released Handbook of 3D Integration defines 3D integration as “the integration of thinned and bonded silicon integrated circuits with vertical interconnects between IC layers”. [1] This book is an excellent reference for those wanting to understand the fabrication principles for 3D as well as the approaches various organizations are taking to develop vertical integration.

Vertical integration is now in a position to allow significant improvements to those drivers that are critical to the semiconductor industry. More specifically, in the right application, 3D can provide 1) better electrical performance, 2) lower power consumption, 3) higher functionality, 4) improved form factor, 5) mixed technologies, and 6) lower cost.

B. Industrial Markets for 3D

There are a number of markets that are studying 3D. All major memory manufactures are working on 3D memory stacks. Significant cost reduction can be expected for large memory devices. The memory cost can be considerably less than going to a deeper technology node.

Pixel arrays with sensors and readout are well suited to 3D integration since signal processing can be placed close to the sensor. Current 2D approaches cannot handle the data rate needed for high speed imaging applications.

3D IC Pixel Electronics-
the Next Challenge

R. Yarema
On behalf of the Fermilab Pixel Design Group
D. Christian, M. Demarteau, G. Deptuch, J. Hoff, R. Lipton, A. Shenai, M. Trimpl, T. Zimmerman

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Microprocessors represent another market. A major bottleneck is access time between the memory and CPU. Memory caches are used as an interface but they require a significant amount of expensive chip real estate. Initial applications for 3D will use Logic to Logic stacking and Logic to Memory stacking.

Finally, in 2D FPGAs, wire delays are an inherent problem. 3D integration can improve the performance by moving the programmable interconnect circuitry from the logic block layer and placing it on a separate tier.

C. HEP Applications for 3D

The industrial markets are large and there is little HEP can do to influence the paths that they take toward vertical integration. However, there are already two areas where HEP can stand to benefit from the current state of the art.

The first is in the area of 3D pixel arrays. There are already descriptions of working 3D circuits with a sensor layer and two layers of electronics [2], [3]. In addition, Fermilab has already built a circuit with 3 layers of electronics where the total thickness of the electronics portion is only 22 microns [4]. The Fermilab circuit was designed as a demonstrator for the International Linear Collider (ILC). This circuit will be discussed in more detail later on.

The other area of interest for HEP is 3D bonding technology as a replacement for bump bonds in hybrid circuits. Fermilab worked with RTI International to develop CuSn eutectic bonding with small interconnect pillars for fine pitch bonding [5]. Initial tests showed the CuSn bonds to be stronger than conventional PbSn solder connections. Figure 1 show these pillars on a 50 micron pitch and a cross section of one of the connections.

Figure 1: (l) 7 micron diameter pillars on 50 micron pitch, (r) cross section of solder connection showing height of connection.

If post processing such as thinning a part after bonding is required, the percentage of bonded surface area needed to hold the parts together can be significant. Because of the 10
micron bond thickness, the bonded area may represent too much mass for some applications.

Another option of interest is the Direct Bond Interconnect (DBI) developed by Ziptronix. Minimal mass is required for bonding with the DBI process. Bond pitches as small as 3 microns have been demonstrated. Figure 2 shows 25 pixel sensors bonded to a Fermilab BTEV pixel ROIC wafer using DBI. After the chip to wafer bonding, the sensors were thinned to 100 microns. Due to the large surface bonding area associated with the DBI process there was no damage to the sensors during the thinning process.

Figure 2: Sensors bonded to ROIC using DBI process

A third option, called CuCu bonding, which also provides a low mass interconnect, is being pursued by Fermilab. A CuCu bond uses a very thin copper bond pad on each surface. If post processing such as thinning is needed, a relatively large part of the surface area will need to be bonded just like a CuSn bond. The advantage to CuCu bonds is that the thickness of the bond material is so small that it does not add significantly to the mass of the circuit. This process is used by Tezzaron and it will be described later in this paper.

II. BASIC PRINCIPLES FOR 3D

There are four key technologies needed for 3D integration, 1) via formation, 2) bonding, 3) precision alignment, and 4) thinning.

There are two main approaches to via fabrication. One is called “via first” and the other is called “via last”. In the “via first” process, the vias are an integral part of the wafer fabrication process. Thus the vias are imbedded in the wafer at the foundry. The vias can be fabricated either before or after the transistors are formed.

In the “via last” process, the vias are added to the wafers after the front end of line (FEOL) and back end of line processing (BEOL) has been completed. These vias are often added by a third party vendor.

The trend for low cost vias seems to be moving toward the “via first” process. Later in this paper there are examples of the “via first” and the “via last” processes.

The via formation processes are different in SOI CMOS and bulk CMOS processes. In CMOS the Bosch process is usually used to form vias. These vias need to be passivated before filling with metal to avoid shorts between all the vias. In the SOI process, a different etch process must be used to form the via but no passivation is needed before filling since the vias are already in an insulator.

There are five bonding options that are commonly used for 3D fabrication. These are all shown in figure 3. One bonding approach uses a polymer adhesive (typically BCB) to form a uniform bond over the entire surface. A second approach uses an oxide bond where an oxide covers most of the surface area to be bonded. The oxide surfaces are specially prepared and brought together to form an exceptionally strong silicon dioxide to silicon dioxide bond. With both the adhesive bond and the oxide bond, vias are formed after bonding to form the electrical connections between the parts being bonded. CuSn eutectic bonds are formed by placing copper on two mating surfaces and then placing a small amount of tin on the copper on one of the surfaces. The surfaces are then brought together and heated to form a high temperature eutectic bond. Typically the copper is 5 microns thick on each surface. With CuCu thermo compression bonds, thin copper pads are placed on each surface (normally the pads are a fraction of a micron thick). After careful cleaning, the surface are mated and heated to form the bond. The final option, called DBI, is a combination of two ideas. Oxide surfaces are prepared with small imbedded metal contacts that have high thermal coefficient of expansion. When the surfaces are brought together an oxide bond is immediately formed. After some time, the assembly is heated and the high expansion metal forms a compression bond. With the CuSn eutectic bond, the Cu thermo compression bond, and the DBI processes, both the mechanical and electrical connections are formed at the same time. Fermilab has been working with different vendors on options b, c, d, and e shown in figure 3.

Figure 3 – bonding options

Currently wafer to wafer 3 sigma bonding alignment is better than 1 micron. Typically vias have an aspect ratio of about 8 to 1. Therefore it is important to thin the wafers as much as possible in order to reduce the area needed for vias. Figure 4 shows a very thin wafer.

Figure 3: 6 inch wafer thinned to 6 microns and mounted to 3 mil kapton (MIT LL)

III. ACTIVITY IN HEP

Fermilab submitted the first 3D integrated circuit for HEP to MIT Lincoln Labs in October of 2006. In November of 2007 there was a meeting sponsored by CNRS/IN2P3 in
France called the 3D Integration Technologies Perspectives. Closely following this meeting there was another workshop in April 2008 sponsored by the Max Planck Institute called Vertical Integration Technologies for HEP and Imaging sensors. As a result of these activities new programs are developing. In Italy, the Ministry of Research has funded a 2 year program on 2D MAPS and Vertically Integrated Sensors that will focus on device and technology investigations rather than specific experiments. Another Italian effort is the INFN proposal for Pixel Systems for Thin Charged Particle Trackers Based on Vertical Integration Technologies. This 3 year program will focus on experiments like Super B and the ILC. After the meeting in France funding was approved for several French labs to develop vertically integrated circuits. Applications for the ILC, SHLC and imaging are expected.

At Fermilab a second 3D chip will be submitted to MIT LL in October 2008. In addition, Fermilab is forming an international 3D HEP collaboration for a multi project wafer run to develop vertically integrated circuits through Tezzaron. The run will have two stacked circuits with a deep N-well option. Up to 10 fully integrated 3D wafers will be fabricated in a 130 nm process. Submission is targeted for early 2009. Thus it is clear that interest for 3D has grown within the HEP community.

A. Description of first 3D Circuit for HEP

The first 3D chip designed for HEP was called the VIP1 (Vertically Integrated Pixel). It was a demonstrator chip for the ILC vertex detector. The chip was designed in the MIT Lincoln Labs 0.18 micron SOI process and had three tiers of stacked electronics. Details of the VIP1 circuit design were presented at the 12th LHC electronics workshop [6] and are not repeated here. The chip included all the major features needed for a vertex detector chip:

- Readout between ILC bunch trains
- High speed data sparsification
- Analog outputs from each pixel for improved resolution
- High resolution digital and analog time stamping
- Test input for every pixel
- 20 micron pixels in a 4096 pixel array.

A block diagram of the chip is shown in figure 5.

Most time stamping circuits designed to date for the ILC vertex detector are limited to 6-20 time stamps per msec. The digital time stamp in VIP1 uses a 5 bit Gray code counter that provides 32 time stamps/msec and it is easily expandable. Figure 6 shows both the digital and analog time stamp circuits. The digital time stamp circuit has a slow counter on the perimeter which counts up during the 1 msec bunch train. When a hit occurs, the current state of the counter is latched in the hit pixel for read out at a later time. The analog time stamp has a slow ramp generator on the perimeter that rises 1 volt during the beam train. When a hit occurs, the analog value of the ramp is latched in the pixel for read out. The digital and analog time stamps can be setup so that the digital time stamp provides a coarse 5 bit time stamp and the analog time stamp provides additional bits for higher resolution.

Figure 6 shows both the digital and analog time stamp circuits. The digital time stamp circuit has a slow counter on the perimeter which counts up during the 1 msec bunch train. When a hit occurs, the current state of the counter is latched in the hit pixel for read out at a later time. The analog time stamp has a slow ramp generator on the perimeter that rises 1 volt during the beam train. When a hit occurs, the analog value of the ramp is latched in the pixel for read out. The digital and analog time stamps can be setup so that the digital time stamp provides a coarse 5 bit time stamp and the analog time stamp provides additional bits for higher resolution.

Figure 7 shows a single cell block diagram of the VIP1 and figure 8 shows how the pixel is mapped into a 3D structure. There are 3 main parts: the analog front end with a test input and double correlated sampling, a pixel sparsification section with hit look ahead capability, and the time stamp section.

The MIT LL process used to build the VIP chip is a “via last” process wherein the vias are added after wafer fabrication and wafer to wafer oxide bonding is completed. The total height of the electronics in the 3 wafer stack is only 22 microns as shown in figure 8.
B. Test results of first 3D chip [8]

The basic functionality of the VIP1 has been demonstrated through the following series of tests.

- Full sparsified data readout
- Successful operation of the token passing scheme
- Operation of the digital and analog time stamp circuits
- Threshold scan
- Input test charge scan
- Fixed pattern and temporal noise measurements

At the present time, no problems have been found related to the 3D interconnects. On the other hand, the chip performance was severely compromised by poor transistor models and low yield. It should be pointed out that the same readout architecture has been demonstrated in a 2D MAPS device fabricated in the ST 130 nm process [7].

Figure 9 shows hits pixels in the full 64 x 64 array as a function of threshold. The readout is done using the sparsified data readout scheme.

Pixel to pixel threshold dispersion is shown in figure 10. The plots were taken by setting the common pixel threshold at increasing levels (no charge injection) and reading out all pixels over threshold using the data sparsification scheme.

The left hand plot in figure 10 was made with the integrator reset and shows threshold dispersion with a sigma of 25 e. The right hand plot was made with the integrator released and with the discriminator auto zeroed and shows a dispersion of 75 e. The increase in dispersion is thought to be due to internal coupling problems.

Another test was performed injecting a test charge into 119 pixels to simulate a hit pixel pattern. The left hand side of figure 11 shows the preselected hit pattern. The right hand side shows the pixel pattern read out using the standard data full sparsification scan. Although the results are not ideal, they demonstrate successful operation of the test inputs.

The analog signal response from the pixels in the 119 pixel test pattern was shown to be reasonably linear as seen in figure 12. As the level of the test charge through the test capacitor (0.2F) was increased more pixels exceeded the threshold up to 119. The plot shows the mean analog signal level of those pixels exceeding the threshold voltage. The superimposed line is an indication of the linearity. There is no signal at low input voltages due to the small size of the injection capacitor.

The digital time stamp circuit was shown to work but had a significant dependence on the power supply voltage. In a test, the 119 pixel hit pattern was injected at different times and the time stamp was read out. At a supply voltage of 1.4 V, the time stamp was correct for 118 of the 119 pixels. The analog time stamp, while working, gave poor results due to high leakage current in the sample and hold circuit.

A new improved version of the chip is being prepared for submission. The goal of the new submission is for improved yield and performance at the expense of a larger pixel size.
IV. A PATH TO THE FUTURE

Development of 3D integrated circuits is a challenge for a number of reasons. Depending on the approach taken, the cost can be high. Because most 3D processing is done at the wafer level, access to full wafers is needed. Finally the choice of vendors for small customers is very limited at this time. Fortunately Fermilab has found a vendor, Tezzaron, willing to do a multi project 3D wafer run. The run cost is reasonable.

As a leader in 3D technology, Tezzaron has built 3D devices for imaging, memory stacking, FPGAs, and microprocessors. Currently Tezzaron is gearing up to produce 10,000 3D wafers/month in 18 months. The 3D chips will include 2, 3, and 5 layer stacks of memories from 512Mb to 4 Gb. The wafers will be fabricated by Chartered in Singapore where the 3D assembly is completed by Tezzaron. The Tezzaron 3D assembly process is expected to be in 1 to 3 more foundries by the end of the year. The advantages of using Tezzaron include: existing rules for vias and bonding contacts, low cost, reasonable turnaround, one-stop shopping for wafer fabrication, via formation, thinning, and bonding. Fermilab has organized a collaboration of 6 French labs and 6 Italian labs to contribute to a MPW run at Tezzaron.

Chartered is one of the world’s top semiconductor foundries with an extensive line of CMOS and SOI processes down to 45 nm. Tezzaron has chosen the 130 nm CMOS process for 3D integration. Chartered has fabricated nearly 1 million 8 inch wafers in the 130 nm process and data demonstrates consistent high yield. Chartered is working to extend through silicon via (TSV) processes to 300 mm wafers and 45 nm technology. There is a full set of commercial tools to support the 130 nm process. The 130 nm process is well suited to analog circuit design offering deep N-wells, MiM capacitors, and multiple threshold voltage transistors.

The Tezzaron 3D process is a “via first process where TSV’s (super contacts) are formed after FEOL processing as shown in figure 13. The vias are only 6 microns deep. Figure 14 (l) shows the bonding of two identical wafers using a Cu-Cu bond in a face to face configuration. Figure 14 (r) shows the top wafer thinned to 12 microns to expose the vias and metallization added for bump bonds or wire bonds.

The Fermilab 3D MPW run will use a face to face bond as shown in Figure 14 to form a two wafer stack. To reduce mask costs, a single set of masks will include both the top and bottom circuits. For devices that do not have an integrated sensor, bond pads will be added to the top wafer for bonding to sensors at a later time using the Ziptronix DBI process.

The 3D collaboration expects to make a MPW submission in the first part of 2009. Submissions from Italy, France, and Fermilab will include projects for the ILC, SLHC and Super B. The cost of fabricating 25 eight inch wafers in the 130nm process and complete 3D assembly should be under $300 K.

V. CONCLUSION

New technologies have always presented challenges to HEP. Success with new technologies in HEP has often led to dramatic advances. Industry is making rapid progress in developing 3D integrated circuits. HEP is beginning to respond with new initiatives to explore this technology. Fermilab has been working with different 3D technologies for over 2 years and has now begun a collaboration with 12 international laboratories in France and Italy to use the Tezzaron 3D process to develop circuits for ILC, SLHC, and related applications. We believe that the collaboration will provide an excellent path forward for development of 3D integrated circuits to help HEP meet the 3D challenge.

VI. REFERENCES


Mobile Test Bench for the LHC
Cryogenic Instrumentation Crate Commissioning

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Abstract

The Large Hadron Collider (LHC) at CERN is a two-ring superconducting accelerator and proton-proton collider of 27 km circumference, which is in operational phase. The dipoles operate at 8.3 T, cooled by superfluid helium at 1.9 K. The operation and monitoring of the LHC require a massive amount of cryogenic instrumentation. This paper focuses on the commissioning of the cryogenic instrumentation.

I. INTRODUCTION

The Large Hadron Collider (LHC), the circular proton-proton accelerator will reach beam energy of 14 TeV (center of mass) and luminosity of $10^{34}$ cm$^{-2}$s$^{-1}$ [1]. The LHC ring consists of 8 sectors (Figure 1), each divided in: regular arc (ARC, ~2.5 km), 2 dispersion suppressors (DS, ~0.5 km) and 2 long straight sections (LSS, ~0.5 km). The operation and monitoring of the LHC require a massive amount of cryogenic instrumentation channels - most of them operating in radioactive environment - with a robust and reliable design. The cryogenic control system has to manage more than 16 000 cryogenic sensors and actuators.

II. INSTRUMENTATION ELECTRONICS

More than 800 instrumentation crates (Figure 2) are installed, connected and tested underground. They house electronic cards for the temperature (TT), pressure (PT) and liquid helium level (LT) measurements, supply electrical power to the cryogenic heaters (EH) and read the digital valve status [2].

These crates communicate through a FieldBus, based on the WorldFip protocol [3].

The Instrumentation readout is performed through 2 field-busses:

- Profibus for valve actuation. Located at 4 underground protected areas and connected through optic fiber to two PLC (ARC/LSS-surface).
- WorldFIP for TT, PT, LT, valve position reading and heaters. Up to 80 crates (radiation tolerant) distributed in the tunnel, other 20 crates/sector in protected areas.

There are also two Supervisions Systems in parallel:

- SCADA-CRYO for the LHC cryogenic operation (synoptic channels for navigation, monitoring and control of all instruments, alarms and interlocks handling, real-time and historical trends, data/event logging and archiving).
- CIET (Cryogenic Instrumentation Expert Control) for the access to the data of the WorldFIP instrumentation channels (remotely

Figure 1: The LHC sectors and interaction points. P1: ATLAS detector, P2: ALICE detector, P3: Collimation system for off-momentum particles, P4: Radio Frequency superconducting acceleration cavities, P5: CMS detector, P6: Beam abort systems for the beams extraction, P7: Collimation system for the beam halo, P8: LHCb detector.

Figure 2: Instrumentation crates under the dipoles (left) and in the radiation protected areas (right).
The commissioning of the Cryogenic Instrumentation [4] (electronics, cabling, sensors, actuators), after their installation in the LHC tunnel is done with a Mobile Test Bench (MTB).

Four Test Benches have been built at CERN to ensure the correct functionality of all electronics (three of them are used for tests and the fourth for debugging-development and for the pressure sensors calibration).

III. MOBILE TEST BENCH

The MTB (Figure 3) is based on a PXI platform, running LabVIEW™ application (Figure 4). The PXI rack houses:

- An embedded controller by National Instruments, running Windows XP.
- Two FIP communication cards for the top and bottom level of the crates with different FIP addresses.
- A 276×8 matrix module by Pickering for the switching of connections between the MTB instrumentation and the cards/cables under test.
- One programmable resistor module by Pickering for the simulation of the various sensors during the card tests.
- Various other cards (power supply card, multimeter card).

Other important components of the MTB are:

- One Keithley 2400 SourceMeter for resistance measurements in 2-wire mode and current sourcing for the 4-wire measurements.
- One Keithley 2182 Nanovoltmeter for accurate voltage sensing for the 4-wire measurements.
- A connector panel, which provides the physical interface between the MTB instrumentation and the cards/cables under test.
- One heater card test box, which houses power relays that are used to route power from the heater card to the load during the heater card test (PXI matrix can’t handle the current drawn by the load).
- One UPS, which supplies all MTB electronics with AC mains power (removal of the MTB from one crate to another, without to shut it down).

The MTB project uses Perforce, a Software Configuration Management (SCM) tool, which provides a centrally managed storage area for all files of a project, keeps detailed track of the history of each managed file (versions, changes, bug-fixes, comments, etc.) and allows collaboration amongst users.

More specifically Perforce is used to manage the LabVIEW software distribution from the developer team to the operator team, individual crate configuration files and also the results for all cryogenic instrumentation crates. All crate data stored in layout database. XML data files (CIDs, FIP addresses, type of cards, active channels, cable numbers, type of sensors etc) are used to overcome constraints such as size and complexity of layout database, network presence and speed at the tunnel.

The results are stored locally in the corresponding folder of the crate and after the completion of tests are submitted to the Perforce server and MTF - a database that stores the data related to the management of the LHC equipment. Information about electronics and instrumentation is stored in Layout Database.

The following tests are performed with the MTB:

- Consistency test: verification of matching of the crate configuration with the CERN Layout DataBase
- Card test: check electronic cards functionality
- Instrument test: check instruments presence and their functionality
- Pin-to-Pin test: validation check for cables and connectors (short circuits, low insulation resistance)
- FIP test: functionality verification of the full readout chain (sensor+electronics).

A. Monitoring

Monitoring (Figure 5) is not actually a test, but a useful tool that shows all the measurements the crate performs (crate...
not powered, missing or not connected cable, instrument improperly installed and electronic card not operational). It provides an overview of all data that the crate feeds to the FIP network (sensor measurements, noise levels, card state etc).

**D. Instrument Test**

Purpose of the test is verification that each instrument (sensor/actuator) is physically present at the machine, correctly wired and properly connected and it has the expected resistance value, given the instrument type and the machine conditions.

The test (for TT, PT, LT) is based on the 4-wire method (Figure 8), which uses two pairs of wires, one pair to apply excitation current and another pair to measure the voltage drop across the sensor.

![4-wire method for the Instrument test.](image)

**E. Pin to Pin Test**

Purpose of the test is the detection of the electrically measurable errors in cable/instrument (short circuits and low insulation resistance) with measurement of the resistance between all pin combinations of a cable connector and the resistance between each pin of the connector and ground (Figure 9) in 2-wire mode.

![Pin to Pin test.](image)

**F. FIP Test**

Purpose of the test, which is the last MTB test, is a final cross check, as it requires all the cables to be connected back to the crate. The FIP functionality is already checked during the card test. During the test the 4-wire resistance value of the sensor is returned and comparison with the 4-wire measurement of the instrument test takes place.

**G. Troubleshooting Tools**

The most common problems are related to electronic cards, instruments, cables, bad contacts, short circuits, open circuits, wrong grounding, database views refresh state,
missing info in the database, FIP communication or components of the MTB itself.

The troubleshooting tools are the stand-alone loads (connectors with discrete resistors internally connected), digital multimeter matrix relay test and cabling test.

Purpose of the matrix relay test is to check the MTB matrix for stuck open relays or relays with worn out contact. It measures the resistance of all possible paths (relay combinations) and reports all paths with resistance value higher than a predefined limit.

Purpose of the cabling test is to identify possible short circuits in the MTB wiring. The test includes the matrix, the connector panel and the MTB cables.

H. Planning

Three mobile test benches have been used, working in parallel, having two shifts per day (morning/evening), when necessary.

The test duration varied between 2 and 10 hours/crate, depending on the crate equipment and complexity.

The rate achieved is ~2-3 crates/MTB/shift in average for the ARC (tunnel) and ~1 crate/MTB/shift for the LSS (protected areas), while the commissioning duration was 2-3 weeks per sector (tunnel) and 1 week for protected areas depending on problems. The increased experience accelerated the procedure to this level. The second or third pass after the repairs for cross check has not been taken into account.

IV. CONCLUSIONS

The MTB is a valuable tool for finding most problems with cards, cables, sensors and connectors (i.e. wrong or not connected cables to the field instrument, wrong grounding/shielding in the cables or connectors, bad contacts, short circuits, open circuits, blown fuses, damaged cables or connectors, missing connections, missing info in the database, and mismatches with specifications and database).

It is a relatively complicated tool with long debugging period for exhaustive checks. Increased responsibility of the operator for results interpretation/evaluation and reporting was necessary for the commissioning of approximately 800 electronic crates and more than 12 000 cryogenic sensors and actuators.

The operational performance (within specifications) has exceeded 98% for thermometers and ~100% for other instruments.

V. ACKNOWLEDGEMENTS

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VI. REFERENCES

The Radiation Tolerant Electronics for the LHC Cryogenic Controls: Basic Design and First Operational Experience

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Abstract

The LHC optics is based in the extensive use of superconducting magnets covering 23 km inside the tunnel. The associated cryogenic system for keeping the magnets in nominal conditions is hence distributed all around the 27 km LHC tunnel and the cryogenic instrumentation submitted to the LHC radiation environment is composed of about 18'000 sensors and actuators.

Radiation Tolerant (RadTol) electronics was designed and procured in order to keep the signals integrity against electromagnetic interference and to reduce cabling costs required in case of sending the analog signals into the 30 radiation protected areas.

This paper presents the basic design, the qualification of the main RadTol components and the first operational results.

I. INTRODUCTION

The LHC cryogenic control system [1] is based on industrial Programmable Logic Controllers (PLCs) using remote input/output interfaces both to acquire the process measurements (temperature, pressure, level, etc) and to manipulate the actuators (valves and electrical heaters). Whenever possible standard commercial electronic/electrical equipment is employed and due to the tunnel environment its location is restricted to protected areas typically found at the bottom of the LHC tunnel access shafts and the two alcoves located in between two access points.

However custom electronics are necessary both because of the stringent measurement accuracy required by the temperature readout [2] and of the tolerance to withstand the environmental tunnel radiation [3]. The active electronic submitted to radiation is never installed along the LHC long straight sections in order to avoid their high radiation fluences. The electronic is designed to be of radiation tolerant grade with an aimed survival radiation dose of 1000 Gy and a neutron fluence of $10^{13}$ neutron/cm$^2$, this correspond to the expected radiation to be found in the dispersion-suppressor regions.

The sensors and actuators are often close to the beam pipes and can be subjected to an extremely high radiation as can be expected around the LHC inner triplets. For the highest doses no qualification was ever performed although most devices are inherently radiation hard owing to their mechanical design [4-6].

II. DESIGN

The most ambitious target for the LHC cryogenic RadTol electronics was the measurement of temperature that required identical accuracy as that typically found in laboratories but replicated in several hundreds of channels, subjected to the environmental radiation and electromagnetic pollution and with limited access during the LHC operation. To minimize the radiation dose the electronics is located under the main LHC dipoles using the magnetic yoke as a radiation shield.

Table 1 lists the main requirements for the analogue front-ends in order to achieve the specified temperature measurement uncertainty. The overall design is optimized for the measurement of resistance, as most of the sensors used for the LHC cryogenics are of the variable resistance type.

<table>
<thead>
<tr>
<th>Table 1: Main RadTol electronics requirements</th>
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<tbody>
<tr>
<td>Sensor resistance range [Ω]</td>
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<tr>
<td>Excitation current [µA]</td>
</tr>
<tr>
<td>Noise referred to input [µV Hz$^{-1/2}$] in the 0.01 to 5 Hz bandwidth</td>
</tr>
<tr>
<td>Sensing wire resistance [Ω]</td>
</tr>
<tr>
<td>Operation Temperature [°C]</td>
</tr>
<tr>
<td>Humidity [%]</td>
</tr>
<tr>
<td>Neutron dose [n/cm²]</td>
</tr>
<tr>
<td>Gamma dose [Gy]</td>
</tr>
<tr>
<td>Lifetime [years]</td>
</tr>
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</table>

The radiation tolerant electronics use a variety of COTS (Commercial Off The Shelf: ADC, DAC, power amplifier, passives, etc) as well as radiation hard components like the front end (quarter micron IBM CMOS technology) and the CERN voltage regulator.

Analogue components are expected to drift with both the Total Integrated Dose (TID) and the ambient temperature. In order to cope with drift in both active and passive components, a resistance comparison bridge configuration is used (Figure 1). The comparison resistors are metal foil resistors with 0.1% tolerance in order to avoid individual adjustments, with excellent stability versus temperature variation (10 ppm/°C) and immune to the expected TID. The requirements shown in Table 1 require that the acquisition ADC to be at least 14-bit in resolution. The errors will be mainly provoked by non-linearities in the ADC or the front-end amplification chain that include the differential amplifier and the switching excitation current source.
The front end ASIC is not designed to behave as an instrumentation amplifier and thus its main characteristic are expected to vary significantly with ambient temperature (Figure 2a). The ASIC drift is compensated (Figure 2b) by the bridge configuration and switching of the excitation current and input stage (Figure 1) that eliminate thermoelectric effects and voltage offsets.

The electronic cards are integrated inside a crate that provides a backplane for exchanging analogue and digital signals. When located in the tunnel the crates can be exposed to humidity in case of degraded vacuum as water condensation may occur on the outer vacuum vessel of the superconducting magnets. To cope with this a cover has been provisioned for all tunnel crates; it provides a gap in order to permit natural convective ventilation.

The thermal design was considered from the first step, it aimed to provide sufficient ventilation without active cooling. Larger than usual heat sinks are used and as a consequence the cards have a depth twice than usual as those used for pcb cards with a standard height of 3U or 6U. Active cooling would be a maintenance hindrance due to the large number of crates (ca 800), the restricted access conditions and the fact that the tunnel is a radiation controlled area. The overall thermal dissipation is expected to increase with the TID as leakage currents and voltage offsets are much affected by radiation. The additional thermal dissipation is estimated from measurements performed during the radiation qualification campaigns.

The internal components temperature and air velocities field was simulated in operational conditions [7]. These simulations were used to determine the ratio between the overall perforations area and the total area for the top and bottom covers. The highest temperature are expected for the linear power amplifiers supplying the electrical heaters and the superconductive liquid helium level gauges, the CERN radiation hard voltage regulators and the diode rectifiers in the dc power distribution card. Figure 3 show the surface temperature of the cards used for measuring the level of liquid helium. According to the simulations the thermal design has sufficient margin to cope with the worst case estimations.

The electronic cards are controlled by a set of FPGAs (Field Programmable Gate Arrays) that communicate with the industrial fieldbus interface that is composed of the bus controller and the line driver. WorldFIP® fieldbus has been selected for the radiation tolerant electronics.

### III. Radiation Qualification

Radiation qualification campaigns were performed in “dirty” LHC like conditions in a target area (TCC2) fed with beams incoming from CERN Super Proton Synchrotron (SPS) where the radiation was composed of many types of particles with a large energy spectrum and in dedicated radiation facilities for characterizing electronic components [8]. The dedicated facilities were: ITN nuclear reactor in Lisbon-Portugal for neutron and TID studies, and the cyclotrons at Louvain-Belgium and PSI-Switzerland for Single Event Effects (SEE) and TID studies.

The TCC2 area was used to qualify the discrete components like the reference resistors used in the comparison bridge and for characterizing assemblies that are...
too big for being qualified in either the nuclear reactor or the cyclotrons.

The front end IBM quarter micron ASIC is radiation hard by design and no degradation of its performance was measurable up to a TID of 20 kGy in gamma radiation.

Figure 4 shows data obtained in the Lisbon reactor for the effects of neutron fluence on the output voltage for the JFET input stage power operational amplifier OPA541; it withstands a neutron fluence of $5 \times 10^{12}$ neutron/cm$^2$ without major effects in the operating parameters [9].

![Figure 4: Neutron fluence effects on the maximum voltage swing for the power amplifier OPA541.](image)

Digital and mixed analogue digital COTS were investigated for SEE and if required for determining the maximum TID before failure. SEE were never observed when irradiating with a 60 MeV proton beam the 16-bit successive approximation ADC ADS7801UB [9]. The ADC test was performed within the resistance measurement setup described in chapter II; Figure 5 shows the degradation of the resistance measurement with TID. Above 500 Gy the measurement errors exceed the LHC tolerance. It shall be noted that the ADC internal voltage reference was very dependent on the TID and an external reference is employed for the radiation tolerant electronics. During the ADC test the ACTEL FPGA family A54SX fabricated in anti-fuse technology was also irradiated, not a single SEU was observed. To increase the radiation robustness, the FPGAs are programmed in triplicate logic. The overall current consumption increases by about an order of magnitude.

![Figure 5: TID effects on the measurement error](image)

The 12-bit DAC AD565 fabricated in fast bipolar technology with a zener internal voltage reference is capable of withstanding a neutron fluence exceeding $3 \times 10^{13}$ neutron/cm$^2$ and 1.9 kGy, that far exceeds the requirement for radiation tolerant electronics for LHC cryogenics. Figure 6 shows the effect of neutron fluence on the internal voltage reference, this was one of the many parameters measured during the test. Self-annealing effects can be seen on Figure 6 as shown by the sudden drops on the reference voltage that are actually observed during irradiation stops.

![Figure 6: Neutron fluence effects on the 12-bit DAC](image)

The communication relies on a microFIP™ mezzanine card manufactured by Alstom; it includes the bus controller and the line driver. The communication card is used in the microcontroller mode and the FPGAs are programmed in such a way as to emulate a microprocessor. Single Event Upsets (SEU) effects were investigated in the Louvain cyclotron [11]; the rate of errors is higher for memory bits in the “0” state as shown in figure 7. By calculating the error cross section and using the modeled LHC radiation fluences for particles with energies higher than 20 MeV it is estimated that 2 errors per bus node and year will occur. Erroneous bits are easily detected and corrected by the controllers located in the surface main control rooms. However an SEU in the configuration memory may require a reset of the fieldbus card; over 4 tested samples one such event was detected and required a complete reset. The maximum TID range for the 4 samples was 800 to 1300 Gy, only one card failed at 800 Gy demonstrating an excellent radiation tolerance for this mezzanine card.

![Figure 7: Single Event Upset (SEU) effects](image)
IV. PROCUREMENT

The PCB manufacturing, card assembly and crate mechanical construction was subcontracted and more than 10’000 assembled PCB and 800 crates were procured.

The most critical COTS were purchased and delivered by CERN. Obsolescence has been an issue for the 16-bit ADC ADS7807 that has been replaced by a pin-to-pin compatible circuit ADS8507. This new ADC generation was required for the project because the numbers of some cards increased and by a lower yield than expected in the assembled PCBs. Cards using the new ADC are restricted to radiation protected areas.

Initially the card qualification pre-series were plagued by problems related with unexpected modifications of the PCB electrical inter-connection layout and by corrosive residues that could reduce the usable lifespan of the electronics.

During the series manufacturing manual rework has produced opened vias because of an inappropriate solder tip temperature and a PCB material with too narrow margins in what concern temperature excursions. This manual rework occurred in several production batches and to estimate the potential card failures an accelerated test was performed; it consisted of 200 temperature cycles between -20 and 80 °C. The fraction of damaged cards reached 6%, indicating that the same failure rate will occur for about 3’000 cards. The foreseen spares are not sufficient if such a high failure rate actually occurs.

V. PERFORMANCE IN THE FIELD

The LHC radiation tolerant electronics for the tunnel cryogenics control system and its associated instrumentation and communication infrastructure have been completely commissioned [12-14].

Before installation of the LHC magnets the cryogenic distribution line was validated. The acquisition electronics was of the industrial type that is not optimized to measure thermometers meant to be operational at cryogenic helium temperatures. Figure 9 shows, at “tunnel” temperature before cool-down, the temperature profile along sector 81 using either industrial or custom radtol electronics. Qualitatively the radiation tolerant electronics when compared with the industrial type, yield temperature measurements in a narrower band and there is no gap between the platinum and Cernox™ temperature readouts; Cernox™ being capable of measuring temperatures in the range 1.2 to 350 K. The superior performance of the custom electronics is due to its compensation of thermoelectric potentials that is absent on the industrial type and when measuring thermometers in the range 1.6 to 20 K the excitation current is lower reducing the thermometer self-heating effects.

The measurement at the nominal superconducting magnets operational temperature is within the specifications that at 1.7 to 2.2 K have an uncertainty tolerance budget of +/- 0.01K shared in equal parts between the readout electronics and the temperature sensor. Figure 10 shows a typical temperature measurement along a 107 m LHC standard cell, composed of 6 dipoles and 2 quadrupoles, in nominal conditions. Thanks to the extremely high thermal conductance of superfluid liquid, the 107 m long cell is in quasi-isothermal conditions permitting to assess in-situ the quality of the temperature readout; the temperature spread is well within the LHC tolerance.
The LHC has already been commissioned with circulating beams and no major interference problem has been observed with the dc power supplies, the kicker system or any major LHC system. Some minor grounding problems required additional filtering when using front-end cards with galvanic insulation.

VI. CONCLUSIONS

The radiation tolerant front-end electronics for the LHC cryogenic controls has been commissioned for all the LHC sectors.

The cross-correlation between the various measurements (temperature, pressure, liquid helium level, etc) confirms that they are well within the LHC requirements. In particular for the measurement of temperature, the obtained uncertainty is not only equivalent to that previously obtained in the laboratory but the acquisition electronics are made to survive an environment far more hostile to that typical of the industrial environment and furthermore the measurement system has been massively replicated.

The overall radiation tolerant electronics has been qualified and the weakest component is the 16-bit ADC that during the irradiation campaigns is not able to withstand TID in excess of 400-500 Gy, lower than the 1000 Gy design target. It shall be noted however that, for all the tested devices, the qualification dose rate is extremely high and during the LHC operation self-healing annealing effects will most probably contribute to extend significantly the components lifetime in what concern TID as well as the neutron fluence.

During procurement several manufacturing non-conformities have been discovered that may demand the fabrication of new cards. As for any radiation tolerant design obsolescence will be an issue for any renovation or extension project.

The next challenge will be the understanding of the modes of failure in order to define a maintenance plan that shall take into account the accumulated radiation (TID and neutron fluence) and the access restrictions.

VII. REFERENCES

Results from the commissioning of the ATLAS Pixel Detector

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Abstract

The Pixel Detector is the innermost detector of the ATLAS experiment at the Large Hadron Collider at CERN. It is an 80 million channel silicon tracking system designed to detect charged tracks and secondary vertices with very high precision.

After connection of cooling and services and verification of their operation, the ATLAS Pixel Detector is now in the final stage of its commissioning phase. Calibration of optical connections, verification of the analog performance and special DAQ runs for noise studies have been performed and the first tracks in combined operation with the other subdetectors of the ATLAS Inner Detector were observed. The results from calibration tests on the whole detector and from cosmic muon data are presented.

I. INTRODUCTION

In order to fulfill the requirements of coverage up to $|\eta| < 2.5$, vertex resolution below $15 \mu m$ in the $R\phi$ plane and below $1 \text{ mm in } z$, high efficiency with low material budget and radiation hardness to operate after a total dose of 500 kGy or about $10^{15} n_{eq} \text{ cm}^{-2}$, the ATLAS Pixel Detector provides three hits over the full rapidity range, has the innermost layer at a radius of 5 cm and a pixel size of $50 \times 400 \mu m^2$. The sensitive area of 1.6 m\textsuperscript{2} is covered by 1744 modules distributed over three layers in the barrel and three disks for each endcap, containing a total of 80 million electronic channels. Only the basic features of the modules and of the read-out system are presented here, a detailed description can be found elsewhere [1].

A. The pixel module

Modules are the basic building blocks of the active part of the Pixel Detector. Each module consists of the silicon sensor with a volume of $60.8 \text{ mm} \times 16.4 \text{ mm} \times 250 \mu m$, 16 front-end electronic chips bump bonded to one side of the sensor and a flex-hybrid glued to the other side of the sensor containing a Module Control Chip (MCC) to receive and transmit digital data out of the module (see Figure 1). The front-end chips are about $200 \mu m$ thick and the flex-hybrid $100 \mu m$. During production the radiation hardness of the modules was tested and they are expected to be fully operational after the expected lifetime dose.

The readout chip contains 2880 pixel cells arranged in a $18 \times 160$ matrix, each (see Figure 2) with an analogue and a digital block. The analogue block contains a charge sensitive preamplifier and a discriminator in which the amplified charge signal from the sensor is compared to a tunable threshold. The digital read-out part transfers for each hit the address, the timestamp of the leading edge and the timestamp of the trailing edge to the buffers at the chip periphery where the Time-over-Threshold (ToT) is computed by subtracting the leading from the trailing edge timestamp. A feedback circuit in the preamplifier causes a nearly linear return of the pulse to the baseline, so that the ToT can be used to measure the signal amplitude and therefore the deposited charge.

The threshold and the feedback current are tunable globally for each chip and by a fine adjustment for each pixel.
B. The read-out system

The communication between modules and off-detector read-out electronics occurs via optical links (see Figure 3), whose architecture was inherited from the ATLAS SCT [2]. The electrical-optical interfaces are the opto-board on the detector side and the Back Of Crate card (BOC) in the counting room racks, where the Read Out Drivers (RODs) are housed in 9 VME crates, each connected to a BOC at the crate back-plane. Each opto-board serves the six or seven modules building a barrel half-stave or a disk sector. A BOC can be connected to up to four opto-boards at a readout speed of 40 Mb/s, which is sufficient for the outermost layer. For the middle layer and the end caps two opto-boards are connected to the same BOC, allowing a maximum speed of 80 Mb/s, while the innermost layer must be read at up to 160 Mb/s, so that only one opto-board can be connected to each BOC.

![Figure 3: Architecture of the readout system](image)

In the trasmitter (TX) plug-ins of the BOC, the clock signal and the commands sent by the ROD to the modules are Bi-Phase Mark (BPM) encoded and converted into an optical signal by a Vertical-Cavity Surface-Emitting Laser (VCSEL) array connected to one fiber per module. On the opto-board a PIN diode array receives the optical signal and a Digital Optical Receiver Integrated Circuit (DORIC) decodes it and extracts the clock.

The data sent by the modules are encoded in non-return-to-zero (NRZ) format and converted to an optical signal on the opto-board in a VCSEL Driver Chip (VDC) followed by the VCSEL array. Depending on the rate, one or two fibers per module are used and the number of VCSEL arrays and VDCs per opto-board varies accordingly. The receiver (RX) plug-in of the BOC performs the conversion from optical to electrical signal and the decoding with a PI N diode array and a Data Receiver ASIC (DRX).

The amplitude of the VCSEL current in the opto-board is driven by the $I_{\text{set}}$ current, that depends on a tunable voltage ($V_{I_{\text{set}}}$). Once the optimal laser power for the whole opto-board has been determined, threshold and data delay can be adjusted for each RX-channel of the BOC.

In the ROD (see Figure 4) two different paths are used for data and for calibration, due to the different occupancy. At the typical occupancy of noise or physics data ($\leq 10^{-4}$) the data fragments can be sent to the ATLAS common part of the Read-Out System (ROS) [3] via the S-Link. During calibration scans up to 1/32 of the pixels can be injected at the same time, so that the information on each single hit has to be summarised into histograms and only these are transferred out of the ROD to the Single Board Computer (SBC) of each crate via VME connection. A further reduction of the exported data can be obtained by performing a fit on the slave DSPs and histogramming only the resulting fit parameters, as is done for the determination of the discriminator threshold and noise of each pixel with an S-curve fit to the pixel response as a function of the injected charge.

![Figure 4: Block diagram of the ROD.](image)

II. CALIBRATION

The calibration of the ATLAS Pixel Detector cannot take place during normal data taking and needs dedicated software packages, due to the different data path that has to be used. In order to steer the whole system from a single GUI, a distributed system was developed, based on Inter Process Communication (IPC). A block diagram of the calibration infrastructure is shown in Figure 5.

![Figure 5: Block diagram of the calibration infrastructure.](image)

From the GUI, called Calibration Console, the user can start a scan, which is actually executed on the SBC of each crate by sending commands to the RODs. In this way the time consumption to run a scan on the whole detector is not much higher than for one of the slowest RODs (connected to 26 modules). The scan configuration can be customised from the Console and is saved to a database before starting the scan, from where it is
read by the crates. The Console monitors the progress of the scan, reading the information published about each ROD on the Information Server (IS). The histograms produced by the scan are available for fast reading in the Histogram Server and are automatically archived to a file on disk.

A scan only collects the data for which the hardware is necessary, while, whenever possible, the analysis of the histograms, computing the actual calibration constants, is run separately, leaving the hardware free for physics data or for the next scan. The analysis is started by the user from the Calibration Console, where the cut values can be customised, and the processes, one per ROD, are queued by the Analysis Scheduler and executed by the next free worker in the analysis farm. The analysis configuration is saved to a database, the monitoring of the analysis progress is based on IS and the histograms to be analysed are retrieved from the histogram server. The calibration constants are saved into the Analysis Result database and can be converted into the format necessary for the Offline Conditions database, to be used for data reconstruction and simulation.

Additional monitoring tools were developed, e.g. the ROD Status Monitor, that displays the ROD status presently published in IS as well as the errors per ROD and per module during scans and data taking, or the SBC Monitor, showing CPU and memory consumption of the SBCs.

III. COMMISSIONING

The detector was assembled with its mechanical support between March and June 2007. During assembly tests were performed to check the connections between the modules, the optics, boards and the low and high voltage supply lines in the Patch Panel on the support (PP0). Procedure and results of the connectivity test can be found elsewhere [4].

A. Installation and connectivity test

The Pixel-package was installed in the ATLAS cavern in July 2007, but remained unconnected for a few months, waiting for the outer parts of the Inner Detector (ID) to finish their cabling. Until December, the services were connected from the counting rooms up to PP2, inside the muon detector, and they were tested to detect malfunctioning as well as discrepancies between the actual connections and the connectivity database. Furthermore the cooling exhaust pipes at PP1 (at the ID end-plates) were replaced, since they had been damaged by corrosion.

The connection of services and optical fibres at PP1 could only start in February 2008 and also in this case tests were performed during connections to check for damages and differences from the database. The cables and fibres after connection at PP1 are shown in Figure 6. A general fibre swap at the BOC side was found and most of the fibres had to be reconnected in a few days.

The light transmission to and from the detector was tested: the light power on the TX channels was found to be lower than during assembly, as expected considering the different fibre attenuation. During the test period TX channels have been dying at the very high rate of a few per month. Their behaviour was found to be compatible with ElectroStatic Discharge (ESD) damage during production and the higher number of dead channels with respect to SCT could be explained by the fact that the SCT lasers were kept off when not in operation, while the Pixel ones were on all the time. New TX plug-ins are being produced both for Pixel and SCT, with particular care to avoid ESD damage.

Since in April the modules could not yet be cooled down, only one FE was configured per module and a threshold scan over 1/10 of the pixels of this FE was performed to make sure that the sensor was biased.

B. Sign-off before Inner Detector closure

Cooling was available starting from April 25th. Each loop, cooling 26 modules in the barrel or 12 modules in the endcaps, was tested singularly, measuring temperatures, back-pressure and heater power with different detector configurations, corresponding to different heat loads. While some loops were unstable with the detector off, most of them could be easily stabilised with configured modules, dissipating about 4 W each. Three endcap loops were found to be leaky and will not be operated for normal data taking, but could be kept on up to now, to complete the commissioning of all the modules. On May 1st, 77 of the 88 Pixel cooling loops had been tested, when the system had to be turned off due to a cooling plant accident and the Inner Detector was closed a few days later, before the foreseen sign-off could be completed.

Before the cooling accident, about 900 modules could be tested by performing a threshold scan on all the pixels: 8 modules with open high voltage connection and one without clock were identified and they cannot be recovered, two modules were swapped and the database was corrected accordingly, for 4 modules the threshold was not tuned in the configuration used at the moment and 3 modules show threshold scan results similar to those for an open high voltage connection, but a direct measurement was either not yet performed or it did not confirm the open line. The number of dead pixels in the tested modules did not in-
crease significantly with respect to the measurements performed during module production. Based on a sample of 25 million pixels, the electronics noise was measured from the S-curve fit to be on average 166 electrons. Only about 1% of the pixels have noise higher than 200 electrons, while for a further 1% the fit did not converge.

C. Preparation for first data

In the cooling system three compressors were damaged due to prolonged slippage in the magnetic coupling between the motor and the compressor shaft. They could be repaired and the contaminated coolant was replaced, so that the Pixel detector could be cooled again in time for the beam-pipe bake-out, that took place successfully at the end of August. The coolant loss was at the level of 1 kg/h during bake-out, so that further cooling commissioning, until the 11th of August, was necessary to find and possibly remove the leaks.

![Figure 7: Communication errors as a function of threshold (y axis) and data-delay (x axis) settings in an RX plug-in at fixed opto-board laser power for six channels with clock (left) or pseudo-random pattern (right). The point indicates the chosen settings.](image)

To restart operation with cooling, a new tuning of the opto-links was necessary. While modules have to be kept at about 0°C, opto-boards cannot operate stably at this temperature, therefore heaters were installed to keep the opto-boards at a higher temperature. In order to preserve the opto-board lasers from dying, it was first tried to tune the opto-links with the opto-boards at 10°C, but slow turn on effects were observed in some channels at this temperature, i.e. some channels reached the full power only after a few microseconds. The opto-link tuning is normally performed by sending clock to the modules and reading it back at different values of $V_{th}$, and for different settings of the threshold and data delay in the RX plug-in. The number of errors with respect to the expected signal is plotted versus the chosen parameters and values are chosen for which no communication errors were reported (see Figure 7, left). This method is fast enough to test the whole parameter space with the required granularity, but is not sensitive to slow turn on. A scan at fixed laser power and lower granularity, in which a pseudo-random pattern is sent to the modules and each returned bit is compared with the sent one, shows in case of slow turn on that the point chosen by the tuning algorithm is in a region with communication errors (see Figure 7, right). Most of the links could be tuned when the opto-boards were instead warmed up to 20°C, that was therefore chosen as the operating temperature.

On August 28th the whole detector could be turned on, 1662/1744 modules showed no communication errors after opto-link tuning and were further tested. From standalone data taking with a random trigger, the noise occupancy of each pixel was determined. The few modules limiting the data taking rate were disabled and about 5000 pixels with occupancy above $10^{-5}$ were masked out. In this way the average number of clusters per bunch crossing could be reduced from 100 to less than one. It was observed that most of the clusters are produced by single noisy modules and mostly concentrated on a small number of pixels inside them (see Figure 8).

![Figure 8: Noise hits per module in a layer (left) and per pixel in a module (right).](image)

The plan for calibration in September was to collect a complete set of constants necessary for offline reconstruction and simulation, based on the threshold and ToT tuning performed during module production. Until September 20th the threshold scans were completed, while the ones involving timing and ToT were only partially done. The noise occupancy data were compared with the threshold scan results and a very good overlap was found between the pixels with high occupancy and the ones failing the S-curve fit after the scan. The threshold scan results confirmed the disconnection of some modules from the high voltage supply and the presence of one or two bad FEs in 8 modules, for which no pixels could be fitted.

D. Cosmics data

The Pixel detector was included in a combined ATLAS run for cosmic muons for the first time on September 4th, but since the timing was not tuned properly yet, no tracks with pixel hits were recorded. After changing the time window for read-out and extending it to 8 bunch crossings, on September 14th the first track with 7 Pixel hits and 16 SCT hits was recorded. The corresponding event display is shown in Figure 9.

The few tracks available after a few days of running could already be used to align the barrel layers with respect to the SCT, while smaller units, like the staves and maybe even the modules, need higher statistics, but could still be aligned with cosmics data.

Since the stability of the beam cannot be assured yet, the high voltage of the modules is not turned on during beam commissioning.
IV. Summary

Running the opto-boards at 20°C it was possible to tune the opto-links stably for about 95% of the modules, that could be further calibrated and used for data taking of cosmic muons with the threshold and ToT tuning obtained during module production. Three cooling loops, corresponding to 36 modules, will not be operated because they were found to be leaky, but the modules could be still calibrated and are kept on for commissioning. As long as the priority lies by stable running, there is no necessity to retune thresholds and ToTs and the modules failing calibration or giving errors during data taking will only be tested at a later time. The identification of bad pixels agrees well between calibration and data taking so that both methods can be combined. Cosmics tracks for alignment are being collected, but for the safety of the detector the high voltage cannot be kept on during beam commissioning.

References


Figure 9: Event display of the first track with Pixel hits.
Design, production and first operation of the ALICE Silicon Pixel Detector system


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Abstract

The ALICE Silicon Pixel Detector (SPD) constitutes the two innermost barrel layers of the ALICE experiment. The SPD is the detector closest to the interaction point, mounted around the beam pipe with two layers at r=3.9 cm and 7.6 cm distance from beam axis. In order to reduce multiple scattering the material budget per layer in the active region has been limited to ≤1% X₀. The SPD consists of 120 hybrid silicon pixel detectors modules with a total of ~10⁷ cells. The on-detector detector components design and production are reviewed. First system and detector electronics. In this contribution the SPD is the interface to the ALICE trigger, data acquisition, control located in the control room, is housed in 20 VME boards; it and an optical transceiver module. The readout electronics, read-out is based on a multi-chip-module containing 4 ASICs and an optical transceiver module. The readout electronics, located in the control room, is housed in 20 VME boards; it is the interface to the ALICE trigger, data acquisition, control system and detector electronics. In this contribution the SPD detector components design and production are reviewed. First operation results are reported.

I. SPD detector overview

The SPD [1] consists of 120 detector modules, the half-staves, which are arranged in two cylindrical layers at 3.9 and 7.6 cm from the beam axis. Each detector module comprises two ladders; a ladder consists of 5 pixel chips [2] with 8192 pixel cells each, bump bonded to a sensor using Sn-Pb bumps of 20 μm diameter [3]. In order to achieve the lowest material budget, the pixel chips are thinned to 150 μm and the sensor thickness is 200 μm. In total the SPD contains 9.83 x 10⁶ pixels. At the end of each half-stave a multi chip module (MCM) [4] reads out the 10 pixel chips. The MCM contains 4 ASICs, the rx40 [5] to receive an LHC synchronous clock and serial data on optical fibers, the digital pilot chip [6] to configure and read-out the pixel chips, the 800 Mbit/s serializing chip GOL [7] to send the data on one optical fiber from the detector to the control room and the analog pilot chip [8] to provide bias voltages to the pixel chip. The electrical connection between the pixel chip and the MCM is done via a aluminum based multi-layer flat cable, the pixel bus [9]. An aluminium-kapton foil, the grounding foil, is electrically separating the half-stave from the carbon fiber support structure. Cooling pipes are directly integrated into the carbon fiber structure [10]. Copper and kapton flat cables deliver electrical power to the half staves.

II. SPD system components

A. Pixel ASIC

The pixel ASIC [2, 11] contains 256 x 32 pixels and the read-out is based on a binary concept, where the full matrix is shifted out on a 32 bit bus in 256 consecutive 10 MHz clock cycles. Each pixel chip generates a pulse (fast-Or) whenever at least one pixel cell detects a particle signal above threshold. The fast-Or is used to implement a prompt trigger which contributes to the ALICE L0 trigger.

The functionality of the ASIC from the first engineering run proved to be acceptable. Three production runs were carried out between 2001 and 2003. The ASIC working parameters can be adjusted via internal DACs, remotely programmable. The optimization was done using a dedicated MCM emulator test system based on a wavere prober developed for that purpose. The same system was also used to test the ladders.

B. Multi-chip module ASICs

The ASICs mounted on the MCM are all produced in 0.25 μm CMOS using radiation tolerant layout techniques. Tripliation of sensitive logic cells performs SEU protection. A VME and FPGA based prototype was used to define and verify the functionality of the digital pilot chip. This VME board was also used in the pixel chip and ladder acceptance test system. The first version of the pilot chip was designed in 2002 and successfully tested. In 2003 a modified version was produced which included the functionality to transmit the fast-Or signals off the MCM. The fast-Or output of the pixel chip indicate the presence of at least one hit in the pixel matrix. The analog pilot was designed and tested during 2003. For the digital and the analog pilot chips dedicated test boards were produced. The full quantity of both chips was produced in multi project wafer runs. The rx40 and GOL chips were produced in common LHC projects and were used without modification.

C. Multi-chip module

The first prototype was based on a 5 layer FR4 PCB. This version used the rx40 block inside the digital pilot. However,
The pixel bus design flow and test systems

The connection between the pixel chips and the MCM is done with a 5-layer aluminum kapton based flat cable, the pixel bus. The pixel bus is 166 mm x 13.8 mm x 0.35 mm in size. Aluminum was chosen as conductor in order to reduce the material budget of the half-staves to a minimum [4]. No commercial processes for such components could be found. The CERN printed circuit workshop developed a custom process and produced the full quantity.

Two layers are reserved for power and ground connections. The pixel chip has separate connections for analog and digital supply. However, tests showed that the two supply connections can be connected together outside the chip without loss of performance. Three planes were used for the transmission of signals, the 32-bit data bus, the 10-bit fast-Or bus and the 25-bit control bus.

The bus manufacturing principle [9] is to glue three aluminium kapton foils together which form the first two 50 µm layers containing ground and power lines and the first 10 µm thick signal layer. Then a kapton foil is attached and the vias to the preceding layer are generated. For layer 4 and 5 10 µm aluminium is deposited via vacuum evaporation, onto a kapton foil and again the vias to the preceding layer are formed. As the production of aluminium vias is a delicate process and in order to reduce the number of vias each layer was made accessible for wire bonding on the edge of the bus by reducing the width by 500 µm compared to the layer below.

The R&D process for the bus was started with a 7 layer copper based prototype where the analog and digital power supplies were still separated. The first prototype bus and two ladders were glued next to each other and wire bonded. This required the bus connections to be swapped compared to the final design where the ladders are sitting below the bus. On this mirrored bus electrical acceptance tests were conducted taking the different resistivity between aluminum and copper into account. The next prototype step involved fully functional 5 layer copper busses where also the mechanical dimensions have been adapted to real needs and the first detector half-stave was assembled. In the last stage aluminum prototypes and production series were constructed. The major difficulties were to find the correct process parameters for the aluminum deposition and etching of the vias. While the edging process for copper micro vias is well known, the chemical process parameters for aluminum needed to be determined. As the process is run in many sequential steps where each step is potentially destructive, each new layer was tested for short circuits or interruptions.

The final bus was equipped with SMD decoupling capacitors, pt1000 temperature sensors and pullup resistors. As PCB testers are not suited to test automatically PCBs with mounted SMD components and are also incompatible with the fragile aluminum bonding pads, each bus was temporarily wire bonded onto a carrier card which was connected to a test system emulating the pixel chips and MCMs, thus testing each line on the pixel bus. This cumbersome test procedure was required to avoid attaching a defective bus to the expensive detector module components, as this assembly is hardly reworkable.

The R&D process started in 2001, the first mirrored/non-mirrored copper busses were delivered 2002/2004, the first aluminum busses were delivered 2005 and the full production was finished in 2007.

E. SPD off-detector read-out electronics

The 120 half staves are controlled and read-out via 20 VME based electronic boards, the router cards, which are sitting in the control room located at about 100 m from the detector. Each of the router cards houses 3 daughter cards (link receiver) which communicate with two half staves. The routers multiplex the data from the link receiver cards and send them via the ALICE detector data link (DDL) to the DAQ. Furthermore the routers form the interface to the ALICE central trigger processor via the TTC interface and detector control system via a VME connection.

One of the challenges during the production of the router cards was to gain experience with the mounting of large ball grid arrays (BGA) and produce 9U VME cards with a flatness compatible with BGA mounting. The router cards contain BGA packages with 1020 pins. The acceptance test are based on boundary scan methods allowing to pin point directly faulty solder connections using a board wide JTAG chain. In certain cases FPGAs with few soldering faults were found, in other cases the soldering faults were so severe that not even the
The general testing of the router and link receiver printed circuit boards was rather straightforward. The electrical functionality was verified using the JTAG boundary scan method. The processor functionality, the functionality of the optical components and the FPGA firmware of the link receiver cards were verified using a dedicated hardware test bench which emulates the components connected to the link receiver card. In general the basic commissioning of the FPGA firmware was simple as the entire system including the detector ASICs and PCB board connections was simulated using HDL system simulations prior to board fabrication. This allowed the verification of the interfaces to the DAQ, the trigger, the ALICE DCS and the SPD detector modules already before the production of router and link receiver cards and again the test and integration of the hardware and software systems was constrained by the deadlines for the installation of the SPD in the experiment. The test period went from mid 2006 to mid 2007 [3].

**G. Surface detector system test**

The full detector system including read-out, DAQ, DCS, trigger, cooling, optical and electrical cabling and power supplies was integrated and tested in a dedicated area in the CERN Departmental Silicon Facility during several months for most components. Functionality tests of the full detector were performed. A burn-in of the off- and on-detector electronics was carried out. At the same time as much as possible of the read-out electronics was commissioned. The progress in the test and integration of the hardware and software systems was constrained by the deadlines for the installation of the SPD in the experiment. The test period went from mid 2006 to mid 2007 [3].

**H. Installation of electronics, power supplies, electrical and optical cables**

The SPD off-detector read-out electronics is installed in the surface control room in 2 VME crates and thus easily accessible for maintenance. The low voltage system is based on CAEN EASY 3000 [15] system. The control main crate is located in the surface control room and the LV supply modules are located in the cavern. 20 A3009 modules serve the detector. Each module has 12 floating channels with differential sense lines for 6 half-staves without local regulation - 1.8V for the pixel chip supply and 2.5V for the MCM supply. The maximum length of the LV power supply cables is about 38 m. The bias voltage for the silicon sensors is provided from the control room using CAEN 1519 modules housed in the main control crate. 12-channel coax cables run from the control room all the way to the sensors. The cable length is about 100 m.

The two optical input lines of the MCM carrying clock and serial data are routed from the control room to the 120 half-staves in about 110 m. The data lines of the half-staves go to the pixel trigger crate in the cavern on a 38 m long path on the A side of the detector (36 m on the C side). There the fibers are split, one branch goes to the trigger processor, the other continues to the control room. The length of the fibers from the splitter to the control room is about 70 m. All fibers in the system have been matched in their length with a precision of 30 cm for the different sections. This ensures that the phases of all half-staves are aligned to each other without the need of individual delay tuning. For the data lines from the half-staves to the PIT the cable path has been designed to be as short as possible such that the fast-Or signal is delivered to the pixel trigger processor in the shortest possible time.

Due to the layout of the ALICE experiment between the control room and the half-staves patch panels have been installed creating 5 break points. These break points have a strong impact on cost and reliability. The test of the detector with power on could only be carried out once the cables and cooling pipes were installed. Some patch-panels were then no longer accessible. Therefore during the installation intensive test sequences were carried out in order to ensure the integrity of the connection.

The R&D phase started early 2006 and the production was finished in end 2007.

**F. Pixel trigger processor**

The SPD pixel chip has a digital output, the fast-Or output, which is activated if at least one out of the 8192 pixels has been hit. The fast-Or output of each pixel chip is transmitted on the optical fiber to the pixel trigger processor (PIT). The PIT extracts the 1200 fast-Or bits and applies the pixel trigger algorithm in order to provide a L0 input trigger signal to the ALICE central trigger processor CTP within 800 ns [13, 14]. The PIT system comprises one 9U sized mainboard with one Xilinx Virtex4, 1513 pin FPGA acting as the trigger processor. The main board carries 10 daughter cards which receive 12 optical fibers each, extract the fast-Or bit information and send it to the main board. As the system is very compact in design initial concerns about cooling issues where studied using cooling simulation models. The design and production of the boards were straightforward and both the prototype and production boards were working immediately. This was possible due to the learning phase during the production of router and link receiver cards and again the intensive use of simulation verification on board level prior to the production of the boards.

The R&D phase for the system started early 2006 and the production was finished in end 2007.
Transient voltage suppressors (TVS) where installed as close as possible to the detector [15] in order to protect the detector modules from electrical over stress. The design and production of the cabling network started in 2005 and was terminated in 2007. The installation of the electrical and optical cables was started at the end of 2006 and completed in 2007.

I. Interlock system

The temperature of each half-stave and MCM is constantly measured with 11 sensors (1 per read-out chip and 1 per MCM). The information is sent via the optical link to the control room, where the read-out electronics and the software based DCS evaluate the temperature and control the power supplies. In addition to this interlock chain a PLC based system in the cavern reads the temperature sensors from the half-staves and acts as a direct hardwired interlock to the power supplies. The system was conceived in 2006 and installed in 2007.

III. System, commissioning and first runs

Fig. 1 shows a simplified block diagram of the SPD system. The fast-Or signals from the half-staves are processed in the PIT to form the SPD L0 trigger decision which is forwarded to the ALICE central trigger processor (CTP). Via the TTC system the clock and the trigger decision are received by the SPD off-detector electronics. Upon reception of a positive trigger decision the SPD is read-out via the off-detector electronics.

The ALICE silicon pixel detector has been installed inside the experiment in June 2007. The detector surrounds the beryllium beam pipe; the minimum distance to the inner layer modules is ~5 mm. In the following months the silicon strip and silicon drift detectors as well as the Time Projection Chamber (TPC) have been moved over the SPD. The cabling and cooling connections could be completed only in November 2007, when the mini-frame supporting the overall cabling was lowered into the cavern. Extensive tests of the electrical and optical cabling have been performed before actually powering the system to avoid damage to the detector caused by any possible cabling mistakes.

In December 2007 a two-week cosmic ray run has been carried out in which one side only of the SPD was operated. The second side could not be operated because the necessary power supply modules had not been delivered at that time. Another cosmic ray run took place in February/March 2008; this was the first time the full detector was operated. Both cosmic run periods allowed commissioning tests of the cooling system, the cable and power supplies and the detector electronics. The first cosmic events have been recorded in the SPD in February 2008. Data acquisition test and noise run tests verified that detector parameters were unchanged compared to the laboratory setup. In the full ALICE setup the SPD maximum design data taking rate of 3300 Hz was verified. Long term and high trigger rate tests allowed to examine and eliminate rare multi-buffer overflow conditions. Dedicated trigger test sequences were performed where L2 accept and reject signals were mixed. For each L2 accept event test pulses were initiated in the front end electronics. Off-line verification proved that each L2 accept was recorded whereas L2 rejects were deleted. The pixel trigger processor was then setup and thus allowed the commissioning of the detector with the pixel trigger to capture cosmic events. The first cosmic events have been recorded in the SPD in February. Since then the detector has been operated almost without interruption. Figure 2 shows an cosmic event display. Intensive trigger and DAQ tests allowed optimising the read-out electronics and control software. The first particles generated by injection tests in LHC have been recorded in the SPD in June 2008. Figure 3 shows an event display during a

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**Figure 1:** Simplified system block diagram.

**Figure 2:** Event display of a cosmic ray triggered by the pixel trigger.

**Figure 3:** Event display during an beam injection.
beam injection test in August 2008.

Great effort has been put into automatic control procedures. Upon each start of an acquisition run the SPD DCS verifies the proper configuration of the electronics and resets the system in order to avoid errors due to wrong manual configuration but also to clear processes and buffers left from a run not having been terminated properly.

In the meanwhile the SPD has taken thousands of self-triggered cosmic events for geometry alignment and provided a stable trigger signal to the other ALICE detectors. The system runs stable over months. The continuing effort is dedicated to automatisation, such as power-on and -off procedures and the automatic recognition of errors or trends which might lead to errors, allowing non-experts to operate the detector.

IV. SUMMARY

The SPD system development has been successfully terminated. The system is installed and operating stably. An overview of the design and commissioning process has been given. The implementation of the SPD system was a technological challenge. The commissioning results and the performance of the system show that this challenge has been appropriately met. The experience gained shows that early R&D work for sub elements and production of building blocks such as ASICs must go very closely together with the system development in order to optimize use of resources, performance and reliability.

V. REFERENCES


Installation, Commissioning and Performance of the CMS Electromagnetic Calorimeter Electronics

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Abstract

This contribution reviews the CMS high resolution electromagnetic calorimeter (ECAL) and its commissioning within CMS in situ.

I. CMS: A DETECTOR FOR LHC

The Compact Muon Solenoid (CMS) detector is a multi-purpose apparatus due to operate at the Large Hadron Collider (LHC) at CERN. LHC will yield head on collisions of two proton (ion) beams of 7 TeV (2.75 TeV per nucleon) each, with a design luminosity of \(10^{34} \text{cm}^{-2}\text{s}^{-1}\) (\(10^{27} \text{cm}^{-2}\text{s}^{-1}\)).

A complete description of the CMS detector can be found in [1]. Here we report a short summary.

The overall layout of CMS is shown in Fig. 1. At the heart of CMS sits a 13 m long, 6 m inner diameter, 4 T superconducting solenoid providing a large bending power (12 Tm) before the muon bending angle is measured by the muon system. The return field is large enough to saturate 1.5 m of iron, allowing 4 muon stations to be integrated to ensure robustness and full geometric coverage. Each muon station consists of several layers of aluminium drift tubes (DT) in the barrel region and cathode strip chambers (CSC) in the endcap region, complemented by resistive plate chambers (RPC).

The bore of the magnet coil is large enough to accommodate the inner tracker and the calorimetry inside. The tracking volume is given by a cylinder of 5.8 m length and 2.6 m diameter. In order to deal with high track multiplicities, CMS employs 10 layers of silicon microstrip detectors, which provide the required granularity and precision. In addition, 3 layers of silicon pixel detectors are placed close to the interaction region to improve the measurement of the impact parameter of charged particle tracks, as well as the position of secondary vertices. The electromagnetic calorimeter (ECAL) uses lead tungstate (\(PbWO_4\)) crystals with coverage in pseudorapidity up to \(|\eta| < 3.0\); ECAL is surrounded by a brass/scintillator sampling hadron calorimeter (HCAL) with the same coverage. HCAL is extended by an hadron forward calorimeter (HF) to cover up to \(|\eta| < 5.2\).

II. THE CMS ELECTROMAGNETIC CALORIMETER

The geometrical structure of ECAL is shown in Fig. 2. The barrel part of ECAL (EB) covers the pseudorapidity range \(|\eta| < 1.479\). The barrel granularity is 360 fold in \(\phi\) and (285) fold in \(\eta\), resulting in a total of 61 200 crystals. The crystals have a tapered shape, slightly varying with position in \(\eta\). They are mounted in a quasi projective geometry to avoid cracks aligned with particle trajectories, so that their axes make a small angle (3°) with respect to the vector from the nominal interaction vertex, in both the \(\phi\) and \(\eta\) projections. The crystal length is 230 mm corresponding to 25.8 radiation length. The barrel crystal volume is 8.14 m\(^3\) and the weight is 67.4 t.

The full barrel calorimeter is divided into 2 equal cylinders of radius 1.29 m. Each cylinder is made of 18 supermodules. A supermodule (SM), 1700 crystal, is divided along \(\eta\) into 4 different modules, each containing 400 or 500 crystals. Four modules, separated by aluminium conical webs 4 mm thick, are assembled in a SM.
The endcaps (EE) cover the rapidity range \(1.479 < |\eta| < 3.0\). The longitudinal distance between the interaction point and the endcap envelope is 315.4 cm; the endcap consists of identically shaped crystals grouped in mechanical units of 55 crystals (supercrystals, or SCs). Each endcap is divided into 2 halves, or Dees which holds 3662 crystals. The crystals and SCs are arranged in a rectangular \(x-y\) grid, Fig. 3, with the crystals pointing at a focus 1300 mm beyond the interaction point, giving off pointing angles ranging from 2 to 8 degrees. The endcaps crystal volume is 2.90 \(m^3\) and the weight is 24.0 t.

III. ECAL CONSTRUCTION AND INSTALLATION

The ECAL project spans many years and several hundreds collaborators. In September 2008 ECAL comprises about 200 PhD physicists.

The decision to use \(PbWO_4\) (instead of Cerium Fluoride) has been taken around the middle of September of 1994; TWEPP2008 marks almost exactly the 14th anniversary of that day. When the calorimeter material was finalized CMS was not yet officially existent: CMS had been proposed (Oct. 1992) but not approved yet (it happened on 31 Jan. 1996). The ECAL hardware procurement and construction phases lasted about 10 years. Crystals had been produced mostly in Russia, with a contribution of 1531 barrel crystals and 2593 endcap crystals from China; the a production rate has been about 10,000 crystals/year. Modules have been built in two construction sites, Casaccia INFN laboratories near Rome and CERN, and then assembled in SMs at CERN: the first SM (without electronics) was completed in 2002 and the last in 2007. Endcaps Dees had been built in 2007 and 2008.

IV. ANCILLARY SYSTEMS

The installation of a large system such as ECAL has as a prerequisite several ancillary subsystems such as cooling, ECAL safety system and the the detector control system (DCS).

The cooling system has a double duty: the first and most obvious one is to remove the heat produced by the electronics, estimated to be 180kW while the second task is to ensure temperature stability to the photodetectors (especially the APD in the barrel) and crystals since the number of scintillation photons emitted by the crystals and the amplification of the APD are both temperature dependent. In the barrel the total water flow has been set at 50 \(l/s\) (each SM has a flow of 1.39 \(l/s\)). A major task for the ECAL DCS is the monitoring of the crystals and APDs temperature and the verification that the required stability of \(\pm 0.05^\circ C\) of the is achieved.

The purpose of the ECAL Safety System (ESS) is to monitor the air temperature of the front end environment (expected to be around 25–30 C), the water leakage detection cable, which is routed inside the the detector and the proper functioning of the cooling system. ESS automatically perform pre defined safety actions and generate interlocks in case of any alarm situation. The read out system, with full built in redundancy, is independent of the DAQ and control links and based on a Programmable Logic Controller (PLC). In case of any critical reading hard-wired interlock signals are routed to the relevant crates in order to switch off the high voltage (HV) and low voltage (LV) and/or the cooling PLC in order to stop the water flow on a certain cooling line.

The commissioning of these subsystems has been done in parallel with the installation of the first ECAL SMs. This is of course not an ideal situation since the requirements needed for SMs installation, mostly stable conditions, are in opposition to the needs of debugging these ancillary subsystems (possibility to change temperature conditions, turning on and off the electronics, generation of interlocks).

V. ECAL COMMISSIONING

ECAL commissioning is a very broad term that indicates all necessary actions needed to make ECAL work. It is a job that proceeds in parallel with the installation phase and terminates much later, when all ECAL parts are ready to take data. The first SM was installed in CMS during the first quarter of 2007 and the endcaps were installed and commissioned in Summer-Fall 2008. ECAL commissioning can be divided into two large groups:

- Hardware Commissioning: on- and off- detector electronics, HV and LV systems, laser monitoring and fiber optics
links

• DAQ: necessary software to run ECAL

A. Hardware Commissioning

Fig. 4 shows a block diagram of the ECAL electronics. We indicate with the term on-detector electronics all components that are physically placed in the detector while the off-detector electronics is placed in the service cavern. On- and off-detector electronics are linked by a system of fiber optics with data and trigger information sent on different fibers:

• Data: 1 link per trigger tower

• Trigger: 1 link per trigger tower in the barrel and 5 links per trigger tower in the endcaps

The total capacity of the system is around 640Mb/s.

The on-detector electronics chain starts with a photodetectors (the case of the APD is shown) whose signal is shaped by a Multi Gain Pre Amplifier and digitized by 40 MHz ADC. To meet the dynamic range and precision requirements the MGPA has 3 gains (1, 6 and 12) and the ADC has 12 bits. Data are pipelined in the FE card where trigger primitives generation is performed. FE sends trigger words at 25 ns rate while data are transmitted on receipt of a Level 1 trigger. Overall the on-detector electronics comprises approximately 21,000 custom made boards, with an average power consumption of 2.3 W/ch for a total consumption of 180 kW.

The logic of the off-detector electronics is shown in Fig. 5. Four boards are needed to configure the electronics, read out the appropriate data and generate the trigger. The clock and control system (CCS) board distributes the clock, trigger and broadcast commands, the trigger concentration card (TCC) generates the trigger primitives and transmit them at each bunch crossing, the data concentration card (DCC) is responsible for collecting crystal data while the selective read out protocol (SRP) selects which trigger tower should be read out. Overall the off-detector electronics comprises 18 VME 9U and 1 VME 6U crates controlled by 28 crate mounted PCs. The commissioning of both on- and off-detector electronics is completed with only two voltage regulators non functioning correctly.

The HV and LV systems provide the necessary voltages to the photodetectors (APD in the barrel and VPT in the Endcap) and on-detector electronics. The HV system has a total of 1224 independent channels in the barrel and 8 independent channels in the endcaps; the LV system comprises a total of about 680 LV channels in the Barrel and about 150 LV channels for the Endcaps. The commissioning of these systems is also completed.

One of the most important issue for ECAL is how well we can track changes in crystal transparencies. Crystal transparency is affected by radiation damage in a way that depends on the dose-rate. It’s estimated that transparency will decrease by 1 or 2 per cent at low luminosity while at nominal luminosity it can oscillate as much as 10% within an LHC cycle at $\eta = 2.5$. The first laser monitoring system has been used in a 2001 test beam and since then it has been used successfully in many other test beams achieving a stability of 0.068%. The full system is now installed in CMS and tested.

B. DAQ Commissioning

DAQ commissioning deals with all aspects needed to run together the various sub parts of ECAL: trigger, selective readout protocol, laser, detector control units, condition and configuration databases, non event monitoring, run control, data quality monitor. In the following I will describe 3 examples: trigger, selective read out and laser.

Fig. 6 schematically shows a very powerful method used to commission the trigger system: the off line emulation of on line trigger decisions. During a global run, when the ECAL trigger
is active and its decisions are used to trigger CMS, the values used to calculate the trigger decisions are also recorded. Offline the trigger decisions are recalculated and compared with what was decided on line.

Figure 6: Trigger generation and emulation.

This method proved to be very important to spot hardware related problems (for example wrong cabling) and to tune trigger algorithms.

An important aspect of DAQ commissioning has been the implementation of the Selective Readout Protocol (SRP): when a trigger tower has energy over a given threshold (the actual value is programmable, we used values of the order of 0.5-1 GeV) the SRP flags for complete read out all towers around it, Fig. 7. This solution allows high interest regions to be read out without zero suppression.

Each colored square represents a trigger tower (TT) that has been read out and the color indicates the number of crystals read in that TT (red = 25 crystals, all of them).

Figure 7: A single event read out using the Selective Readout Protocol: groups of 3x3 trigger towers are read completely around the seed tower. The arrows point to two different high interest regions.

Another important milestone in ECAL commissioning has been the start up of the monitoring system. During normal operation ECAL acquires 3 types of non physics events: pedestal, test pulse for the electronics and laser shots. These monitoring events are acquired during the LHC abort gaps: the LHC filling scheme has an interval of 118 bunch crossing (118 * 25 ns = 2.95 µs) where there are no particles, the so called abort gap (which might be used to dump the beam). ECAL uses these gaps to take calibration data and it takes 35 minutes to run the full calibration sequence.

The calibration sequence is routinely used in CMS and calibration events are packed in special data streams which are then used to perform daily checks. The system works quite well even though not yet at the level required to handle such a high volume of data (40 Gb of laser data a day) over an extended period of time.

VI. ECAL STATUS

The electromagnetic calorimeter is now fully installed in CMS. Overall the system performs as expected, with noise levels compatible with expectations both in the barrel (pedestal RMS = 1.0 ADC count) and the endcaps (RMS = 1.9 ADC counts). We noticed that noise conditions are dependent upon the CMS geometrical configuration, with the minimum noise reached when CSM is fully closed.

The number of dead or problematic channels varies on a daily basis, some appear and some are fixed. It is difficult to provide a list which is valid beyond a couple of weeks; the most common problems are dead photodetectors, bad connections, broken front end electronics, some LV connections and some clock problems.

Overall we did not have time to deal in full with the list of problematic channels, more studies are needed which can be done only during the winter shutdown. It’s difficult to assess exactly the situation however it’s very exciting to see that less than 1% of the calorimeter has problems.

VII. RUNNING MODE

In the period when ECAL was commissioned not only all other CMS sub detectors were also facing similar challenges but CMS as a single experiment was commissioned. All these activities competed for resources and manpower so it was agreed to divide the week into local runs, where sub detectors were allowed to advance in their preparation, and global runs, when all sub detectors where supposed to join together in global runs.

A. CMS global runs

Global runs started early in 2007, first with only the data acquisition system itself, and then grew to include almost all CMS at the end of August 2008; Fig. 8 shows this evolution.

Figure 8: Evolution of CMS global run. 100 on the vertical scale mean total completion

The main goal of global runs is to exercise as many compo-
nents as possible and to establish protocols for stable running mode. CMS ran in global mode a few days each week and a full week every month to achieve particular milestones. In the period March-August CMS has logged more than 350 million cosmics triggers.

B. ECAL performance in Global Runs

ECAL is designed to measure energy depositions up to 1.5 TeV therefore it’s not optimized to detect the energy released by a cosmic ray (250 MeV). However, increasing the gain of the photodetectors (this is possible only in the barrel) from 50 to 200, it’s possible to clearly see a signal. Note that since cosmic muons are reaching ECAL with all possible angles there is not a real signal ‘peak’ but more a continuous shoulder. Cosmic muons can also deposit quite high energy clusters via catastrophic bremsstrahlung photon emission.

C. Beam Run

On September 10, 2008, LHC injected beam in the accelerator and in the following days CMS saw clear beam related signals. In particular, during the ring commissioning, LHC dumped on purpose the beam (a low intensity version of the real beam, $10^9$ protons at 450 GeV) several times on collimators placed 150 meters away from CMS creating a huge number of muons. We estimated that 2-300,000 muons reached ECAL at the same time dumping 300 TeV of energy: 98% of the crystals were lit up. Fig. 10 shows the energy deposition for one of these dumps.

These beam dump events have been also extensively used to check the timing of the read out, especially for the endcaps, since all crystals are hit at the same time.

VIII. CONCLUSIONS

It has been 14 years almost to the days of TWEPP2008 that the choice of $PbW\:O_4$ was made. ECAL is now ready to take data and we are sure that the next 14 years will bring exciting new insights.

REFERENCES

Installation and Commissioning of the ATLAS Liquid Argon Calorimeter
Read-Out Electronics

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Abstract
The cryostats of the ATLAS LAr calorimeter system are installed in the ATLAS cavern since several years. Following this, an effort to install and commission the front-end and back-end read-out electronics as well as the timing, trigger and control electronics (infrastructure, crates, and boards) has been ongoing and is finished now, in time for the cavern closure. Following cautious procedures and with continuous testing-campaigns of the electronics at each step of the installation advancement, the result is a fully commissioned calorimeter with its readout and a small number of non-functional channels. The paper will give a general overview of the installation and refurbishment campaign of the ATLAS LAr calorimeter electronics. Different problems observed and addressed will be discussed. It will describe noise studies that have been performed and shortly review the solutions implemented to reduce noise.

I. INTRODUCTION
The ATLAS experiment [1] at the LHC is a general purpose detector designed to exploit the full physics potential of the LHC at CERN. The collider will produce proton-proton collisions at a centre-of-mass energy of 14 TeV.

Liquid Argon (LAr) sampling calorimeters [2] are used in ATLAS for all electromagnetic calorimetry covering the pseudo rapidity interval \( \eta < 3.2 \), as well as for hadronic calorimetry from 1.4 to the acceptance limit of 4.8.

The LAr calorimeters consist of four sub-detectors and are contained within three cryostats as shown in figure 1. The central cryostat houses the electromagnetic barrel calorimeter (EMB), while each end-cap cryostat contains an end-cap electromagnetic calorimeter (EMEC), 2 hadronic end-cap wheels (HEC) and a 3 wheels forward calorimeter (FCAL). In total 182468 calorimeter cells are to be read out.

A choice of common electronics for all calorimeters standardizes the hardware to simplify the maintenance. The HEC nonetheless uses cold preamplifiers.

The main tasks for the readout electronics are:
- To measure, for triggered beam crossings, the energy deposit in each calorimeter cell to better than 0.25% at high energy. The dynamic energy range will cover a maximum of 3 TeV down to a lower limit of 10 MeV. The readout should proceed without any dead time up to a trigger rate of 75 kHz.
- To provide the trigger system with the energy deposited in trigger towers of size .1in pseudo rapidity ×.1in phi. The trigger processor combines the information from all ATLAS sub-detectors to deliver at the 40 MHz bunch crossing rate a yes/no decision to read out the detectors.

II. THE READOUT ELECTRONICS

A. Generalities
The readout architecture is sketched in figure 2. When a charged particle traverses and ionizes the liquid Argon in the gap between a LAr electrode and an absorber, an ionization current is measured on the read out cells of the electrodes due to the drift of electrons. The pulse height is proportional to the energy deposit of the particle.

The analog signal is received, pipelined and digitized by the front-end boards (FEB) mounted directly on the detector. The FEBs send the digitized pulse via optical links to the Read Out Drivers (ROD) which are installed in a radiation-free area (USA15) next to the detector cavern (UX15).

Summation of the analog signals is also formed, mostly in the FEBs or in the Tower Builder Boards (TBB) or Tower Driver Boards (TDB) for the HEC, but also in some cases in the receiver system (barrel-EC transition region and FCAL) to build primitives which are sent to the L1 trigger interface to be treated by the Level-1 calorimeter processor.

Each ROD receives the data from up to 8 FEBs and processes the signals of up to 1024 detector cells (128 cells per FEB). For each cell, it will calculate the energy deposited but also the time of the deposition and a quality factor for cell with a high energy deposit, using an optimal filtering algorithm [3]. The ROD sends these results and sometimes

Figure 1: The LAr calorimeters in their cryostats.
also the raw data through 4 optical links housed on a Transition Module (TM) at the back of the ROD, the S-links, to the Read Out Buffers (ROBs) hosted on PCs (ROS).

The LAr readout elements need the bunch-crossing signal (40.08 MHz BC clock) from the LHC machine and the Level-1 accept signal (L1A) from the trigger system. In addition, to synchronize all the readout elements, the LHC provides once per turn the Bunch Counter Reset signal (BCR) used to reset the Bunch Counter Identifier (BCID) in each readout element at a fixed time within the LHC cycle. The Timing, Trigger, and Control (TTC) system distributes these signals to both front-end and ROD system electronic via optical fibers.

B. The Front-End electronics

As was shown in figure 2, the FE system [4] includes front-end boards (FEB) which perform the amplification, shaping, sampling, storage, digitization, and readout of the calorimeter signals. Calibration boards inject precision calibration signals, and Tower Builder Boards and Tower Driver Boards produce analog sums for the L1 trigger. The various boards in the front-end crate (FEC) require the TTC signals for proper operation. In addition, most of the boards need to be configured and monitored. A custom serial link known as SPAC (Serial Protocol for the ATLAS Calorimeters) is used for this purpose. Controller boards (CONT) installed in the FECs are used to receive and distribute the TTC and SPAC signals to the various FE boards.

These boards are housed in 58 front-end crates which are divided in 2 half front-end crates (HFEC) in terms of functionality (FCAL has 2 HFEC but in 2 different crates).

The total number of boards and their distribution on the LAr detectors is summarized in table 1

<table>
<thead>
<tr>
<th>HFEC Type</th>
<th>HFEC</th>
<th>FEB CALIB</th>
<th>CONT</th>
<th>TBB</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>EMB</td>
<td>64</td>
<td>896</td>
<td>64</td>
<td>64</td>
<td>-</td>
</tr>
<tr>
<td>EMEC Standard</td>
<td>32</td>
<td>416</td>
<td>32</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>EMEC Special</td>
<td>8</td>
<td>136</td>
<td>16</td>
<td>16</td>
<td>24</td>
</tr>
<tr>
<td>HEC</td>
<td>8</td>
<td>48</td>
<td>8</td>
<td>8</td>
<td>- 16</td>
</tr>
<tr>
<td>FCAL</td>
<td>2</td>
<td>28</td>
<td>2</td>
<td>2</td>
<td>- 4</td>
</tr>
<tr>
<td>Total</td>
<td>114</td>
<td>1524</td>
<td>122</td>
<td>122</td>
<td>120</td>
</tr>
</tbody>
</table>

The low voltage power required by the FE electronics is delivered by a low voltage power and distribution system made of 58 identical partitions. AC-DC primary power supplies (PS), fed from the 400 VAC three-phase network in the ATLAS pit and organized in racks in USA15, deliver 280 VDC and 10-11 A to low voltage power supplies (LVPS) made of DCDC converters mounted on the detector adjacent to the corresponding FEC.

For each of the 128 detector cells of a FEB, the signal is first subject to several stages of analog processing. Preamplifier hybrids amplify the raw signals, which are then split and further amplified by shaper chips to produce three overlapping linear gain scales, with gain ratios of ≈ 10. Each signal is subject to a fast bipolar CR-(RC)^2 shaping function.

The shaped signals are then sampled at the LHC bunch crossing frequency of 40 MHz and stored by switched capacitor array (SCA) analog pipeline chips, which store the signals in analog form during the L1 trigger latency.

For events accepted by the L1 trigger, typically five samples per channel for physics but up to 32 for commissioning, are read out from the SCA using the optimal gain scale, and digitized using a 5 MHz 12-bit Analog-to-Digital Converter (ADC) common for 8 channels. The digitized data are formatted, multiplexed, serialized, and then transmitted optically out of the detector to the Readout Driver (ROD) in USA15 via a single 1.6 Gbps optical link per FEB.

C. The Back-End electronics

The BE electronics [5] is composed of three systems: the ROD which is the core of the BE, the TTC and the Level-1 receiver.

1) The ROD system

As can be seen in figure 2, the ROD system includes ROD boards to calculate the energy, time and quality factor from the digitized samples sent by the FEBs, TM boards housing the S-links, SPAC Master boards to control and monitor the HFECs and a TBM board to receive the TTC optical information and distribute it electrically to the ROD boards in the crate. It also collects the RODs busy signals in the crate and sends the OR of them to the TTC system.

These boards are housed in 16 9u VME64x crates each controlled by a VME Processor.

The system has been split in 6 partitions each corresponding to a slice of the LAr detectors.
Table 2 summarizes the number of crates and boards for each of the partitions.

<table>
<thead>
<tr>
<th>Partition</th>
<th>Crate</th>
<th>ROD</th>
<th>TM</th>
<th>SPAC M.</th>
<th>TBM</th>
<th>CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>EMB-A</td>
<td>4</td>
<td>56</td>
<td>56</td>
<td>8</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>EMB-C</td>
<td>4</td>
<td>56</td>
<td>56</td>
<td>8</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>EMEC-A</td>
<td>3</td>
<td>35</td>
<td>35</td>
<td>6</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>EMEC-C</td>
<td>3</td>
<td>35</td>
<td>35</td>
<td>6</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>FCAL/HEC-A</td>
<td>1</td>
<td>5</td>
<td>5</td>
<td>2</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>FCAL/HEC-C</td>
<td>1</td>
<td>5</td>
<td>5</td>
<td>2</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>Total</td>
<td>16</td>
<td>192</td>
<td>192</td>
<td>32</td>
<td>16</td>
<td>16</td>
</tr>
</tbody>
</table>

The ROD board receives the TTC signals and has 8 DSPs for doing the calculation on the data received from the 8 FEBs (1 per FEB). For each event accepted by the Level-1 trigger (L1A), it will generate the corresponding BCID and L1ID. It will also directly receive from the TTC system the Trigger type and transmit them to the 8 DSPs. For each event the DSP will match the data coming from the FEB with the TTC information (BCID), calculate the energy, and if needed the time and quality factor for each of the 128 cells from the 3 to 32 samples received. The results of the calculation and also raw data (above a configurable threshold per cell, the raw data will be written out as well) of 2 DSPs will then be merged and sent to the TM to be output on one of the 4 optical links, the S-links, to the Read Out Buffers (ROBs). The reception, matching calculation and transmission must be done within 12 microseconds which is the average time available for a mean L1A rate of 75 KHz. If the DSP cannot accept anymore events, it will set a busy signal to pace the Level-1 trigger.

2) The Timing, Trigger and Control system

The Timing Trigger and Control (TTC) system distributes the different timing and control signals to both front-end and ROD system electronics via optical fibers. This includes the LHC clock (BC), the L1A, the BCR and Event Counter Reset (ECR), the Trigger type as well as more specific command to some modules like the calibration command for example.

The 6 LAr detector partitions each have their own TTC system using a Local Trigger Processor (LTP) in order to run independently when needed. They are housed in 3 6U VME64x crates. Each crate houses 2 partitions covering the same type of detector (Barrel, EMEC, FCAL/HEC) which can be run together under the control of 1 LTPs acting as a master, the other as a slave. On top of that a structure housed in a 4th crate with a special LTP and 4 Local Trigger Processor Interfaces (LTPi) allows all or some of the partitions to be run either under the control of the Central Trigger Processor (CTP), the special LTP or other subsystems (Tiles Barrel Hadronic Calorimeter and Level1 calorimeter Trigger).

Within a partition, The ROD Busy module (RODB) collects the busy from the different ROD crates and transmits a partition busy to the LTP to pace the level-1 trigger generation. When in master mode, the LTP generates all the timing, trigger and control signals, while in other modes it gets the signals from higher in the chain. They are then encoded in the TTCvi and sent on optical links by the TTCex. Optical couplers 1 to 32 (OC32) or 1 to 16 (OC16) provide the necessary optical fan out. For the 6 partitions a total of 212 fibers are connected to the front-end (2 per HFEC, 1 being a spare) and 16 fibers to the ROD electronics. Table 3 summarizes the number of elements for each partition and the control structure.

<table>
<thead>
<tr>
<th>Partition</th>
<th>RODBLTPiLTPiTTCCvOC16OC32</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>-</td>
</tr>
<tr>
<td>EMB-A</td>
<td>1 - 1 - 1 -</td>
</tr>
<tr>
<td>EMB-C</td>
<td>1 - 1 - 1 -</td>
</tr>
<tr>
<td>EMEC-A</td>
<td>1 - 1 - 1 -</td>
</tr>
<tr>
<td>EMEC-C</td>
<td>1 - 1 - 1 -</td>
</tr>
<tr>
<td>FCAL/HEC-A</td>
<td>1 - 1 - 1 -</td>
</tr>
<tr>
<td>FCAL/HEC-C</td>
<td>1 - 1 - 1 -</td>
</tr>
<tr>
<td>Total</td>
<td>6 4 7 6 6 4 6</td>
</tr>
</tbody>
</table>

3) The Level-1 receiver system

The Level-1 receiver system is not described in this paper.

III. THE HV SYSTEM

The HV system provides the drift voltage across the LAr gaps in the calorimeters between electrodes and absorbers. The LAr calorimeter cells are connected to about 4700 HV supply groups, distributed roughly equally among each of the three cryostats. Each of this group is connected to a single HV channel. A total of 157 commercial 32-channel HVPS modules are used, mounted eight to a subrack in 20 subracks. A summary of the HV module count with channel parameters is listed in table 4.

<table>
<thead>
<tr>
<th>Detector</th>
<th>Operating Voltage (V)</th>
<th>Max. Current (mA)</th>
<th>Nb. of 32-Channel Modules</th>
</tr>
</thead>
<tbody>
<tr>
<td>EMB</td>
<td>2000</td>
<td>75</td>
<td>53</td>
</tr>
<tr>
<td>EMEC</td>
<td>1000 to 2500</td>
<td>200</td>
<td>56</td>
</tr>
<tr>
<td>HEC</td>
<td>1800</td>
<td>75</td>
<td>32</td>
</tr>
<tr>
<td>FCAL purity</td>
<td>2500</td>
<td>6000</td>
<td>14</td>
</tr>
<tr>
<td>detectors</td>
<td>2500</td>
<td>75</td>
<td>2</td>
</tr>
</tbody>
</table>

IV. INSTALLATION AND COMMISSIONING EXPERIENCE

A. Generalities

The procedure was to install hardware and test it as soon as possible in a stand alone mode. Then to leave it running, integrate it and use it as much as possible.

Electronics for the front-end was installed and tested one crate at a time with stand-alone tests including pedestal and calibration runs using dedicated acquisition systems.

Electronics for the back-end was installed one crate at a time with a specific injector system to replace the FEBs and a FILAR based readout
system to replace the ROBs, which were not yet connected. TTC signals were provided by the final TTC system.

As soon as these elements were tested and interconnected, they were integrated into the global acquisition system.

Since then the detector has been commissioned continuously with the available readout system doing pedestal, calibration and cosmic runs to verify its behaviour and stability.

B. The Front-End electronics

Installation of the front-end electronic started in summer 2005 for the barrel and in May and August 2006 for the end-caps respectively. All the crates for the Barrel had been tested in September 2006 and December 2006 for the end-caps, but the complete set of power supplies after refurbishment were only available in August 2007. The FEB also needed refurbishment and this was accomplished between July 2007 and March 2008 for the Barrel, end-cap C and end-cap A.

The first time we could read the full LAr detector was in May 2008, a short time before the closure of the apparatus.

Tests of the FE crates were done with 2 stand alone read-out systems located in USA15: One for the barrel and the other for the end-caps. In both cases a LVPS was moved from crate to crate together with a cable made of 48 fibres between UX15 and USA15. As there was no cooling infrastructure for the barrel, the FEBs had to be tested one at a time. For the end-caps a standalone cooling system was used and a full FE crate was tested in a single pass using a read-out with 4 ROBs and standard TDAQ software. Pedestal runs and calibration runs were sufficient to show all defects like bad shapers, damaged calibration lines, dead FEB channels...

All FEBs had to be refurbished, initially because a mistake had been found in the level adaptation of 2 signals between different ASIC technologies. There was an increased risk of long term failure for these components. This was a good occasion to correct another problem which had been apparent only on some boards. Some shapers had their timing constant changing over time due to uncertain disconnection of a resistance network used to precisely set this time constant. This network was adjusted at the time of testing of the chips by burning fuses on the IC which turned out to suffer from partial reconnection over time. By cutting the pins corresponding to the burnt fuses for each shaper, this problem was definitively solved. As a further surprise, when getting the boards out, corrosion was found on some boards. This was due to a bad cleaning process after repair of some boards during production tests. About 50 boards were damaged beyond repair while the others could be recovered after a new cleaning. A new batch of 40 boards is being produced for spare.

The LVPS have been plagued by failures right from the beginning. In summer 2006 a task force was setup to do a deep review of the LVPS. It led to many modifications and component replacements in the design in order to use them for the first years of LHC operation. All LVPS were refurbished between spring and August 2007. All have been working since, though one has lost its redundancy. Following the review, a backup project has started with 2 companies to produce new designs and prototypes, as the reliability of the refurbished power supplies cannot be guaranteed for the lifetime of the LHC operations. In June 2008, when the barrel toroid was turned on for the first time, it was observed that the induced magnetic field was too high in some positions of the end-caps LVPS. An important effort with measures and simulations showed that the installed shielding was not sufficiently covering the magnetically sensitive LVPS. New shielding plates were manufactured and installed in very tight and hardly accessible positions.

C. The Back-End electronics

Installation and tests of the back-end electronics started in August 2005 and were finished in April 2007 for the ROBs and in June 2007 for the fibre connections to the ROBs.

The injector system used for the tests consists of 6 9U VME 64x modules with 5 outputs each. 1 to 2 optical splitters on each output provide a total of 60 FEBs equivalent output needed to test half a ROD crate. The readout of the ROBs was done by 3 ROS PCs equipped with 7 FILAR boards providing the 28 readout inputs needed. The Injector generates data with the same format as the FEB when receiving L1A. A comparison of the injected data with the read-out data is done to validate the half crate.

Front-end fibres were then connected when available, followed by the fibres to the ROBs. Final commissioning using FEBs and ROBs could then start. This commissioning has been going on since June 2007 until the first beam.

The major problem encountered was the commissioning of a full ROD crate using FEBs and ROBs with a high L1A rate (>40 KHz) and transferring the raw data. In this mode, transfers on all ROD modules within the crate are almost synchronous, paced by the busy of the system. This generated huge current surges on the 3.3 V power supply which is connected to the crate through a 1 meter long cable. It produced a voltage oscillation which triggered the overvoltage protection circuit of the power supply and shut it down. A solution was found by doubling the cable in order to reduce the inductance and by adding a big 3.3 mF capacitor on each of the ROD boards to have a better current reservoir.

With these modifications, in the same conditions, the current surge was reduced from 30 A to less than 10 A and the voltage oscillation from 300mV to 50 mV. We haven’t seen any problem since these modifications, whatever the conditions of operation.

D. The Timing Trigger and Control

Installation of the TTC system in USA15 started in September 05 as soon as the rack infrastructure was available. It was completed in November of the same year except for the control structure (LTPIs) which was added in May 2008.

The TTC system was first connected to the ROD system electronics and used for the ROD system commissioning. Connection to the front-end electronics was finished in August 2007 allowing commissioning tests with both front-end electronic and ROD system.

There was never a specific commissioning of the TTC system. Rather functionalities were progressively used and tested when needed for the commissioning of the detectors.
Problems were only discovered when we started to use the system at high speed in long term tests in fall 2007.

The first problem to observe and understand was that a L1A could occasionally go through when the Busy was present. This was tracked down to a fault in the ROD Busy module. A glitch of a few ns could be observed on the TTL open collector output of the Busy when there was a VME access to the status of this module. It was large enough for the LTP to be able to produce a L1A if it happened at the wrong time. The cure was to use the NIM output which filters this glitch in the conversion from TTL to NIM.

The second problem was related to a few corrupted events received from the FEBs by the RODs in long runs (days) and at high rate L1A. This problem took 6 months to understand as it implied a very complex mechanism.

VME accesses to the status register of the LTP can provoke a very small glitch on the clock output of the LTP (1-2ns) when at the same time there is a transition on the LTP internal orbit signal and the internal LTP clock has a different logic level than the incoming CTP clock. This glitch should not have any effect as it should be filtered by the PLL in the TTCex. But this glitch, when present at the input of the Analog Device TTCex phase comparator of the PLL, stops it for 350 microseconds. This is an unexpected behaviour that the manufacturer has not been able to explain. As a consequence the TTCex output clock starts shifting in order to recover the lock process which takes a few milliseconds. This provokes a corruption of the data sent by the FEBs on the link and at a later stage an unlock of the QPLL in the FEBs which then needs a further 400 milliseconds to recover. During all that time data can be more or less corrupted as the FEB and ROD clock is shifting permanently.

The clock glitch was suppressed with a new version of firmware for the LTP. The TTCex was not modified as the correction proposed by Analog Device has not shown any improvement.

V. NOISE RELATED ISSUES

Noise correlated to the Tile Hadronic calorimeter power supplies with a frequency peak at 17 MHz had been observed when operating a large fraction of their system. The noise was entering the LAr system by the feed-through heater cables and by capacitive coupling affected channels on the nearby cables in the FEC supports on the cryostats. These heater cables were equipped with filters efficient only up to 10 MHz. Additional filter boxes have been added. Tile power supplies have also been modified to incorporate additional output filters.

Noise bursts have been observed in cosmic and pedestal runs. It was originally identified with the help of the so called OddCellMonitoring software tool. The original pedestal of each channel or cell have been measured and recorded. With a perfect Gaussian noise distribution (width of $\sigma$ noise) we would expect about 0.27% of the cells to be over 3 $\sigma$ noise away from the pedestal in a given event. If a certain channel is more often above this threshold, it is easily identified. Looking at the L1 interface output with a spectrum analyser where many cells are added, we see noise peaks in the range 3.5 to 6 MHz. Looking at the signal with a scope we could see the noise increasing with a periodicity of 250 microseconds.

The source of this noise was not identified but the path to get into the LAr detector was shown to be via coupling between the outer shield of the HV cables and the internal cables. In order to avoid grounding loops between the detector and the back-end electronics very strict grounding rules have been agreed upon and implemented. The shield of the HV cables was only connected on one end (USA15). This noise was suppressed by adding a 1 microfarad capacitor between the outer shield of each HV cable and the cryostat. This was done at the level of each HV filter box located on the cryostat.

VI. CONCLUSION

The back-end electronics is now fully commissioned and operational with no dead channel as it is easily accessible in case of failure.

The front-end electronics which is now not accessible is also commissioned and operational, with a few dead elements. Recently, one 1/8th of the HEC calorimeter could not be readout due to the failure of a power supply for the cold preamplifiers. Also 7 FEBs out of a total of 1524 are not transmitting their data to the BE but are operational for the trigger. These problems will be fixed during the next shutdown.

The detector has 100% of its HV channels working with about 6% of them operated at a reduced voltage but still producing a usable signal. 0.5% data channels have minor problems like increased noise or damaged calibration lines.

The readout system is now very stable. Cosmic data has been taken over the last 2 years together with other ATLAS sub-detectors. The calibration constants which have been monitored over a few months are stable at better than 0.1%. The ATLAS LAr system is ready to record the first LHC beam events.

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WEDNESDAY 17 SEPTEMBER 2008

PARALLEL SESSION A5
INSTALLATION & COMMISSIONING
The LHCb Silicon Tracker: lessons learned (so far)

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Abstract

The LHCb Silicon Tracker is part of the main tracking system of the LHCb detector. It covers the full acceptance of the experiment in the Tracker Turicensis (TT) in front of the dipole magnet and the innermost part in the three Inner Tracker (IT) stations downstream of the magnet. We report on final elements of the production, the installation and commissioning process in the experiment. Focusing on electronic and hardware issues we describe the lessons learned and the pitfalls encountered. First experience of detector operation is presented.

I. OVERVIEW

The Silicon Tracker of the LHCb experiment [2] consists of silicon strip detectors with a pitch of around 200 μm. For the TT station upstream of the magnet, a 500 μm thick sensor with 512 strips is used, while the three IT stations after the magnet feature 320 and 410 μm thick sensors of 384 strips each. This adds up to 143k readout channels for the TT station and 129k channels for IT. The signals are amplified and processed by the Beetle readout chip [3], which transmits its data via differential analogue lines to the Service Boxes. The Service Boxes are located outside the acceptance of the tracking system to minimize the amount of dead material. For the TT station, they are mounted to the upstream face of the LHCb dipole magnet while the IT Service Boxes are fixed to the lower end of the support frames of each tracking station. Digitizer Boards inside these boxes digitize and convert the analogue signals into optical signals which are transmitted via fiber of up to 120 m length to the counting house [4].

II. SILICON SENSOR MODULES

A. Conductive (Silver) glue

Conductive glue was used to connect the grounding of the TT readout hybrid to the cooling block of the sensor module and for the connection of the biasing voltage on the back side of each silicon sensor. While initial testing showed a good connection, older prototypes suffered from high glue resistances. The reason is due to the inability of the silver glue to stop the oxidization for the underlying aluminium [5]. In addition the grounding of the readout hybrid suffered from thermal cycling (Fig. 2). It was therefore decided to change the connection procedure for these locations. The grounding of the readout hybrids was changed to a screwed solder lug. As no soldering is possible on the back side of a silicon sensor, the bias lines of the Kapton supply cables were bonded to the sensor followed by a glob-top seal to protect the bond wires.

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1 for a complete list of authors see [1]
B. 4th channel problem

A problem that was discovered very recently concerns the wire bonds at the inputs of the Beetle front-end chips. As shown in Fig. 3, these are executed in four bond-rows to match the four-fold staggered input pads of the Beetle. A few weeks after the installation of the detector modules in the experiment it was found on six out of the 280 installed readout hybrids that a significant number of bonds in the inner-most of these bond rows were broken. Nothing similar had ever been observed in the extensive burn-in tests that each module had to pass during its construction and that were designed to reproduce conditions in the experiment as closely as possible. As of now, we have no explanation for this effect, investigations are ongoing.

III. CABLE CONNECTIONS

The Beetle readout chips amplify the signals from the silicon sensors and transmit the analogue signals upon a Level-0 trigger to the Service Boxes. This transmission is done via electrical cables. For the TT station, the first 70 cm are done via flexible Kapton cables to minimize the cross section which has to be routed through the thermal isolation of the detector box. Directly outside of the cold volume, the Kapton cables are then connected via small patch panels to 8 m long multi-conductor round cables. These cables then connect to the Service Boxes which are located at the magnet return yoke outside the tracking volume.

A. High density connectors

Each readout hybrid requires a single cable connection only, where all necessary supplies and signals are provided. An 80-pin high-density connector was chosen which connects on the Beetle readout hybrid inside the cold volume and to small patch panels outside. Due to the mechanical layout, the inner ends of the cables are guided by small gaps in the main cooling plate. Therefore no torque applies to this mating interface. As space is very limited on the outside between the feedthrough and the patchpanels, the cables had to be bent in tight radii to be mated to the patch panels. The resulting torque led in several cases to unreliable electrical connection between mated high-density connectors. To ensure a mechanical fix of this mating, milled aluminium clamps were designed which could be applied to the patch panel stack and improved the connection (Fig. 5).

B. Kapton cable cracks

Another result of the required tight radii were cases of hairline cracks on the boundary of the rigid soldered pins of the high density connectors to the thin signal traces on the flexible Kapton cable. This is a well known problem and could have been avoided by a rigid support under the solder joints together with a gradual thinning of signal traces to avoid width discontinuities. Due to the small trace width and the flexible Kapton substrate, the only repair option is to replace an affected cable. As no mechanical movement is involved after installation, no system-wide replacement of this cable type is currently foreseen.

IV. ELECTRONIC DESIGN ISSUES

The following section describes problems with electronic design issues. These problems are located on the Digitizer Board, which digitizes the analogue signal and serializes the data for optical transmission, as well as on the backplane which provides power, timing and control signals to the Digitizer Boards.

A. Fast ADC bandwidth

In early laboratory tests, a non-flat noise distribution within a analogue readout frame was discovered. As this distribution was persistent even without any attached readout chip, it was traced back to have its origin inside the Digitizer Board itself.
In addition to the sampling rate, any ADC has a specified analogue bandwidth. Usually, this bandwidth exceeds the sampling rate to enable ‘undersampling’, i.e. to digitize a signal with a frequency larger than the sampling rate. To limit the amount of noise at the input of an ADC, a lowpass filter with a properly dimensioned cutoff frequency has to be used. While an early datasheet of the used ADC cited an analogue bandwidth of 100 MHz [6], an updated version listed a bandwidth of 1000 MHz [7]. Tests have shown that a 70 MHz lowpass, which could be easily added to the existing layout, was sufficient to restore the required flat noise distribution (Fig. 6). This lowpass filter was fitted to all Digitizer Boards prior to installation in the detector.

B. VCSEL mounting

The Digitizer Board design uses the CERN GOL chip [8] to encode the digitized physics data into a serialized bitstream. To make use of the internal laser driver of the GOL, single VCSEL diodes were mounted directly next to each GOL chip. These VCSEL diodes are glued into a metal receptacle with threaded holes to provide mechanical fixation to the printed circuit board as well as optical alignment with an attached fiber (Fig. 7).

During reception tests of the production Digitizer Boards, 30 % of the VCSEL diodes were determined to be outside of the optical power specifications. Tests performed by the vendor confirmed a misalignment of the VCSEL diodes inside the metal receptacle. This problem was traced to the soldering procedure of the diodes, which were wave soldered. As the diodes were already fixed to the board via their screws, a large amount of heat was transferred through them into the receptacle which led to the weakening of the glue holding the diode in alignment. As the preproduction boards were hand-soldered, this problem did not show up during the first batch of boards. A repair of these diodes was not possible and therefore all boards had to be screened and the defective diodes were individually replaced.

C. Slow control ADC

Each Beetle readout hybrid features a PT1000 resistive thermometer, which can be read out by its associated Digitizer Board. This is done via a DCUF slow control ADC [9]. After installation of the Service Boxes in the detector, all ADC readouts showed an oscillating odd-even behaviour (Fig. 8).

The source of this behaviour was determined to be an overvoltage condition on one of the other ADC input channels. An incorrectly dimensioned resistive divider resulted in an input voltage of 3.8 V, which is beyond specifications for a 2.5 V powered ADC. Once this resistive divider was corrected the DCUF readout worked as designed. The change of dividers has only been done for some Digitizer Boards corresponding to selected locations in the detector as this problem was understood only very late in the commissioning process. As these are non-critical readings, the dividers will be changed over time during normal maintenance and board replacements.

D. Pressfit Connectors

Another problem encountered during commissioning in the experiment involved the used ‘Pressfit’ mounting procedure for the backplane connectors. Being an industrial standard for solderless connector mounting, it was initially believed to be adequate for use in the Service Box backplanes. In this through-hole technology variant, the board holes are tightly specified to provide an electrical and mechanical contact to a socket pin which implements a spring-like design. However some protruding pin tips got bent during delivery of the backplanes which compromised the spring tension and resulted in electrical contact failure. Finally, suspicious
contacts were resoldered manually to ensure a proper mechanical and electrical contact.

E. Voltage regulators

After installation in the detector, immediate commissioning tests for the electronics systems started. It was however determined that for some readout sections no programming of the frontend chips was possible. Other frontend chips could be programmed but failed to generate increased noise in the readout chain indicating a working preamplifier with sensor capacitance attached. This behaviour was caused by a failure of radiation tolerant low-voltage regulators [10] (either digital or analogue supply line) which consequently had to be replaced. Although the failure mechanism is still under investigation, it is likely related to the impedance of the 8 m long cables, which connect the Service Boxes including the regulators to the readout hybrids. Being already installed in the detector, these cables were not part of final burn-in tests of the complete Service Boxes, where such a problem would have been easily spotted. Interestingly, the regulators also signalled an overcurrent condition on their respective monitoring pin, despite the current being only 30% of the maximum rated current.

F. Power line oscillations

During first trials with the maximum trigger rate of 1.1 MHz, several Service Boxes on the Cryo side of the TT subdetector reduced their current consumption by about 10%. This reduced current was still present when stopping triggers again. The only way of restoring the current to standard levels was a complete shutdown of the low-voltage supply followed by a restart. This effect was not seen on either the Access side of the TT subdetector nor in the complete IT subdetector. The final source for this behaviour was later determined to be large (> 2 Vpp) voltage oscillations on the low voltage supply line between the MARATON power supplies [11] and the Service Boxes. Also here it is suspected that the problem is due to the long cables of about 30 m of length, which connect the supplies to the Service Boxes on the Cryo side of the detector. This behaviour was much less pronounced for the Access side of the detector, where power supply cables are about half the length.

Being restricted in volume and board area, only ceramic capacitors were included on the input voltage bus in the Service Box backplanes adding up to about 40 µF of total capacitance. A possibility to suppress the oscillations is to shift the accumulated phase shift of the regulation loop away from a multiple of $2\pi$, which was done by adding 1000 µF electrolytic capacitors externally to each Service Box. Various load tests confirmed the stability of the regulation loop in this configuration, which was eventually extended to the complete TT subdetector.

V. CURRENT STATUS

Both the TT and IT subdetectors were commissioned during spring and summer 2008. Due to the limited accessibility of the IT subdetector, repairs or exchanges of defective units were delayed until the winter shutdown. Currently, 98% of the detector is ready for taking physics data. Being much more accessible, repairs for the TT subdetector were possible until a very late stage resulting in a detector being 99% ready for datataking. These numbers are expected to improve further during the 2008/2009 winter shutdown.

During the LHC injection tests in August 2008, a large amount of data could be recorded for both subdetectors which resulted in initial timing settings and determination of signal-to-noise ratios (Figures 9+10). All results agree with data taken during beam tests in the design phase of the Silicon Tracker development.
Preliminary tests looking at the first beam-related data taken during LHC injection tests look promising. Although the occupancy in these events is high, it was possible to find correlations between tracks extrapolated from the VELO and hits in the TT. The observed width of the peak of around 500 µm is compatible with the angular resolution claimed for VELO tracks. Similar correlations have been observed for the IT.

![Residual distribution of extrapolated VELO tracks for the TT station.](image)

**Figure 10:** Residual distribution of extrapolated VELO tracks for the TT station.

VI. CONCLUSION AND OUTLOOK

Despite numerous iterations and reviews, several errors were introduced in the design of the LHCb Silicon Tracker. Additional problems were seen later at the system level, after full assembly of the TT/IT components and integration into LHCb. Some of these were simple design mistakes whilst others were the result of underestimating the technical complexity of the chosen approach. Due to time constraints no full system test was made in a beam test. Some of the problems certainly would have been uncovered by such a test.

We believe that only an open sharing of lessons learned can prevent similar mistakes to be done in future developments. Due to the methodical approach and a huge effort by the whole Silicon Tracker collaboration, the Silicon Tracker was completed in time for taking data together with the LHCb detector.

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ATLAS SCT Commissioning – TWEPP-08

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Abstract

The Barrel and Endcaps of the ATLAS SemiConductor Tracker have been installed in the ATLAS cavern since summer 2007. All the electrical and optical services were connected and rapid tests performed to verify their continuity. Problems with the cooling circuits, meant that the time for detailed tests in 2007 was limited. These problems have now been resolved allowing the SCT to be operated and participate in combined ATLAS Cosmic ray data taking runs. The results of these runs have been used to determine the hit efficiency of the modules as well as providing invaluable constraints for the detector alignment.

I. INTRODUCTION

One of the largest and most carefully designed particle detectors of our time is the ATLAS detector \cite{1}. Every 25 ns at the LHC \cite{2} a proton-proton interaction will occur, with a centre of mass energy of 14 TeV. Momentum and vertex resolution requirements are of key importance throughout the experiment, hence meticulous measurements are needed. The inner detector (ID) \cite{1} is housed within the central solenoid which provides a magnetic field of 2T to the ID. A detailed system of different types of detectors are necessary in order to accommodate the large density of tracks anticipated at the LHC. There are three sub-systems associated with the ID: Pixels, Semi-Conductor Tracker (SCT) and the Transition Radiation Tracker (TRT). Figure 1 shows a schematic of the ID, with specifics given for the SCT. The details of the silicon tracker will now be discussed.

A. Silicon Tracker Design and Layout

The Semi-Conductor Tracker is positioned as the second closest to the point of interaction. It comprises 4 central barrels and two end-caps, each with nine discs. The basic element of the system is the module. The SCT itself occupies a radial region between 25 and 50 cm. Its design provides 4 space point measurements for a particle originating from the interaction point, up to a pseudo-rapidity coverage of $\eta \geq 2.5$. In total the SCT has an active silicon area of 61 m$^2$. Silicon micro-strip technology provides fine granularity, which in turn, is central to the momentum, impact parameter and vertex position measurements.

B. Module Design and Operation

There are 4088 modules, equating to 15912 silicon strip wafers in the SCT. The barrel section has 2112 modules with only one module type \cite{3}, whilst each end-cap has nine discs populated with trapezoidal modules \cite{4}. A detector module consists of gluing two pairs of single sided sensors, back to back on a highly thermally conducting substrate. There is a small stereo angle of 40 mrad between each side. Each end-cap has four module types Outer, Short Middle, Middle and Inner containing a combination of five wafer types. Each sensor is read out by Application Specific Integrated Circuits (ASICs) \cite{6}, incorporated on the detector module itself. They consist of a front-end amplifier and discriminator and a binary pipeline to store the hits. Each module side is served by 6 of these chips, each one responsible for 128 read-out channels.

A particle traversing the detector induces a current in a strip. The generated current signal is amplified and a voltage output fed into the main amplifier known as the shaper. It provides the pulse shaping according to the timing requirements and it filters the noise in order to maximise the signal to noise ratio, S/N. It detects the presence of a signal when the amplitude is above a pre-defined threshold. When the signal is above this threshold, a 1 is registered and when it is below a 0 is returned. In this way, hit or no hit information is provided and is stored for each of the 128 channels of the chip.

It is extremely important that the charge induced on the aluminium strips is understood. Attention must be given when setting the threshold such that the noise is kept to a minimum, whilst the efficiency is maximised. The maximum allowed noise during the initial LHC start-up, with sensor temperatures $\sim -7^\circ$ C, is set at 1500 ENC, increasing to 2000 ENC during the end of the detector lifetime. With these specifications, this gives an efficiency better than 99% and a noise occupancy less than $5 \times 10^{-4}$. Finally, during the module production, a limit of 1% of the module channels are allowed to be defective.
C. Optical Communication and Readout

Optical links are used to transfer the data from the modules off-detector, as well as distributing the bunch crossing clock, level 1 triggers and commands to the modules [7]. The entire SCT system uses 8176 data links and 4088 transmission links. Vertical Cavity Surface Emitting Lasers (VCSELs) are used for transmission of light signals, and epixial Si p-i-n diodes for the receiving of light signals. For each module, two data links and one Timing, Trigger and Control link exist, and are housed in a light tight package. The data links are operated at 40 Mbit/s, transferring data from the modules off the detector. Single bit errors as well as random hits will cause a loss in the number of real hits being read out. An upper limit of 10$^{-9}$ for the bit error rate (BER) is set in order to maintain a high level of working efficiency for the optical links. The optical links used for the read-out of each module have undergone various stages of testing to ensure that they meet the requirements set out by SCT.

D. Installation and Commissioning

Figure 2: The ATLAS ID Endcap after complete insertion within the Liquid Argon Cryostat, May 2007.

By the summer of 2007 the SCT barrels and endcaps were successfully installed in the ATLAS cavern. All optical and power connections to the modules have been tested and most faults repaired. The electrical tests of barrel modules were initially delayed due to cooling problems. This caused a substantial delay in the time allowed for sign-off tests and further commissioning. In March 2008 the SCT barrel participated in its first “Milestone” run, M6. Within hours, cosmic rays were tracked within the detector. Since then, both endcaps have been signed off, but further problems with cooling have delayed any further participation in combined ATLAS commissioning runs. The cooling problems and solutions will be discussed further on in this note.

II. DETECTOR PERFORMANCE

The modules as well as the support structure and services were built at the collaborating institutes. The final assembly of the SCT barrel was performed at Oxford University, Endcap-A was assembled at NIKHEF (Amsterdam), whilst Endcap-C was assembled at Liverpool University. At every stage of the assembly chain, the modules and services were extensively tested. At production sites, the components were tested before being sent to one of the assembly sites for the construction of the barrel or endcap detectors. Four main stages of tests can be considered:

- Disc/barrel assembly
- Macro-assembly
- Surface reception tests
- Cavern tests

Initially the optical settings for the module communication were set before proceeding with testing the analogue and digital aspects of the module chips. The digital tests check that the redundancy links between modules are functional, the chips bypass links are tested as well as a test of the pipeline circuitry. The analogue measurements include calculating the gain, offset and input noise for each module channel. The performance results over these last two years will now be summarised.

A. Optical links

To allow for a stable data communication between the modules and the readout acquisition, the optical settings for the readout must be optimised. Various tests have been carried out to ensure the best working set-up with regards to sending data to and from the modules. It is also an important factor that the links can work over a wide range of settings. Each RX optical link needs to have the receiver threshold correctly set so that there will be no loss in valid hits from the detector. Analyses of the optical links performance have been performed for barrels and endcaps by calculating the working range of each link. In total, more than 98.7% of the links on Endcap-A were fully functional, 99.5% on Endcap-C and 99.4% on the Barrel. VCSELs which were either declared dead or too problematic to read out data were recovered via the redundancy scheme.

B. Leakage Currents

Module sensors were manufactured by both Hamamatsu and CiS [5]. The modules produced by the latter suffered from an earlier onset of micro-discharge and higher leakage currents. This was as a result of using the non-field plate strip configuration (where the metal strip is narrower than the width of the p-implant.) The barrel modules only used Hamamatsu wafers, therefore they did not suffer from this early micro-discharge effect.

Figures 3,4 show a typical I-V curve for a Hamamatsu and CiS module. The different field plate geometries are reflected in the results. A measurement was taken of all the modules in the ATLAS cavern. The measurements were repeated several times allowing the current to settle, before being ramped to the next voltage. On average barrel modules had leakage currents of ∼150-500 nA and endcap modules between ∼200-1000 nA at room temperature. There were 6% of barrel modules (127) and 3% of endcap modules, which were unresponsive to any bias application. These problems are in the process of being investigated.
Figure 3: A typical I-V scan for a Hamamatsu sensor that uses the field-plate geometry.

Figure 4: The CiS module shows higher leakage currents during an I-V scan due to the use of a non-field plate geometry.

C. Input Noise

A 3Pt-gain test [10] was the quickest form of testing the module to see that it was well within the specifications for input noise and channel efficiency. The scan determines the input noise using the gain, 50% occupancy threshold point and offsets for each module. A list of all the defective channels is also determined. In total 3897 strips were defective for Endcap-A, with a similar number for the barrel modules. This gives an efficiency of more than 99.7% of working strips. If a module has not been trimmed properly, then the input noise of the scan will show this, since the variation from channel to channel is noticeable.

Table 1: A summary of the mean input noise and spreads during the four main stages of testing. All values have been normalised to a module temperature of 0°C.

<table>
<thead>
<tr>
<th>Test Stage</th>
<th>OUTER</th>
<th>MIDDLE</th>
<th>SH-MIDDLE</th>
<th>INNER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disc</td>
<td>1608±51</td>
<td>1532±45</td>
<td>928±26</td>
<td>1070±32</td>
</tr>
<tr>
<td>Cylinder</td>
<td>1589±52</td>
<td>1529±46</td>
<td>929±25</td>
<td>1066±33</td>
</tr>
<tr>
<td>SR1</td>
<td>1592±77</td>
<td>1568±62</td>
<td>932±39</td>
<td>1082±45</td>
</tr>
<tr>
<td>Cavern</td>
<td>1622±83</td>
<td>1620±51</td>
<td>977±26</td>
<td>1119±32</td>
</tr>
</tbody>
</table>

Table 1 gives a comparison of the mean values and spreads of the input noise for the main stages of testing for Endcap-A. All values of the input noise are comparable at each stage of testing. There is a slight increase in noise measurements taken in the cavern. This was the first time that the modules had been read out whilst being integrated within the TRT. This could be one reason for the small difference in values. For Endcap-C and the barrel, the results were similar. In general, there were no signs of module damage over the course of time.

D. Thermal Performance

The temperature of the module hybrid was monitored using a thermocouple placed directly on the hybrid surface. The connection of each module cooling block to the copper pipe circuit determines the quality of the module cooling. The spreads in module temperatures were minimal. The barrel had a ∼1 °C spread on temperatures during testing, and for the endcaps the spread was within 2 °C for each module type.
III. COOLING PROBLEMS

The ID evaporative cooling has had a history of problems since detector commissioning tests were performed at the beginning of 2007. Two major faults caused a significant loss of time to the ID test schedule. The first major fault involved the SCT heaters and the second was a fault with the external cooling plant. The problems and solutions will now be discussed.

A. Heaters

The first substantial tests of the evaporative cooling was in February 2007 during Barrel testing. Part-way through the tests a short occurred within the heater electrical connector supplying the power to the heaters. The role of the heater is to boil away any remaining $C_3F_8$ liquid in the cooling pipes as well as raising the temperature of the $C_3F_8$ above the cavern dew point. It is a small heating element put inside the cooling pipe at the exhaust. After an investigation, it appeared that moisture was getting into the connector. Consequently, all heaters were removed and re-fitted with a sleeve to prevent any more moisture getting in. However, just before the endcaps were due to be installed in May, the same heater fault occurred. A new heater layout was introduced to allow the continueation of detector installation whilst a solution was found for the heater failures. Nearly 120 heaters were moved to a more serviceable area, from the cooling exhausts at the SCT detector to the back of the cryostat flange. This allowed more accessibility for the repairs and future replacements of the heaters. New pipe work had to be re-engineered and then everything installed and leak tested. This re-work took till the end of 2007 to complete, allowing no cold testing of the SCT.

A solution has been made by re-designing the heater connector. The new designs have been installed and tested. Several new designs of heaters are also underway in case of future problems. A printed circuit instead of a coiled wire is one option, the other is a passive system that uses a hot liquid to heat up the cold $C_3F_8$ liquid from the detector. In addition, there were problems found with the heat exchangers, requiring more re-work. The connections were not leak tight and they all had to be removed, re-soldered, re-tested and installed and leak checked.

With both these solutions having been implemented, there have been no more faults, allowing the sign-off tests of both the barrel and endcaps to be finished.

B. Cooling Plant

After the sign-off tests of the barrel and endcap, the pixel commissioning was underway. In May 2008, subsequent cooling problems caused considerable delays to the schedule. Three out of six ID compressors failed catastrophically. The magnetic couplers slipped during the cooling start-up and were unable to drive the crank used to perform the compression. They also acted as a sealant of the $C_3F_8$ cooling volume from the motor and the compressor shaft. This caused the compressors to burn out as well as the loss of 100 kg of $C_3F_8$ from the system and the remaining 900 kg contaminated. Fortunately, only the cooling plant was affected and not the detector itself. A huge clean-up operation was implemented, involving the cleaning of the cooling plant as well as re-pairing of the compressors. The replacement of dirty pipe work was also necessary and additional filters were put in place.

The actual cause of this coupling slippage is still unknown, since an incomplete logging of data has made it difficult to come to an exact conclusion. However, sensors have been added to the system to detect any future slippage of the couplers. A $C_3F_8$ recovery tank has also been installed and tested, preventing any further losses in cooling liquid. Since then, the pipe work has been leak tested, new $C_3F_8$ has been introduced into the system and a successful commissioning of the cooling plant has been made. The pixel b-layer was cooled successfully during the ATLAS beam-pipe bake out, with the centre of the beam pipe reaching 220 °C. Better monitoring and logging of the cooling system will ensure a better understanding of the future replication of a fault.

IV. COSMIC TESTS

For one week in March 2008, the SCT barrel participated for the first time in a global ATLAS ”milestone” run, M6. Many of the sub-detector components were run during this week, allowing cosmic particles to be tracked from the SCT right through to the muon chambers. Cosmics provide an extremely useful method for testing the detector performance. Firstly they test the entire readout chain of the detector and its sub-components. Investigations into cross-talk between modules and noise resulting from synchronous running of the SCT and TRT barrels can also be investigated. They also test the alignment of the detector.

Most cosmic rays at sea level are muons with a mean energy of $\approx 4$ GeV. Since the cosmic rays must pass through 100 m of concrete to access the cavern, the energies of the muons are expected to be much lower than those measured at sea-level. The cosmic muons entering the cavern, will do so predominantly via the two installation shafts, where there is no material for the cosmics to pass through. The angular spread of the cosmic rays is therefore limited affecting the frequency of cosmics passing through the SCT detector.

Three triggers were used during the M6 run. The tile calorimeter, the muon barrel resistive plate chambers, and an scintillator trigger specifically for the ID. Primarily the ID trigger was used, consisting of two scintillators placed above the muon chambers on level 8 in the ATLAS cavern. They were $144 \text{ cm} \times 40 \text{ cm} \times 2.5 \text{ cm}$ and positioned $\sim 1 \text{ meter}$ apart. Since the area of the scintillators is relatively small, a trigger rate of approximately 1 Hz was achieved. In order to have optimal charge collection efficiency it is essential to have a stable trigger time for the TRT and SCT detectors.

A. Timing

During beam physics, the SCT system clock will be synchronized to the bunch crossing clock cycle. However, for cosmics, the arrival of the particle is random within the system clock cycle. It is therefore necessary to measure the phase of the trigger with respect to the 40 MHz system clock. First, the clock and command signals of all the modules were synchronised to arrive at the same time. This is necessary, since compensation must be
made for the different propagating delays of the signals from the timing electronics to the modules. Next, the SCT is timed in properly to ensure the readout of the correct event to maintain a synchronised Bunch Crossing ID (BCID). A course delay is initially varied (in 3 clock cycle steps) and a peak in the number of coincidences versus timing offset gives the approximate timing. For beam data, fine delay scans (280 ps level) will be used to optimise hit efficiencies.

B. M6 Results

During run 43719, more than 1200 tracks were present in the SCT, of which 1183 were present also in the TRT. They were reconstructed successfully by the reconstruction software. Figure 6 shows an example of a track going through the upper and lower parts of the SCT barrel.

![Figure 6: A cosmic muon going through the upper and lower sector of the barrel SCT.](image)

Using the track parameters obtained from the reconstruction, a first estimate of the alignment between the TRT and SCT shows promising results. Without performing any alignment fits, a resolution of $-0.28 \pm 0.8\text{mrad}$ is found for the difference in phi measurements taken from the TRT and SCT $\phi$ track parameter. Residuals showing the difference between the x coordinate of the reconstructed track hit and the actual hit give values of 102 $\mu$m.

The noise occupancy was measured during cosmics run 43719. The results give an average module occupancy of $1.7 \times 10^{-4}$, well below the ATLAS specification of $5 \times 10^{-4}$.

V. CONCLUSIONS

The barrel and endcap SCT detectors are successfully installed in the ATLAS cavern. All modules and services have been tested and the detectors have officially been signed-off. The first steps towards global commissioning have begun, with the SCT joining their first milestone run in March, 2008. Cosmic rays have been tracked through the detector, testing the software and readout chain, as well as the module and track performance. Considerable delays have been caused due to faults within the ID cooling. However, these problems have now been solved and the SCT is due to resume the ATLAS global commissioning. Both beams were circulated in the LHC ring on September 10th, with the SCT endcaps biased at 20 V. Events were recorded in the detector with both endcaps glowing from beam halo muons. The SCT looks forward to its first collisions next year.

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Studies of the Assembled CMS Tracker

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Abstract

During the latter months of 2006 and the first half of 2007, the CMS Tracker was assembled and operated at the Tracker Integration Facility in Building 186 at CERN. At this time, several dedicated studies were carried out to validate the performance of the tracker after assembly, testing general noise performance, looking at a specific problem showing up for part of the tracker [1], and also looking at the performance at high acquisition rates [2]. We report on the the results of these studies and their consequences for operation of the Tracker at the experiment.

I. THE CMS SILICON STRIP TRACKER.

With its 210 m\textsuperscript{2} of silicon, 5.4 m length, 2.4 m diameter and 9.6 million readout channels, the CMS strip tracker is clearly the largest and most complicated silicon detector ever built. It consists of 4 main parts: the endcaps (TEC), the inner barrel (TIB), the outer Barrel (TOB) and the inner disks (TID). All together 15148 modules are distributed amongst these 4 systems. Because of its size and complexity, the collaboration paid meticulous attention to quality control and testing all the way through construction. However, some effects could not be detected during the construction and the final assembly of the subdetectors and the first large-scale tests were needed to point them out. This paper discusses the investigations into the cause of these effects as well as the ramifications for operations at the LHC.

A. TIF and Point 5

The first large scale tests were performed in the Tracker Integration Facility (TIF), a clean room constructed at the Meyrin site specifically for this purpose: the different subdetectors were brought together there and assembled from October 2006 until March 2007. Between March and July 2007, cosmos were taken at the TIF in a ’Sector Test’. All together 4.7 million cosmic triggers were recorded and up to a quarter of the tracker was read out using the final data acquisition (DAQ) electronics. During these tests, the tracker was operated at a range of temperatures, ranging from +15 to -15 degrees Celsius. The results of charge collection [3], track reconstruction [4] and alignment studies [5] agreed well with those expected from the construction studies.

The tracker was then inserted at Point 5 in the CMS Cavern in December 2007. The connection work took from December 2007 until March 2008 and after a short delay due to cooling problems, the tracker was commissioned between half June and end of August 2008. The TIF and the installation and commissioning at Point 5 provided the first possibilities for performing large-scale tests.

B. DAQ chain

To appreciate fully the effects discussed requires a rough idea of the CMS tracker Data Acquisition scheme. Figure 1 depicts the control flow to the front end ASICs, and the data flow back back into the electronics for processing and storage. The Front End Controller (FEC) VME board sends trigger and clock information to the Digital OptoHybrid Module (DOHM), which performs the optical to electrical conversion and forwards the electrical signals to the Control and Communication Unit (CCU), which distributes them to all front-end ASICs. The front-end ASIC (implemented as the APV chip) samples the strip charge, does the analogue pulse shaping, stores the data locally, and upon request transfers them optically to the Front-End-Drivers (FED) VME board. There the data is digitzed and under default operation clusters are formed and zero-suppression applied, dropping clusters below a preset threshold. Finally the FED pushes the data out to the Central CMS DAQ.

II. WING NOISE [1]

The Tracker Outer Barrel (TOB) is made out of 688 ”rods”. Each rod can contain up to 12 modules, and each module consists of 2 silicon sensors and 4 or 6 APV chips on a hybrid which services the sensors. A schematic set-up of a rod (without the sensors installed) can be seen in fig. 2. Cooling, power, optical readout and control signals all enter the rod from one end. Power and electrical signals are sent over a 51 mm wide circuit board called the interconnect bus, a multilayer board that is
symmetric between the top half and bottom half.

The noise (RMS) distribution of such a TOB rod shown in figure 3 looks rather strange. This normalized noise distribution from module 6 of a TOB rod shows a dramatic increase towards the edge channels of the APV chips, which resemble wings, from which the effect was named wing noise. These peaks reach up to 40\% of the average noise value of the module depicted, and can be even more pronounced on other modules. This effect escaped detection during module testing, and was discovered after the assembly of the rods. The observation that the effect is most prominent on module 6 for rods of layers 3 and 4 indicated that this position was special for those particular type of rods. The influence of the extra noise is so big that it would even affect tracking, therefore a solution needed to be found.

![Figure 2: Schematic view of a TOB rod](image)

To investigate the origin of the noise, shielding was applied to the different components of the rod. A testbench rod was used for the first investigations because it allowed more flexibility. The rod power bus was considered a first good candidate for sourcing the noise, because it runs under every sensor. Placing a sheet of copper-clad Kapton between the sensor and the interconnect bus eliminated all the noise, this happened independent of whether this sheet was grounded or not. This pointed in the direction of magnetic coupling, because even an ungrounded sheet would then remove all noise. For magnetic coupling, the copper generates eddy currents that would counteract the external field and thus block the external interference. For electrical coupling an ungrounded sheet of copper would act as a floating capacitor and continue to couple the noise into the sensor. In this case it could only reduce the noise, but never fully eliminate it. Similar sheets positioned between the sensor and hybrid or the fiber frame did not show any influence.

Having understood how the noise entered the sensors, the question turned to what the source was. After some investigation, the wing noise source was discovered to be the connection between the CCU and the DOHM on the rod. The noise current runs on top and bottom of the interconnect bus and is returned through the common ground in the middle. The problem lies with the DOHM differential signals to the CCU. These differential electrical signals are never fully balanced, and the imbalance current has to be returned to the DOHM via the ground of the interconnect bus. The excess current then sources the magnetic coupling. The current path for the noise current is from the CCU over the control circuit board to the power bus, through the power cables, supply rack and then the control power cables to the DOHM. This hypothesis was verified by adding a piece of copper tape between the DOHM and the circuit board, providing a direct return path for the current, which caused the noise to disappear. In addition, this was checked by putting ferrites around the power cables, increasing the impedance and thus reducing the noise current, which was observed. In performing this test it was realized that also the cooling pipes can provide an adequate path for this return current.

The most likely coupling is through the field component parallel to the sensor. The loop which creates the signal voltage is the following: aluminum sense lead on the top, the high voltage bias plane on bottom and the capacitance of reverse biased diodes at the two sides. One way of investigating this is through the bias voltage. Under this hypothesis increasing the bias voltage will decrease the capacitance and increase the impedance of the loop, thus reducing the current and for the APV (a charge sensitive amplifier) also lowering the noise signal. Thus the relative size of the wings should decrease when applying bias voltage, as is confirmed by data. The composition of the induction loop also explains why the noise is most predominantly present in layers 3 and 4. These layers have the largest width of strips, which will give the largest capacitance, thus resulting in most pronounced effect, as observed.

![Figure 3: Wing noise on a TOB module](image)

A. Investigation

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B. Solution and implementation.

The solution for this problem is to establish a common high-quality ground for the power cables, the control power cables and the cooling pipes. This was done for the tracker on the stainless steel cryostat of the CMS magnet. Small daughter cards with capacitors filtering external noise were designed that grounded everything together at the daughterboards (fig. 4), which were mounted on and grounded to the cryostat. This scheme was first tested at the TIF, and then in the CMS cavern at Point 5 by utilizing the Rod-In-a-Box (RIB). The RIB was the first piece of the final tracker installed at Point 5, brought there months before the tracker as a proxy to test and modify as appropriate the cabling and connection scheme for the tracker. The RIB showed that the daughter card scheme worked: the wing noise was absent initially, with the removal of the daughtercard, it reappeared.
The final results for the TOB noise distribution from the commissioning are shown in Fig. 5. At the left the results of the TIF (without daughtercards) are shown [3], and at the right the results of the commissioning are shown, after the scheme was implemented. The shoulder at high noise drops with \textbf{two orders of magnitude}. Currently there are only 9 modules on 7 rods (out of 688 rods) that still show some wing noise. This remaining 1\% of problems is most likely due to mechanical problems with those specific daughtercards or the grounding of the cables. This was already discovered on 8 other modules that were recovered after investigating the connections. When comparing these two plots one has to be aware that the commissioning results have been normalized, and the bump at low noise values is due to dead strips in the tracker.

At the TIF cosmics were used to sample detector performance, but these cosmics were at low trigger rate, of order 10 Hz, while the collisions in CMS will take place at high rate, up to 100 kHz. Therefore a dedicated study was performed to test the behavior of the system at high trigger rate. For this task, the data-acquisition system was augmented, replacing the FED VME readout which cannot sustain high trigger rates with a small scale slice of the final CMS DAQ called a "Column-DAQ". This Column-DAQ required hardware both for readout to acquire rapidly and trigger control to avoid buffer overflow. Fig. 6 gives an idea of this set-up and can also be used as a schematic for the CMS DAQ. As there was no physics signal which would give such high trigger rates, just noise and pedestals were measured using a random high rate trigger.

### A. Column DAQ

Since the final CMS DAQ was not available at the TIF, a special dedicated column-DAQ was built up. Rather than VME readout, data proceeds from the FED through Hardware using S-Link and dedicated network links to a switch and into a small scale computer farm emulating the CMS trigger farm, where it was written to disk. Even with these modifications, the readout was limited to at best 10 kHz. This necessitated further measures to increase the performance of the system. These steps included removing a software bottleneck in writing data to disk, adding an additional rail of network from the FEDs through the switch to the PCs, and the implementation of prescaling at various points in the system, randomly dropping events to relieve bandwidth pressure. With these modifications the 100 kHz level could be reached, but only taking data in Zero-Suppression mode, thus losing all information about channels below threshold. Looking at the occupancies in different channels did point out the effect described below, but not until another prescale was implemented, this time at the FED, the very beginning of the chain in Fig. 6, could the system take data from all channels in an event ('Virgin Raw' readout mode). This turned out to be a critical modification to provide a more thorough investigation of the phenomenon.

### B. High-rate noise characteristics.

When investigating noise behavior versus trigger rate, nothing special was observed at low rates. The behavior of the pedestals and noise at 100 Hz and 3 kHz is consistent. On the other hand, at rates above 30 kHz, a considerable growth in average occupancy took place at the edge channels of the chip (channels 127, 255,...), as shown in Fig. 7.
Testing on many different types of modules proved that this phenomenon was not isolated to a few modules, but affected every single APV of the tracker simultaneously and thus it was a global problem in the tracker running at High Rate, and not due to some faulty components. Fig. 8 illustrates this by showing two different fibers on the same FED and a fiber on a different FED (thus independent) all showing increased ADC counts near the edge channels on the same particular event. Once the full data was available, the common-mode subtracted pedestals could be calculated, and an anti-correlation between the behavior on strip 0 and that on strip 127 was observed and noted as a distinct signature of the high-rate noise. Another distinctive feature of the effect was that it only occurred in randomly distributed trigger intervals, not in fixed (high) rate trigger situations.

The first attempt to narrow down the source of the noise was to try to shield the sensors, motivated by the wing noise study. However, there was no reduction in the effect. Due to the fixed vs. random trigger effect, the trigger hardware was investigated to ensure it was obeying "trigger rules", not sending commands at the wrong time; no violations of the rules were found. Alternatively, the same effect suggests that perhaps the random trigger scheme was sampling some part of phase space that fixed triggers did not, such as some problem in the channel pipelines in the APV used to store the raw data before readout. By controlling exactly when triggers were sent the pipeline position dependence was studied and cleared from any blame. However, in the same study the observation was made that independent of the pipeline, certain intervals between two triggers yielded spikes of maximum occupancy as can be seen in fig. 9. These jumps happened for all fibers simultaneously around the magic bunch-crossing numbers 100, 160 and 380, and near these values of trigger interval the noise increases and when it reaches one of these numbers, the rise is the most pronounced.

C. Explanation

With the knowledge of particular intervals which trigger the effect, a deeper investigation using an oscilloscope to probe both the trigger commands and optical APV data when the effect occurs provided the final explanation for the phenomenon. The effect is caused by cross-talk between the data-acquisition and the read-out. Fig. 10 gives a schematic timeline of readout and acquisition. When a trigger arrives, the data which was buffered in the APV one latency (a programmable time delay) before the trigger arrives is flagged for readout. At the end of the APV's 7 µs readout cycle, this data is then pushed from the APV up-stream to the FEDs. This readout takes a full APV cycle, as is shown in the top half of fig. 10. Just before the APV starts sending data, it also draws more current, which can now affect the data-acquisition or the buffering of new data. Thus in case the trigger then also flags this data for read-out as done in the bottom half of the drawing, then the high-rate noise appears, as depicted in the bottom half of fig. 10. In reality, there are even three current rises during the APV's 7 µs readout cycle, this data is then pushed from the APV up-stream to the FEDs. This readout takes a full APV cycle, as is shown in the top half of fig. 10. Just before the APV starts sending data, it also draws more current, which can now affect the data-acquisition or the buffering of new data. Thus in case the trigger then also flags this data for read-out as done in the bottom half of the drawing, then the high-rate noise appears, as depicted in the bottom half of fig. 10. In reality, there are even three current rises during the APV's 7 µs readout cycle, leading to three magic numbers of 100, 160 and 380 bunch-crossings (1 bunch-crossing=25 ns at LHC). Thus the effect is an interplay between two tasks of the APV: the buffering and the sending of the data up-stream. This explanation has been confirmed by independent bench tests at Imperial College and simulations from Rutherford Laboratory.
Possible solutions

There are several ways to mitigate the high-rate noise which are under consideration. The high-rate noise could be identified offline and the corresponding data flagged as corrupted and thus thrown away, leading to a 1% loss of data, and therefore not favored. A second option would be to change the trigger rules, so that the 'magic' trigger intervals and the surrounding bunchcrossings are prohibited. This would lead to considerable deadtime, especially because intervals are hard to define in trigger rules, usually only lower time bounds are used. It would also be possible to deal with the problem further down the DAQ chain and hardware veto the triggers that arrive at the moment the APV is reading out data. This option still generates dead-time but a lot less than the trigger rules, the disadvantage is that it is difficult to implement in the firmware. Finally the anti-correlation observed in the common-mode subtracted pedestal could be used as a signal of the High Rate effect. The values of strip 0 and 127 are of similar magnitude but with an opposite sign in case of high-rate noise. This could be used to reject these events, but that is fairly risky since the algorithm is not optimized yet and it is not known how much good data would be thrown away. A variant on this option would be to flag these events and then deal with them offline. This would also require a firmware change to provide an extra flagging bit in the FED header.

IV. COMMISSIONING RESULTS

The overall results during the tracker commissioning are extremely good. The noise problems are under the percent level. In the end only 71 modules out of 15148 (0.5%) show a non-standard noise distribution. 9 of these are wing noise problems, but there are also a few new phenomena that showed up, like the mysterious noise (25 modules), figure 11a) and the MUX noise (18 modules), figure 11 b). The MUX noise owes it name to the spikes occurring every 16 strips, indicating a multiplexing problem on the concerned strings. Both of these new noise problems are correlated with bad supply of power to the modules or a bad control signal. This was noticed by looking at the voltage values at the modules itself, which turned out to be low for several of them and also by looking at odd synchronisation results indicating a problem with the control signals.

V. CONCLUSIONS

In general the CMS tracker performs extremely well, but there were a few small hiccups when the first large-scale tests were performed. Two new effects were found, the high-rate noise and the wing noise. A dedicated investigation at the TIF lead to the discovery of the origin in both cases and for the wing noise a solution has already been implemented. For the high-rate noise multiple options are still considered. These two cases showed the merit of the TIF as a testbench, as both problems were discovered there at an early stage, long before the tracker was moved to Point 5. This allowed for adequate measures to be taken in time. The daughtercard scheme was implemented before tracker arrival, and the high rate mitigation will take place well before CMS expects to reach high trigger rates. As commissioning ensues, new noise phenomena are showing up on a small scale, and the CMS tracker community highly anticipates what the first pp collisions may bring.

ACKNOWLEDGMENTS

The authors would like to thank especially everyone who worked at wing noise and the high-rate noise puzzles as well as the rest of the CMS tracker community.

REFERENCES

The CMS Tracker is, by far, the largest silicon detector ever built. It has 206 m$^2$ of active area and is comprised of 15232 modules with over 9.6 million readout channels. To operate the CMS Tracker, a large service infrastructure is required. This infrastructure consists of cooling, data acquisition, and power systems. Each cable, fiber, and pipe must be installed and tested prior to the installation of the tracker.

The tracker uses over 2000 power supply units (PSUs) located in 29 racks throughout the experimental cavern at Point 5 on the Large Hadron Collider (LHC) ring. The DAQ system has 440 Front End Drivers (FED), 80% of all the FEDs used by CMS, located in the service cavern. The cooling system consists of a primary chiller, which was intended to use a brine solution. The cooling geometry, with the tracker divided into 144 “Cooling Loops” then further subdivided into “Control Groups” and “Power Groups”. This structure allows small fractions of the tracker to be tested (and operated) independently.

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The control and safety systems have been partitioned around the cooling geometry, with the tracker divided into 144 “Cooling Loops” then further subdivided into “Control Groups” and “Power Groups”. This structure allows small fractions of the tracker to be tested (and operated) independently.

The immense size and complexity of the CMS Tracker and its infrastructure made it necessary to develop systematic testing procedures. Whereas the previous generation of silicon vertex detectors were tested by hand, by a small team, the CMS Tracker testing had to be automated with its progress carefully monitored. This was especially necessary as service installation was done in a tightly managed, overlapping sequence that distributed the various activities over the whole of the CMS central barrel wheel YB0, managing to work in parallel with other CMS activities, including installation of the electromagnetic calorimeter (ECAL) and heavy lowering of the barrel wheels and endcaps of CMS.

A. PP1 Checkout

The 2300 cables of the power delivery system connect from the power supply racks located on six balconies on either side of the experimental cavern to the Patch Panel 1 (PP1) boards located inside the solenoid. There are 14 PP1 sectors on each side of CMS (plus and minus), and each sector contains five PP1 boards (stacks) that have nine cable connections (places). Each cable end was then labeled with a unique identifier and barcode that showed its connection locations, rack, crate, board, connector for the PS end or sector, stack, place on the PP1 end. The label information is stored in an Oracle database which was used by the software during the checkout. The power cable connection was completed in November 2007 and then began the PP1 Checkout.

To assure that there were no errors in the physical cable map and that all cables were connected properly, a software tool was developed to test each cable and location. Loadboxes, built at Fermilab, were then connected up to five at a time to the PP1 locations. As the power cables also contain lines for the temperature and relative humidity sensors, these were tested by attaching “simulators” that would report a known value. The technician would attach loadboxes and probe simulators for each PP1 location and the automated test would then turn on the appropriate power supply and measure the load. Probe values were read from the PLC, checking the correct value was read at the correct location in the tracker. Each of the two low voltage and two high voltage channels and up to three probes were tested on each PP1 location. The results of each test were then stored in an Oracle database. In this way the PP1 Checkout tool verifies the entire control and power distribution system up to the PP1. This includes the logical map in the database, the physical cable map from PP1 to PSUs, and the cables from PSU to the PLC. Tests for the connection between PP1 and the tracker will be discussed in the following sections.

To monitor the progress of the PP1 Checkout, a web site was developed to show the test results by PP1 location. The web site provided different views, including overviews listing percentage of locations tested successfully, failed tests, and untested locations. Different filters could also be applied to the results to display specific failures (i.e. low voltage, high voltage, missing probe, ...) so the technicians could coordinate repairs by type. As the web pages were dynamically generated from the results...
database, the displayed information was always current. After initial installation approximately 5% of cables needed repair.

B. Interlock tests

The Tracker Safety System uses seven Programmable Logic Controllers (PLC) to read out all probes values. Based on the temperatures and humidities, the PLCs can interlock some or all of the power supplies to prevent damage to the tracker. A series of cables run from the PLCs in the service cavern to the power supply racks. This physical map of the interlock cables was tested by a software tool that simulates interlock conditions and verifies that the correct power supplies were interlocked. This test was particularly important because an error in the interlock map would endanger the tracker.

C. Cooling

Before the tracker was connected, one sector of the cooling pipes was tested to $-30^\circ C$ to check the insulation. Also, the two cooling plants were tested. During these tests, a weld in one heat exchanger failed allowing brine to contaminate the $C_6F_{14}$. This would have been disastrous had the tracker been connected as brine could cause corrosion of the cooling pipes inside the tracker volume.

This resulted in a delay in operating the final cooling system as all contaminated pipes and one plant had to be cleaned. Furthermore, all heat exchangers of this type were replaced and it was decided to replace the brine in the primary plant with $C_6F_{14}$ so another failure of this type would not endanger the tracker.

As a result of this delay, the first two months of the tracker checkout was performed with a temporary cooling plant. The capacity of this smaller plant was such that only four cooling loops could be tested simultaneously.

D. TKCC

The Tracker Connection and Checkout (TKCC) began following the completion of the PP1 Checkout. The TKCC began with the arrival of the tracker at P5 at the end of 2007. Simultaneously, cooling pipes were welded, fibers were attached, and power cables were connected from the tracker bulkhead to the PP1 boards. As connections were completed for each of the three systems it was logged in the database. When all three systems for a cooling loop were connected, that cooling loop was flagged as ready to be tested.

DCU/PSU Scan The DCU/PSU was the first test, using both the DCS and DAQ, to verify the cable map from the logical name in the database to physical connections from power supplies and FEDs to the detector elements. Each power supply was powered in turn, the DAQ then read out the unique Detector Control Unit (DCU) ID from each module. This ID was then cross-referenced in the database to determine that the correct detector element was indeed powered. Disconnected or faulty power cables would result in no DCU ID being read. Reading a DCU ID that does not match the tested detector element implies a swapped power cable. During the TKCC, less than 20 power cables were found to be disconnected or swapped. In the most severe case, one entire Control Group (8 cables) were determined to be swapped.

The repair of the cable problems was made easier due to the completion of the PP1 Checkout. Since the cable map was verified from PS racks to the PP1 boards, any swaps must have occurred between the PP1 boards and the tracker bulkhead. These cables were then checked at the PP1 and the bulkhead and reconnected if necessary. However, if changing the cable in PP1 or at the bulkhead was difficult or not possible the swap was made at the PSU and the cable was relabeled.

Connection Run The TKCC connection run measured light levels from the optical fibers. This served two purposes, first, to determine that the fiber was connected to the correct location and second, to detect dirty fiber connections. For a well-connected fiber one should see the light level saturate at 1023 adc counts. Fibers with very low light levels were cleaned.

Timing Run To account for the differing fiber lengths a latency offset must be determined for each fiber. The latency offset was calculated by the Timing Run. In the Timing Run the lasers were fired simultaneously, the response time was measured, and the offset was calculated. Before the Timing Run the cable structure can be seen, after the latency offsets are applied the latency is strongly peaked at the preferred value of 25 n.s.
Gain Scan  For each optical fiber the laser gain must be set. There is one laser for every two chips on a module. The gain scan is performed by measuring the adc counts with each of the four gain settings. A result of 640 adc counts is considered optimal.

Pedestal Run  The Pedestal Run is the final TKCC test and tests the HV, noise characteristics, and storing of pedestals to the database.

III. CURRENT STATUS

With the completion of the TKCC, commissioning using cosmic events began in mid-2008. The tracker participated in several cosmic runs with all of CMS using a global trigger. These runs which took place with the magnet off were known as the Cosmic Run Under ZEro Tesla (CRUZET). There were four weeks of CRUZET runs performed during the summer of 2008 with the tracker joining in weeks three and four. During the tracker’s first week participating in CRUZET, over nine million cosmic events were recorded.

First Beams  During the first beam event of September 10th, the tracker remained off. This was a precaution to ensure the safety of the tracker in case of a beam accident. Data from the Beam Condition Monitors showed nothing that would endanger the tracker.

IV. SLHC UPGRADE POTENTIAL

As a part of the SLHC Upgrade, the CMS Tracker will be replaced. The services (power, cooling, and fibers) will need to be reused, as many of the services are currently installed beneath other sub-detector (ECAL) services, for which, no upgrade is planned. As the service requirements for the SLHC Tracker are different from the current tracker, the possibilities for reuse are discussed in this section.

A. SLHC Environment

The SLHC upgrade is projected to deliver 10 times the luminosity, but with twice the bunch crossing interval. This results in an expected 400 pile-up events, up from 20, per bunch crossing. Specifically for the tracker, this means there will be ~20000 tracks, up from 1000 at the LHC. To reduce the occupancy in the tracker, it is planned to reduce the strip length by at least half, thus increasing the number channels.

B. Power

The two main factors determining the power requirements of the SLHC Tracker are the feature size of the chips, which then sets the operating voltage, and the number of channels. Current designs have many more channels than the current CMS Tracker due to the reduced strip length. A final decision has not been made, but there will be at least twice as many channels and probably much more. However, the SLHC tracker will use chips with a feature size no larger than 0.13 $\mu$m. This smaller feature size then has an operating voltage of 1.2 V, roughly half of the current operating voltage. With half the voltage, but at least twice the number of channels, the SLHC Tracker will have a higher total power consumption than the current tracker ($\sim 30$ kW). Smaller feature sizes of 0.09 $\mu$m and 0.065 $\mu$m are also being considered and would have an operating voltage of 0.7 V.

With a lower operating voltage, but more power used, the currents will be higher, as will the losses. These higher currents exceed the limits of the power cables. As a result, several new powering schemes are being considered.

DC-DC Converters  The use of DC-DC converters placed near the tracker bulkhead would allow a higher voltage to be delivered along the power cables, keeping the currents within existing limits. However, electronics placed near the bulkhead would have to be radiation hard and able to operate in a $4T$ magnetic field. It is also necessary to find a low-noise solution. Radiation hard air coils are being considered but the high noise presents a problem. Studies of several designs are currently underway.

Serial Powering  A serial power scheme would also keep the currents on the cables within acceptable limits. There are several disadvantages of serial powering that must be considered. Of most concern is that the failure of one module could cause the loss of all the modules in the string. Also, the modules have different grounds.
C. Cooling

An improved cooling system is being considered for the SLHC Tracker. With the high radiation environment of the SLHC it would be beneficial to operate the tracker at a lower temperature, possibly using coolant at as low as $-50^\circ C$. This would keep leakage currents down, thus power consumption, and improve beneficial annealing. While several cooling systems have been considered, the favored method is $CO_2$ cooling.

$CO_2$ cooling allows for a lower operating temperature, while providing additional benefits. With the lower viscosity of $CO_2$ smaller pipes may be used inside the tracker, reducing the material budget. Existing cooling pipes are already insulated, which is a requirement for the $CO_2$ cooling system, so reuse is possible between the plant and the tracker.

V. CONCLUSION

The testing of the CMS tracker services went smoothly. All services, power, fiber, cooling, and safety systems were tested systematically. The only delay was due to the failure of the cooling plant which limited the number of simultaneous tests because of the capacity of the temporary cooling plant. Currently, the CMS Tracker is commissioned and ready for physics with 99.7% of channels operating.

The SLHC upgrade presents new challenges for the CMS Tracker Services. Due to the position of service cables, underneath other sub-detector services, services must be reused. To keep occupancy low with 20 times more tracks, strip lengths must be reduced, increasing the number of channels. New smaller feature size chips help reduce the total power consumption, while increasing radiation hardness, but higher currents exceed existing cable limits. New powering schemes are being investigated that will allow more power to be delivered to the tracker without increasing currents in the existing cables.

The favored cooling system using $CO_2$ has the benefit of lowering the material budget, while operating at lower temperatures. The location of cooling pipes beneath other sub-detector services make reuse a necessity. This is also true for the fibers, which will also not be able to be replaced easily. In total, the CMS Tracker services have a good potential for reuse with the SLHC Tracker.

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The electronics of ALICE Dimuon tracking chambers

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Abstract

The muon spectrometer is one of the main detection system of ALICE, the dedicated heavy-ion experiment at CERN LHC. The muon tracking system consists of five cathode-pad chamber station (ST) with two detection planes each. The readout architecture, based on dedicated FE boards, embedded digital crates and a trigger dispatcher crate and the process to reach the electronics final design will be described, as well as the production and the tests of the 19,600 FE boards. Finally, the integration of ST1 at CERN (including EMC issues and commissioning) will be highlighted.

I. INTRODUCTION

The Quark-Gluon Plasma is expected to be formed in heavy-ion collisions at LHC energies. Several signatures of this new state of the matter will be studied by Alice [1]. The Dimuon spectrometer will be especially devoted to the measurement of the quarkonia, J/ψ, and Y, and heavy flavours which decay in muons. Because of very close mass of the Y states, a very good mass resolution, better than 100MeV/c² is required [2, 3]. It is directly correlated to a very good spatial resolution of the chambers with many consequences on the electronics requirements.

The ALICE Dimuon spectrometer is composed of several absorbers, a trigger system, a dipole and a tracking system. The muon tracking system consists of five cathode-pad chamber (CPC) stations with two detection planes each. The stations 1 and 2 are built with quadrants. The stations 3, 4 and 5 are composed of slats. The total chamber surface is about 100 m² [4].

The main responsibilities are the following : IPN Orsay is in charge of the electronics design and production for the whole tracking system. It is also responsible for the first tracking station (ST1) design and building, and for the Dimuon tracking readout software. SAHA institute (Kolkata India) is responsible for the second tracking station (ST2) design and building. IRFU-CEA Saclay, Subatech Nantes, INFN Cagliari, PNPI Gatchina laboratories jointly are responsible for the stations 3, 4 and 5 (ST345) design and building. Two ASIC were designed and produced for the experiment. The front-end readout ASIC called Multiplexed ANAlogue Signal (MANAS) was designed by Semiconductor Complex Limited (SCL Chandigar India) CMOS N-well 1.2μm, while the digital front-end ASIC so called Muon Arm Readout Chip (MARC) was design by INFN Cagliari team in 0.6μm AMS CMOS technology [5].

II. READOUT ARCHITECTURE

A. Specifications and environment

The main constraint is the chamber resolution which must be better than 100 µm to achieve the required mass resolution. The amount of channels is about 1.1 million. The noise must be lower than 2 ADC channels for a 12 bits conversion. With such a requested noise level the front-end electronics must be very close to the detection pads. In a CPC, the detection pads cover all the chamber surface and the front-end electronics must be plugged directly on the chambers, in the detector acceptance. Consequently, special care was taken in the design of the front-end boards to keep their thickness as small as possible in term of radiation length. In addition, in the detector area, the magnetic field value is up to 7000 Gauss, the radiation level is of the order of 500 Rad for the total dose, and the equivalent of 27 neutrons/cm²/s (E>2MeV) [6].

B. Readout architecture

For the 5 stations, the readout principle is the same (See Figure 1). The wire chamber pad signals are processed by front-end MANAS ASIC which insure the signals amplification, their shaping with a 1.2µs peaking time and multiplexing of the 16 channels. These circuits are embedded on MANAS NUmérique (MANU) boards. These boards insure the digital conversion and the data transmission through a MARC ASIC. Sets of MANU boards are connected together on a data bus transmission line called Protocol for Alice Tracking Chamber (PATCH) Bus. Then they go through Translator boards to a digital Concentrator Read-Out Cluster Unit System (CROCUS) Crate. These CROCUS crates are directly connected to ALICE DAQ with an optical link. They receive the Trigger signals through a Trigger Crocus Interface (TCI) Crate. The system represents a large amount of various boards. There are more than 19,000 MANU boards to process about 1.1 million channels. The CROCUS read out crates (22 crates) which include FRonTal boards (120 CROCUS-FRT), ConcentraTor boards (22 CROCUS-CRT) and 22 BACK-Panels. The trigger dispatching crates (two Trigger Crocus Interface (TCI) crates which include two types of boards: Frontal Fan-out Trigger (FFT) and Frontal Trigger Dispatching (FTD)) and the related software were designed at Orsay and were produced for the whole Dimuon spectrometer collaboration [4].
The readout of the buses is performed thanks to a token. Bridges are implemented to bufferize the signals. Moreover, on very long buses, boards called Translator board. The lines currents were increased so that these thresholds can shift up to +/-30mV without data loss. Each MANU board deals with 64 channels. The front-end MANAS circuit deals with the data processing functions and a calibration capacitor, for online detector calibration. The main issue is the gain dispersion between the electronic channels which gives a wrong charge measurement on these channels. Without charge correction, especially gain correction, the impact point is not correctly determined leading to a bad spatial resolution. The MARC circuit drives all the detectors configurations parameters, the data transfers from detectors to DAQ, and the data transfers from DAQ to the MANU boards. The system is designed so that it can read any types of bus lines. The operator can describe the detector that he wants to read (number of buses, number of MANU boards on each bus) and the DAQ send an address to each MARC. Due to the fact that we just want to read hit pads an important function of the MARC circuit is zero suppression. For this purpose, pedestals measurements are performed and thresholds are computed and stored into MARC circuits. Online, MARC circuit is also able to switch off one MANAS of its board or to switch off the full MANU board if it is requested by the shifter.

During the detectors debugging phase, we had to tune the current in some Bus Patch to be able to read them or to increase the safety margin to read them. The data edges are detected High or Low with to corresponding thresholds on comparators. This detection is made on a terminal board called Translator board. The lines currents were increased so that these thresholds can shift up to +/-30mV without data loss. Moreover, on very long buses, boards called Bridges are implemented to bufferize the signals. The readout of the buses is performed thanks to a token which is sent to one MANU board which keeps it while it sends its data on the bus and then sends the token to the next MANU board.

### C. Bus lines principle

A key point on the detectors is the data transmission. It is performed thanks to lines called Bus Patch. They were designed at Orsay but each laboratory adapted the system for its station. Each MANU board is connected on the line and the impedance matching is calculated for the board located in the middle of the line. All the other boards are not impedance matched. The line impedance is settled with a resistor impedance terminal at the end of the line. This is an acute problem especially for ST1 which density is quite high as seen on horizontal lines in Figure 2 (the black rectangles are MANU boards).

### E. CROCUS crates

All the data readout is driven by the CROCUS crate. The CROCUS crate receives data from a maximum of 50 Patch Buses spread on 5 CROCUS_FRT boards. 10 Patch Buses are connected to 1 CROCUS-FRT, more precisely 5 Patch Buses are connected to 1 frontal Data Signal Processor (DSP), so there are 2 frontal DSP per CROCUS_FRT board. The data speed transmission between the Patch Buses and the CROCUS_FRT is 40 Gbits/s via LVDS links. Each CROCUS_FRT DSP is connected with one link port to one CROCUS_CRT concentrator DSP (Figure 4). There are 10 link ports for the 10 CROCUS_FRT frontal DSP connected via the Back Panel to 2 CROCUS_CRT concentrators.
The data transmission speed on these link ports is 200 Mbyte/s. Then a CROCUS CRT Master DSP concentrates the 2 DSP data via a 320 Mbyte/s parallel bus. This Master DSP sends the data via a Xilinx FPGA to a Single Interface Unit (SIU) board (designed at CERN) which sends the data via an optical link to Alice DAQ. All these transmissions are driven by some FPGA.

Figure 4: CROCUS CRT Diagram

All the readout sequence was tested on quadrants and slats to tune the whole timing managements. A Jtag chain is implemented on the boards so that all the CROCUS FPGA programs can be modified and reloaded from the Alice control room. Another point is the detector calibration, which is an important concern for the tracking. A dedicated piggy-back board was designed to be embedded on CROCUS-FRT boards. A signal is sent to all the MANU boards thanks to a DAC and some switches.

F. Trigger CROCUS Interface

This crate insures the dispatching of the trigger signals to the 20 CROCUS crates. Two different boards were designed: FFT board and FTD board. FFT board receives the trigger signal from the Central Trigger Processor and dispatches it to 5 FTD boards (one per station). The crate receives the trigger signal through a Clock distribution board called TTCrX and designed at CERN. Many tests were necessary to control the delivered trigger sequences and to deal with the data errors. The TCI crate also has a function of CROCUS crate checking.

III. CONSTRAINTS IMPOSED BY THE ENVIRONMENT

The front-end electronics is plugged directly within the detector acceptance (MANU boards) or very close to the detectors (CROCUS crates) with consequences on the design.

To decrease the matter thickness in front of the detectors, the MANU PCB are to the upper limit of today technology in term of thickness, they are very thin (0.5mm, 6 layers) and the component density is quite high, so the manufacturer had to face many problems in the fabrication process. In addition, the ground layers in these PCB are wire meshed. The other power supplies are carried with wires instead of layers, which is not recommended to deal with such low noise levels, but it was sufficient for us.

All the metallic structures as Crocus crate are amagnetic ones because of the high level magnetic field. The crocus crate was especially designed to be embedded close to the detectors.

Many Radiation tests were performed. The total dose should be 500 Rad for 10 LHC years. The MANAS were tested up to 13 kRad [6] with no changes in noise and gain up to 12.8 kRad. A decrease of pedestals value was observed after a 1 kRad dose. However, this does not represent a problem since, as previously mentioned, pedestals measurements are regularly foreseen to perform zero suppression. It should correct their decrease, if they decrease.

MARC circuits were tested for SEU hardness for a $5.6 \times 10^{11}$ cm$^{-2}$ equivalent hadrons fluence which is expected for the Dimuon spectrometer. For the whole detector, the SEU rate will be 56 per day. With a pedestal reload every 6 hours, the error rate will be negligible compared to the total number of channels (1.1M).

FPGA and DSP also were SEU hardness tested with an equivalent rate of 27 (E > 2MeV) neutrons per cm$^{-2}$/s. The results were 1 SEU every 5 hours for the Stations 1 and 2 and no SEU for the stations 3, 4 and 5.

The stations 1 and 2 are mounted in a confined environment. So, an air cooling system was carefully designed. During the commissioning period the measured temperature was lower than 30 °C.

IV. ELECTRONICS PRODUCTION

We produced 19600 Manu boards, 22 CROCUS read out crates including 110 CROCUS-FRT boards, 210 calibration boards, 22 CROCUS-CRT boards and 22 back-panels. We also produced and tested about 450 Translators boards for ST1 and ST2, 150 special board for ST2 called bridges, about 675 translator boards and about 350 bridges for Stations 3, 4 and 5. Two TCI crates with 10 FTD boards and 2 FFT boards were produced.

A. Front-end boards production

After production, the 19600 boards were numbered and were tested in industry from 2005 to 2007. For tests purpose, a dedicated test bench was developed and transferred to industry (Figure 5).

The test bench has a go/no go function and a diagnostic option to help for the boards repairing. Each MANU board wears a barcode with its number. The test bench produces a test sequence for the power supplies short circuits, for the MARC circuit test (i.e. all the transmission protocol), for the MANAS specifications (i.e. pedestal, noise, gain, value of the internal calibration capacitor). A data file was produced and delivered to Dimuon Spectrometer.
collaboration with the data of each Manu boards. The test bench deals with two MANU boards at the same time. It sends the calibration signals through the same calibration generator as on the CROCUS-FRT boards. The program was written in Visual C++ language.

V. INTEGRATION AT CERN

A. Detectors mapping

Because of the channels gain dispersion, the detector must be fully mapped. The average channel gain is about 3.3mv/fC and we sorted gains from 3.1mV/fC to 3.45mV/fC. All the other values were rejected. As said before, the Front-end boards are numbered with a bar code. All the detector locations are also numbered with a bar code. So, we have a channel/gain corresponding file for the whole detector, and corrections can be implemented to reach a resolution better than 100 µm.

B. EMC questions

We were extremely careful concerning the EMC questions. The boards design included power supply layers and guard rings between analogue and digital parts. The power supplies are filtered with devoted SHAFFNER FN7562-32-M4 100 nF capacitors. They provide an attenuation of 65 dB for 100 MHz signals and 40 dB for 10 MHz signals. Three capacitors, one for each power supply, are implemented in dedicated filtering boxes (figure 6). The global electronics grounding was studied and implemented on the detectors. The data transmission cables are flat shielded cables, and all the data are driven with LVDS level differential lines. There is a large mechanical grounding for these cables both on the Crocus crates and on the detectors. Inside the Crocus crate, the EMC problems are solved with individual boards shields. Concerning this matter, Station 1 and Station 2 are in a favourable configuration: all the metallic parts (filtering boxes, Crocus crates, detector supports) are screwed on the grounded Alice structure as seen on figure 6.

C. Tests summary

Many beam tests were performed to validate the detectors and the electronics design. During these beam tests the spatial resolution was measured to 50 µm [7].

Each board (a global amount of 21,000 boards including 19600 MANU) was individually tested and the FPGA and DSP programs were downloaded. ST1 and ST2 assembly began, and each bus line was validated with a CROCUS-FRT board readout. Concerning Station 345 all the slats were validated with a Crocus crate. For station 1 each quadrant was tested with a cosmic-ray test bench which included a full readout Crocus system and the final water cooled Wiener PS512 power supply.

1) Pedestals run

The first tests were pedestals runs, without high voltage, with a 2.5 kHz random external trigger. They show quite uniform values (about 300 ADC channels) of the pedestals for all the tested channels. The corresponding noise is 1.2 ADC channel corresponding to 0.73 mV or 1300 e- for a full readout channel including the MANAS circuit, an amplifier and the ADC AD7476 (figure 7). The MANAS calibration test showed a 1.8 V linearity (2.5 V power supply). So the electronic dynamic range is about 11 bits, which is quite good.

2) Cosmic run at Orsay

With a 1600 V High Voltage applied to the detector, we observed many correlated spots between the two cathode planes of each quadrant. These events are due to cosmic rays and confirmed the functionality of the zero suppression system (Figure 8).

3) Installation at CERN

All the detectors were tested again after their shipping in a surface building at CERN (pedestals tests). Then, they were mounted in the cavern and electrically connected.
Figure 7: Display of the electronic noise in ADC channels of a full cathode plane of ST1

Figure 8: Cosmic signals
At the end of their integration, the CROCUS crates were connected to ALICE DAQ and the CROCUS software was integrated in the ALICE Data Acquisition system. In September 2007, the first chambers readouts were performed. 115,200 channels were read (figure 9). The results showed the same levels of pedestals and noises as in the laboratory tests or in the surface tests. It shows that the EMC choices implemented on the detectors are correct. Then a first Cosmic test was performed in December 2007 with zero suppression. The first track crossing Station 1 and Station 2 as well as the muon trigger was observed in March 2008 (figure 10).

VI. CONCLUSIONS
In September 2008, half of the Dimuon spectrometer was successfully commissioned. The CROCUS software is integrated in ALICE DAQ system, so the Dimuon spectrometer can participate to ALICE runs. The electronics functionalities were tested: pedestals runs, zero suppression mode data taking. The average pedestal is around 300 ADC channel, it is uniform and stable. The noise is 1.2 ADC channel, and it is stable. The conditions are good so that a less than 100 µm chamber resolution can be reached. The commissioning of Dimuon spectrometer is being completed.

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Readout Electronics of the ATLAS Muon Cathode Strip Chambers

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Abstract

The ATLAS muon spectrometer employs cathode strip chambers (CSC) to measure high momentum muons in the forward regions ($2.0 < |\eta| < 2.7$). Due to the severe radiation levels expected in this environment, the on-detector electronics are limited to amplifying and digitizing the signal while sparsification, event building and other tasks are performed off-detector.

I. INTRODUCTION

The CSC system is designed to measure high momentum muons in the forward regions (pseudorapidity $2.0 < |\eta| < 2.7$) of the ATLAS detector [1]. Its principle of measurement is to determine the hit coordinates by interpolating charge deposited on adjacent strips. Multiple layers of strips allow for tracks to be formed from these hits. At an expected strip hit rate of up to 600 kHz a signal-to-noise ratio of 150:1 is required to obtain a single layer resolution of $\sim 60 \mu m$.

A total of 32 chambers are arranged in two endcaps, as part of the ATLAS ‘Small Wheels’ which are positioned between barrel calorimeter and endcap toroidal magnets. Two versions of chambers, differing slightly in active area, are used ('large' and 'small') alternately for seamless coverage of the desired $\eta$ region. A chamber has four identical layers, each providing a precision measurement in the (radial) bend direction and a coarser measurement of the transverse (azimuthal) coordinate. Each chamber has a total of 768 precision coordinate strips and 192 transverse coordinate strips. The precision strips have a readout pitch of 5.31 and 5.67 mm for large and small chambers, respectively. The strip capacitance ranges from 20–50 pF, depending on strip length which varies due to the chamber’s trapezoidal shape.

Because of the severe radiation levels anticipated for the CSC environment, a minimum of the electronics is located on the detector. The on-detector electronics amplifies and shapes the cathode strip signals, and stores the analog pulse height information during the first-level trigger latency. When a trigger is received, four consecutive time samples are digitized and transmitted via fiber-optic links to the off-detector electronics. Sampling and digitization are performed on-detector but are controlled by the off-detector electronics.

The off-detector electronics processes the data in two stages. The sparsification stage suppresses hits below threshold and hits not associated with the current bunch crossing. The rejection stage identifies tracks and removes isolated background hits. The remaining data are formatted and sent to the ATLAS Trigger/DAQ System (TDAQ) for further processing.

II. THE CSC READOUT ELECTRONICS

A. The on-detector electronics

The CSC on-detector electronics [1, 2] consists of two layers of amplifier-storage module (ASM) boards. Each strip is connected to a preamplifier and shaper circuit, implemented as a radiation-tolerant custom ASIC, which forms a bipolar pulse with a 70 ns peaking time to mitigate pile-up effects. The shaped pulses are sampled every 50 ns, and the analog pulse height information is stored in a custom radiation tolerant CMOS switched capacitor array (SCA) for the duration of the first-level trigger latency, which for the CSCs is estimated to reach 188 bunch crossings in the worst case scenario. The SCA provides an effective pipeline depth of 288 bunch crossings. Following a trigger, those cells of the SCAs specified by the ROD are time multiplexed and digitized using 12-bit Analog Devices AD9042 ADCs. Custom ASICs multiplex the data from 16 ADCs to two G-Link serializers configured to operate with 16-bit input words at 40 MHz single frame rate.

Eight preamplifier/shaper ICs supporting a total of 96 channels reside on a printed circuit board (ASM-I). Two ASM-I boards piggyback on one
ASM-II which contains the 16 SCAs, ADCs, multiplexors serving 192 channels total, and two fiber optic G-Link transmitters. One HP-1024 fiber optic receiver handles incoming control signals from the ROD. A total of five such ASM-I/ASM-II combinations are needed to read out one chamber – four for the precision coordinate strips and one for the transverse coordinate strips from all four layers. Four ASM-I/ASM-II configurations are attached to the narrow edge of the chamber and share a common Faraday cage and cooling fixture. The transverse strip ASM-I/ASM-II package is attached to the broad side of the chamber, together with circuitry for injecting a pulse onto the wires of each layer for calibration purposes.

Figure 1: Principal design of the CSC off-detector electronics.

**B. The off-detector electronics**

The off-detector electronics [3] consists of 16 readout drivers (RODs), each coupled with a transition module (CTM). Each ROD/CTM pair handles the incoming data of two chambers, i.e. from 10 ASM-II boards (Fig. 1). It also controls the ASM-II, in particular the readout of the SCA when a trigger has been received. In addition the ROD provides data monitoring functionality, and controls the calibration pulser module. Eight RODs are housed in one 9U VME64x crate equipped with an additional custom backplane. The CTM contains all op- toelectronics for readout and control of the ASM-II boards as well as for sending the processed data to the data acquisition system. It connects to the ROD directly via the custom backplane. A timing interface module (TIM) [4] in each VME Crate distributes clock and trigger signals to the CTMs. Each crate contains a Concurrent Technologies VP-110 single board computer which acts as ROD crate controller (RCC). It communicates with the TDAQ via Ethernet, and is responsible for relaying control commands from the TDAQ to the RODs. It also is used to collect information from the RODs for monitoring purposes.
While most of the ROD’s control and data routing functionality is implemented in Xilinx Spartan-II field programmable gate arrays (FPGAs), processing of the ten 160 Mbyte/s data streams from the ASM-II boards is handled by digital signal processors (DSPs).

One 300 MHz Texas Instruments TMS320C6203 DSP with 2 MBytes off-chip memory supported by two Xilinx Spartan-II FPGAs for interfacing are grouped together on a small plug-in module. The ROD hosts 13 such modules, 10 for sparsification and cluster identification, two for event building and further background rejection, and one host module (HPU) which supervises the others and communicates with the RCC via the VME bus.

Most of the CTM’s functionality is implemented in Xilinx Virtex-II Pro FPGAs. This includes the multi-gigabit transceivers for communications to the frontend, which couple with Zarlink ZL60101/2 12-channel parallel fiber optic modules (one transmitter and two receiver modules per CTM). Fiber optics communications to the ATLAS DAQ are provided by a HOLA S-Link [5] mezzanine card which plugs into the CTM.

C. Off-detector electronics software

Signals associated with a particle trajectory must be correlated both in space (adjacent strips) and time (synchronized peaking times). The four consecutive time samples (Fig. 2) retrieved from each strip provide pulse shape information, i.e. charge and time. The effective trigger latency is adjusted so that the second and third sample are closest to the peak of the positive lobe.

Receipt of a first-level trigger automatically leads to readout of the four samples associated with the event. At the same time, the trigger information is propagated to the HPU.

The ten sparsification processing units (SPUs), one per ASM-II, reduce the raw data size by suppressing strip signals below a threshold determined by the channel’s measured pedestal value, and by rejecting signals outside the timing window correlated with the trigger. The SPU applies calibration constants to the data, organizes the hits into clusters and determines their peaking time [6].

Data from the frontend is distributed to the SPUs via a bus system connecting to the DSP’s expansion bus (XB). Data flow between SPUs and RPs, and to the S-Link, is handled by a separate bus system called the data exchange (DX). It connects to the extended memory interface (EMIF) of the DSP. For each event, the fragments produced by the SPUs are moved to the associated rejection processing unit (RPU) in sequence. It performs a track search based on the clusters identified by the SPUs. Isolated clus-
ters are then removed from the event. The remaining data are transferred via the DX and the 160 Mbyte/s S-Link to the readout buffers of the ATLAS TDAQ system, where the data is stored during subsequent second-level trigger processing and event building.

The HPU controls and maintains the readout pipeline, i.e. it has the capability of throttling the data flow at various points of the pipeline. While raw data events are delivered to the SPU input buffers automatically, all subsequent steps – the actual processing of the data, transport from SPU to RPU, transport from RPU to S-Link – are only performed if requested by the HPU. Frontend readout can only be throttled by inhibiting triggers via a busy signal propagated to the ATLAS trigger. The event header and trailer – containing trigger, size, and status information – is inserted by the HPU directly. The assembly of the complete event fragment from two chambers is completed by sequencing header, payload, and trailer accordingly on the DX.

III. COMMISSIONING

The complete readout chain from chamber to ROD had previously been tested with cosmic rays and with >100 GeV muons.

The chambers with attached frontend electronics were assembled on the Small Wheels in 2007 and commissioned one chamber pair at a time. The Small Wheels were installed in the ATLAS experimental cavern early in 2008. A full system readout has not been possible at the time of this conference due to a limitation of the VME power supplies, the solution for which is awaiting implementation by the manufacturer.

In the meantime, vigorous debugging efforts are made to remove the last stability and rate limitations in the ROD firmware and software. The system is expected to be ready in time for first collisions at the LHC.

IV. CONCLUSIONS

Muon tracking in the forward region of ATLAS is performed by cathode strip chambers. Because of the harsh radiation environment, the on-chamber readout electronics are kept as simple as is practical. Noise reduction measures are entirely performed off-detector. The off-detector electronics use DSPs for noise reduction and event building. At this time all hardware is installed. Firmware and software of the off-detector electronics is being debugged.

ACKNOWLEDGEMENTS

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Design and Commissioning of the ATLAS Muon Spectrometer RPC Read Out Driver

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Abstract

The RPC subsystem of the ATLAS muon spectrometer provides the Level-1 trigger in the barrel and it is read out by a specific DAQ system. On-detector electronics pack the RPC data in frames, tagged with an event number assigned by the trigger logic, and transmit them to the counting room on optical fibre. Data from each sector are then routed together to a Read-Out Driver (ROD) board. This is a custom processor that parses the frames, checks their coherence and builds a data structure for all the RPCs of one of the 32 sectors of the spectrometer. Each ROD sends the event fragments to a Read-Out subsystem for further event building and analysis. The ROD is a VME64x board, designed around two Xilinx Virtex-II FPGAs and an ARM7 microcontroller. In this paper we describe the board architecture and the event binding algorithm. The boards have been installed in the ATLAS USA15 control room and have been successfully used in the ATLAS commissioning runs.

I. INTRODUCTION

THE Large Hadron Collider (LHC) is a proton-proton collider, with a centre of mass energy of 14 TeV, which started operation in Sept. 2008 at CERN. The ATLAS experiment has been installed at one of the four LHC’s beam interaction points. ATLAS is an “all-purpose” detector designed to have almost a 4π geometry around the interaction vertex and it has a cylindrical symmetry along the beam axis; it is made of different sub-detectors, each with its own dedicated read-out electronics. Its inner tracking detector is located inside a 2 T axial magnetic field; outside there is a liquid argon electromagnetic calorimeter and a hadronic calorimeter using scintillating tiles in the barrel and liquid argon in the endcaps. In the outer region, the muon spectrometer is instrumented with precision measurement chambers and trigger chambers. The bending magnetic field in the muon spectrometer is generated by an air-core toroid made by 8 coils.

Resistive Plate Chambers (RPC) are used both for trigger and readout purposes in the barrel region (figure 1). The RPC chambers are arranged in projective towers to form three cylinders concentric with the beam axis and have a 16-fold segmentation in the azimuthal plane, following the eightfold azimuthal symmetry of the magnetic structure. The whole Muon Spectrometer barrel is divided into 32 physical sectors (16 within each half barrel).

In order to reduce the interaction rate from 1 GHz to 100 Hz, the ATLAS trigger has been designed with a three level architecture. The raw rate of 1 GHz proton-proton interactions is reduced to 75 kHz by the Level-1 trigger system, that also flags interesting events with a Level-1 Accept signal (L1A) with a fixed latency of 2.5 µs.

II. THE ATLAS SYNCHRONIZATION SYSTEM

In the LHC collider [1], protons are grouped in “bunches” that interact every 25 ns. From the point of view of the trigger system, ATLAS is a synchronous system working at 40 MHz, the bunch crossing frequency of the LHC. All the trigger electronics are driven by a common clock signal, synchronized with the bunch crossing frequency of the collider. Different from the trigger, the DAQ dataflow does not have a fixed latency and can be considered asynchronous with respect to the bunch crossing. However, the RPC DAQ system is also synchronized with the same clock, in order to share resources with the LI trigger and optimize the routing of the distribution system.

Front End electronics associate the data in each event to a number identifying the bunch crossing that generated the collision (Bunch Crossing Identifier, or BCID) and to a unique progressive number (Event Identifier, or EVID) identifying that event. The BCID is incremented every LHC’s clock cycle and the EVID is incremented every time a L1A pulse is generated by the trigger processor and the; both these numbers are managed by counters on the front end boards synchronously to the LHC’s clock. In
In order to initialize and handle these two identifiers (i.e. EVID and BCID), two signals are transmitted: the Event Counter Reset (ECR) is issued on request by one of the subsystems of the ATLAS apparatus, if a malfunction has occurred; the Bunch Counter Reset (BCR) is transmitted periodically after every orbit, in order to rewind the BCID counters.

Because of the large dimensions of the detector, the reference clock, the L1A, the ECR and the BCR signals must be transmitted over distances up to hundreds meters. In order to allow the synchronization of the DAQ systems with the machine clock, a physical layer has been chosen, able to distribute the clock and control signals to all elements of the ATLAS apparatus, with programmable skew and low jitter. This is made by the Trigger Control System (TCS) and the Timing Trigger and Control (TTC) system.

The TCS is in charge of the generation of the trigger and timing signals. The TTC system is responsible for their distribution to the entire detector. The TTC receives from the TCS the 40 MHz clock signal, the L1A, BCID, EVID, BCR, ECR and other service signals. All these signals are coded and optically transmitted, over a tree structure. At the destination, the receiver board TTCrq [2] restructures the signals and adapts them to the protocols of every sub-detector.

### III. The RPC Read-Out System

The trigger and RPC readout system of the ATLAS’ muon spectrometer is split between on-detector and off-detector sections. The level-1 muon trigger in the barrel region is based on a fast geometric coincidence [3] between different planes of the RPC detectors. On-detector electronics execute, every 25 ns, the trigger algorithm and send, via optical links, the relevant trigger information to the off-detector Trigger Processor, that can validate or reject the event with a fixed latency of 2.5 µs.

Data produced by the RPC detectors are written in FIFO memories on the on-detector electronics and are kept in the buffers during the decision time of the Trigger processor. If an event is accepted by the first level trigger, a L1A pulse is generated and transmitted across the TTC system together with the pertinent EVID and BCID. After the arrival of the L1A pulse, data stored in the FIFO buffers are transferred to the off-detector electronics over the same optical link used for the transmission of trigger information. Trigger and read-out data of each of the 32 sectors of the spectrometer are managed by a Read Out Driver (ROD) crate (see figure 2).

The main task of the RX-SL boards is to receive and elaborate trigger and read-out data from the on-detector electronics. The RX/SL boards pre-process the trigger information and send them to the Trigger Processor through the Muon Central Trigger Processor Interface board (µCTPI) [4], across a custom backplane. The RX/SL boards also arrange readout data in an event frame (RX Frame) and transmit them to the adjacent Read Out Driver across a custom backplane RODbus via a high speed serial link.

The main task of the ROD is to perform a further framing of the readout data, before transmitting them across the optical link S-Link to the next acquisition levels, i.e. to the Read Out Systems (ROS). The ROD also manages the timing signals of the trigger and DAQ system. For this purpose, the ROD hosts a TTCrq receiver module from which it receives the ATLAS’ timing and control signals to be forwarded to the RX/SL boards on the RODbus.

On the RODbus, data and timing signals are transmitted in LVDS standard to achieve high rate, low skew and jitter; the serial links between each RX/SL and ROD have an aggregate bandwidth of ~ 2 Gbit/s (48bit@40MHz) [5]. Control signals run at lower rate and are transmitted using the TTL standard. The RODbus also hosts a 48-bit TTL bus that allows the RX/SL boards to transmit trigger data to the µCTP board.

The ROD boards developed for the other ATLAS sub-detectors [6, 7] implement different logic and functionalities, in order to fulfill the specific detector requirements. However, they all share the same logical output format and optical physical layer. In this way, the ROS design is unique for the entire apparatus, making it possible to use the same architecture for the higher level DAQ systems [8].

A ROS unit is implemented with a 3.4 GHz PC housing 4 custom PCI-x cards (ROBIN), each hosting 3 S-Link optical receivers (Read Out Buffers). Therefore, a ROS unit receives and stores up to 12 event fragments from different channels of the ATLAS detector. Such fragments can be forwarded to the Event Builder, if the event is accepted by the Level-2 trigger, otherwise it will be dropped. The Event Builder is in charge of merging the event fragments coming from the ROS into a full event.

### IV. The Read Out Driver Board

The ROD (figure 3) has the form factor of the VME 64x 6U board and is equipped with two VIRTEX II XILINX FPGAs, labelled as VME FPGA and ROD FPGA. The board also hosts an ARM7 microcontroller, the TTCrq receiver, the S-Link transmitter and the two deserializers (RX SerDes) that receive data via RODbus backplane from the RX/SL boards.

The main task of the VME FPGA is to interface the whole board with the VMEbus; the VME FPGA allows a user to access the ROD FPGA memory locations and configuration registers and to read the microcontroller’s
data. The *VME FPGA*’s clock is obtained from an on-
board 40 MHz oscillator multiplied by 2 by the internal
Digital Clock Manager.

The *ROD FPGA* performs the *event building* algorithm
on data transmitted by the *RX/SL* boards. The *ROD FPGA*
also hosts registers for the configuration and control of the
event builder engine. In the same fashion as the *VME
FPGA*, the *ROD FPGA* clock is obtained multiplying by 2
the 40 MHz board clock. The *ROD FPGA* receives 48-bit
words and the recovered 40 MHz clock from each *RX
SerDes*. It is also interfaced with the *TTCrq* module - from
which it receives the *TTC* timing signals and the 40 MHz
LHC’s clock - and to the S-Link transmitter, that is fed by
a 40 MHz clock derived by the 80 MHz internal clock.

The *VME FPGA* is the *Master* of the serial link,
managing both the write (for data and for address) and
read operations. As a consequence, the *ROD FPGA* can
transmit data only if the *VME FPGA* has previously
requested them. The serial protocol allows the user to set
once an 8-bit target address and then to perform an
arbitrary number of 32-bit read or write accesses to the
selected location in the *ROD FPGA*.

The main task of the ARM7 microcontroller is to
program the *TTCrq* receiver, via *I²C* registers. This makes
it possible to access all the *TTCrq* registers, both for
configuration and monitoring purposes. The
microcontroller also allows reading, via the internal ADC,
the three power supplies on the ROD board (5V, 3.3V,
1.5V). The power supply and temperature on the *RODbus*
are acquired from a remote ADC installed on the
backplane via an *I²C* bus. The microcontroller’s output
data can be read via a RS232 port or can be redirected on
the *VMEbus*, through a 16-bit parallel bus handled by the
*VME FPGA*.

The ROD board is the meeting point of trigger signals
and different readout data streams from the Muon Barrel
Spectrometer. Besides the internal 80 MHz FPGA clocks,
the 40 MHz LHC clock, the two 40 MHz SerDes clocks
and the 40 MHz S-Link clock run all over the board. Even
if these clock signals have the same frequency, they have
an unpredictable phase relationship and should be handled
as domains asynchronous to each other. All these clocks
are present in the *ROD FPGA*, which is the most complex
and critical section of the board. In order to decouple the
clock domains and to guarantee their coexistence on the
*ROD FPGA*, FIFO memories have been extensively used.

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The main algorithm of the *Event Builder Engine* is shown
in figure 6. The *Event Builder Engine* has been
designed as a cluster of Finite State Machines, in order to
guarantee real-time performance.

The *ROD MUON FRAME* produced by the engine is made
of 32-bit words [9]. The frame starts with a *ROD Header*
(pertinent to a specific EVID value), includes as a
payload the frames coming from the *RX/SL* boards and
ends with a *Footer* containing status and error flags.

The received *RX/SL* data are formatted in frames that
are made of a *RX Header*, a certain number of data words
(payload) and a *Footer*. The *Header* contains the EVID and
BCID of the event. The *Footer* contains a control code.
Every **ROD Muon Frame** is relative to a specific EVID value received by the TTC. The **Event Builder Engine** checks the empty flag of the EVID FIFO and waits for a EVID to be processed.

When an EVID is available, the **Event Builder engine** starts writing a valid header into the output S-Link FIFO. The **Header** contains nine control words, such as the **Start of Frame**, the board identifier code and information about the current EVID and BCID value.

Then the **Event Builder Engine** waits for data from the **RX/SL** boards. As in the previous step, the **Event Builder Engine** checks the empty flag of each SerDes FIFO. The received RX frames are parsed to find a **Header**. If the frame is correctly formatted and the embedded EVID and BCID match the current one, it is appended to the ROD frame. The ROD event builder does not inspect the payload of the RX frames: it only counts its total length.

The ROD frame is closed by a **Footer**, containing status words, error flags, the total word count and the elapsed time to build the frame. Then the **Event Builder Engine** restarts and waits for a new EVID value.

The timing information written in the ROD Frame Footer allow us to perform a real-time analysis on the elapsed time needed to build a frame. Figure 7 shows the histograms of the ROD processing time, as a function of the size of the RX/SL frames. This analysis has proved to be a very useful tool for the fine tuning of the ROD Event Builder Engine, giving us information about the average time to build an event or a timeout occurrence. In the plot, the linearity between the ROD processing time and the size of the RX/SL frame is clearly visible.

A data analysis architecture, based on the Xilinx MicroBlaze embedded microprocessor, is under development in our laboratories in Napoli. It can be downloaded in the ROD FPGA and it has been specifically designed in order to control the Event Builder performance. With this data analysis tool, the status and the timing of the Event Builder FSM can be monitored. Presently, even using such MicroBlaze-based data analysis architecture, about 35% resources in the ROD FPGA are still available for further improvement of the Event Builder logic. The timing performance of the FPGA are unchanged. The Event Builder engine with MicroBlaze is shown in figure 8.
VI. THE COMMISSIONING OF THE READ OUT DRIVERS

The ROD boards have been fully tested in the stand alone mode in L.N.F.N. laboratories in Napoli and then installed at CERN in the USA15 counting room. The RPC ROD crates in the USA15 counting room are shown in Figure 9.

![Figure 9: The RPC ROD crates in the USA15 counting room.](image)

The RODs have been successfully tested also in the ATLAS data acquisition environment. The testbench comprised the entire chain, with a ROD board, RX/SL boards and µCTPI boards, connected via a RODbus backplane. RX frames have been correctly acquired and processed by the ROD which also was in charge to distribute TTC timing signals on the RODbus.

In our tests in the ATLAS DAQ, we did not encounter any errors. The impact on the builder logic of corrupted frames have been evaluated in stand alone mode by writing frames with missing or wrong fields in the SerDes FIFOs.

The boards have been successfully used in the ATLAS commissioning runs. In this phase, several millions cosmic muons have been acquired through the Read-Out Driver without any failure of the event building logic. During several tests of the DAQ system with random triggers, a L1A rate of 100 KHz has been reached, thus fulfilling the ATLAS specifications for the L1A rate.

VII. CONCLUSIONS

We summarized the design and the development of the ROD board for the RPC read-out system of the ATLAS muon spectrometer. The ROD verifies their logical and syntactical coherence and builds a Frame which is then transmitted on optical fibre to the next level of the DAQ system.

The framing engine fulfils all the ATLAS requirements. Additional features have been designed in order to allow the user to obtain information about events, errors occurred and to check the internal status of the hardware. Some specific fields have also been included in the ROD frame, in order to perform timing analysis on the ROD Event Builder performance. A data analysis architecture, based on the Xilinx MicroBlaze embedded microprocessor, presently being developed.

The RODs have been tested and installed in the ATLAS USA15 counting room in the early 2008. They have been successfully used in the ATLAS commissioning runs and several millions of cosmic muons have been acquired without any failure.

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WEDNESDAY 17 SEPTEMBER 2008

PARALLEL SESSION B3

MACHINE–EXPERIMENTS, BCM
Fast Beam Conditions Monitoring (BCM1F) for CMS

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Abstract

The CMS Beam Conditions and Radiation Monitoring System (BRM) \cite{1} is composed of different subsystems that perform monitoring of, as well as providing the CMS detector protection from, adverse beam conditions inside and around the CMS experiment.

This paper presents the Fast Beam Conditions Monitoring subsystem (BCM1F), which is designed for fast flux monitoring based on bunch-by-bunch measurements of both beam halo and collision product contributions from the LHC beam. The BCM1F is located inside the CMS pixel detector volume close to the beam-pipe and provides real-time information. The detector uses sCVD (single-crystal Chemical Vapor Deposition) diamond sensors \cite{2} and radiation hard front-end electronics, along with an analog optical readout of the signals.

I. INTRODUCTION

The CMS experiment sits in an unprecedentedly high radiation field and much effort has gone into the design and construction of systems with very high radiation tolerance. The LHC is designed to run with 362MJ of stored energy in one beam and with proton intensities in excess of $10^{14}$ per beam. Even very small fractional losses of this beam can cause serious damage to detector elements.

Whilst the LHC itself has extensive instrumentation designed for machine protection, CMS requirements dictate that CMS must be able to detect beam-related problems as they develop and to assert beam aborts if required. In addition, CMS must be able to log data and perform post-mortem analyses of accidents to understand the accumulated dosage and potential longer term damage to the detector elements. To this end, CMS has implemented within the BRM project, 6 independent and complimentary systems designed to either initiate LHC beam aborts and/or CMS equipment control, or provide fast beam/detector optimisations and diagnostics. Given the nominal LHC collision frequency of 40MHz, the CMS protection mechanisms must be sensitive to very fast changes in beam conditions; the BRM systems have been implemented so to detect changes at the 25ns level, though the initially deployed protection systems will react within times of order $3-40\mu$s.

The BCM1F is one of the faster monitoring systems of the CMS BRM, and is designed to provide real-time fast diagnosis of beam conditions with readout able to resolve the sub-bunch structure.

II. SYSTEM OVERVIEW

The BCM1F uses sensor and electronics that are fast enough to match beam abort scenarios, and small enough to be inserted into areas close to key detector components without adding substantial material or services.

The system is based of four sCVD diamonds, each $5 \times 5 \times 0.5 \text{mm}^3$, positioned on either side of the IP at Z values of $\pm 1.8 \text{m}$ close to the beam pipe and the pixel detectors at a radius of 4.5cm (Figure 1).

![Compact Muon Solenoid](image)

Figure 1: BCM1F locations

The BCM1F diamonds are arranged on the X and Y axes. The purpose of the BCM1F is, as a diagnostic tool, to be able to flag problematic beam conditions resulting in “bursts” of beam loss over very short periods of time. Such beam losses are expected to be one of the critical damage scenarios for the CMS detector systems \cite{3}. The location for the BCM1F is close to the optimal position in terms of timing separation between ingoing and outgoing particles from the IP (i.e. 6,25ns from the IP). The gated rate information from the BCM1F should therefore give a very good handle on the comparative rate of background from beam halo to that from luminosity products.
The sensor is connected to the JK16 radiation hard amplifier [4], after which the signal is transmitted to the counting room (Figure 2) over an analog optical link built from the CMS tracker optical components [5]. The back end readout produces rate, multiplicity, timing and coincidence information independently of the CMS DAQ. However, there is the possibility to feed information into the event stream via a standard CMS SLINK [6].

A. sCVD Diamond Sensors

A number of outstanding properties like its low leakage current and fast charge collection time, fast signal and low capacitance contributing to high SNR, in addition to their physical dimensions and radiation hardiness, make the CVD diamonds most competitive for the locations close to the interaction region than any other type of detector. The sensor concept and layout is similar to the silicon detectors: two metallization pads, deposited on the opposite surfaces of the crystal, are used to apply the electric field and to collect ionization currents when charged particles pass through. Further, there is no need for any cooling of the diamonds since there is no reverse annealing damage effect as seen in silicon-based detectors.

The majority of actual developments [7,8] are based on polycrystalline CVD samples, but recent improvement in the quality and size of single crystals in conjunction with its superior electrical properties (table 1), determine the choice of the sensor for the CMS detector.

<table>
<thead>
<tr>
<th>PROPERTY</th>
<th>Polycrystalline CVD diamond</th>
<th>Single crystal CVD diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hole mobility (cm²/Vs)</td>
<td>1,000</td>
<td>3,800</td>
</tr>
<tr>
<td>Electron mobility (cm²/Vs)</td>
<td>1,800</td>
<td>4,500</td>
</tr>
<tr>
<td>Carrier lifetime (ns)</td>
<td>~1-10</td>
<td>~2,000</td>
</tr>
<tr>
<td>Voltage breakdown (MV/cm)</td>
<td>~0.5</td>
<td>4</td>
</tr>
<tr>
<td>Charge collection distance (µm)</td>
<td>~250 at 1V/µm field</td>
<td>Thickness limited</td>
</tr>
</tbody>
</table>

The sensors were manufactured by Element Six (now Diamond Detectors) [9] after a few years of research and development in collaboration with the RD42 [10] project.

B. Front-end Electronics

In addition to the radiation hardness, the detector locations have constrained the front-end layout, readout, monitoring, powering and test facilities.

1) Amplifier:

BCM1F amplifier (JK16) is the FE part of an ASIC [4] developed for readout of silicon strip detectors. The chip is fabricated in a commercial 0.25µm CMOS technology hardened by layout techniques [11].

Each of the 16 channels (Figure 3) comprises a fast transimpedance preamplifier working with an active feedback loop and an amplifier-integrator stage providing 20 ns peaking time.

2) Optical Readout:

As mentioned above, the tracker analog optical chain is used to deliver detector signals to the S1 counting room (Figure 2). The JK16 single ended output is AC coupled to the custom-designed laser driver ASIC (LLD) [12], which modulates the edge-emitting laser diode drive current. Single fibers from the pigtailed lasers are connected at the periphery of the CMS Silicon Strip Tracker via single-way connectors to a fan-in, which merges single fibers into a 12-fiber ribbon. There is a second break-point within the CMS detector where the transition to a rugged multi-ribbon cable (8x12-fiber ribbons/cable) is made via 12-channel array connectors. In the
counting room each ribbon connects directly to a 12-channel analog optical receiver NGK.

Due to the frontend envelope limits 25×29×15mm³, the piggy-back architecture was employed to interconnect, supply and mount the assembly (Figure 4) of the sensor-amplifier and the analog optical hybrid (AOH) on the carriage L-shape. Minor modifications were done to the AOH board to allow opposite mounting orientation of the laser diode imposed by the minimum bending radius of the pigtail fibers. Unlike the Tracker configuration the AOH gains and laser diode bias cannot be programmed via an I²C interface. Hence, a lot of attention was paid to choose the input polarity and laser bias setting to preserve the dynamic range of the receiver side as well as taking into account heat and radiation impacts on the AOH performance.

C. Patch Panels and Back-end Electronics

Two sets of patch panels were implemented. In the counting room, a 4U chassis houses the PPS1 patch panels which combine and filter high and low voltage, as well as the test pulse facility in one multi-service 8 twisted pair copper cable. On the tracker bulkhead, the PP0 patch panel is used to re-arrange power supplies lines, decouple and regenerate the test-pulse input for each detector.

The CMS tracker 12-channel analog opto-receiver module is used for the BCM1F. Then, signals are fan-out to trigger, time and waveform digitizers.

A general purpose multi-hit TDC with 20-bit resolution and 0.8ns LSB is used to measure the time intervals from different sensors, as well as between ingoing beam particles and outgoing interaction products.

In addition, the BCM1F outputs are sampled at 500MHz by 8-bit resolution flash ADC. The module can be triggered externally or locally if any of digitized inputs exceeds programmable threshold. Upon triggering, the detector data, which is continuously written in a circular memory buffer, freezes the event location for further readout via VME or optical link. Each channel has 2 MSamples memory depth, thus it can capture up to 45 consecutive orbits in continuous sampling mode.

80MHz by a 10-bit ADC and processed by applying algorithms for pedestal and common mode noise subtraction. The module can generate internal and/or external triggers based on coincidence logic with any of the digitized inputs. The TTC-Rx ASIC provides synchronization with the experiment timing and the data is transmitted to the CMS data acquisition system via the S-LINK64 [6] transmitter mezzanine card at a maximum rate of 400 MB/sec.

III. DETECTOR TEST RESULTS

The assembled front-end modules were tested with Sr90 source. Figure 6 shows measured pedestals and pulse height distributions collected at different bias voltages. The pedestal distributions (centred on 0V) are uniform and with good signal to noise separation. At a field of 0.23V/µm field (110V bias for 480µm thickness) the sensor reaches the maximum signal, providing signal-to-noise ratio of 26.

Figure 6: BCM1F module pedestals and pulse height distributions

Figure 7 presents the observed leakage current, the mean and most probable values of the collected charge per MIP as a function of bias voltage. On this plot, the leakage current is dominated by the test setup and passive components on the front-end board.

IV. RADIATION TOLERANCE STUDIES

The radiation hardness of single crystal sensors has been evaluated at PSI-Villigen facility and CERN in 2007. Two sCVD (S1 and S2) were exposed to a 60MeV proton beam with an integrated fluence of about 3×10¹⁴ p/cm². The crystal dimensions and radiation doses are listed in Table 2.
The irradiated samples performance was measured and compared with similar non-irradiated sCVD crystal and the test results are presented in Figure 8. Important signal losses, as well as, some decrease in noise were observed. The 1MIP response has decreased by roughly 80% and signal to noise efficiency degraded from 26 to 7 at a much higher electric field in the crystal.

<table>
<thead>
<tr>
<th>Sensor</th>
<th>Thickness</th>
<th>Size</th>
<th>Radiation dose @60MeV</th>
<th>MIP equiv. radiation dose</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>480μm</td>
<td>4×4 mm²</td>
<td>3×10¹⁵ p/cm²</td>
<td>17.5×10¹⁴ MIP/cm²</td>
</tr>
<tr>
<td>S2</td>
<td>488μm</td>
<td>4×4 mm²</td>
<td>3×10¹⁵ p/cm²</td>
<td>17.5×10¹⁴ MIP/cm²</td>
</tr>
<tr>
<td>S7</td>
<td>465μm</td>
<td>5×5 mm²</td>
<td>none</td>
<td>none</td>
</tr>
</tbody>
</table>

Previous studies of the CVD diamond radiation hardness [13,14] have been done at 24GeV and 26MeV proton beams. The results presented here tend to support the hypothesis of enhanced damage to particle of low energies.

V. INSTALLATION AND FIRST LHC BEAM HITS

The BCM1F assemblies were successfully installed at the beginning of August 2008 (Figure 9), and all 8 modules were fully tested and characterised prior to installation in CMS and were fully functional after installation.

Several hundred hits were collected from the very first particles which have been circulated in the CERN LHC on September 10, 2008.

The oscilloscope screenshot (Figure 10) shows the analog sum of 4 BCM1F outputs from either side of the IP, where the trigger was from the beam pickup electrode installed 175m upstream of the IP. The sensor output amplitude corresponds to a 1 MIP response and the time difference between the pulses is consistent with the particle time of flight from left to right side detectors.

The signal height distribution from one of the BCM1F sensors is shown in Figure 11. One can mention very good signal-noise separation in spite of low hit number, as well as the rough distribution shape.

VI. CONCLUSION

A general overview of the sCVD diamond based fast beam condition monitor was presented. All parts of the system were successfully installed in their final positions and exhaustively tested through implemented facilities. The detectors and associated readout chain demonstrated excellent performance in real working conditions at CMS during very first days of the LHC operation.
VII. REFERENCES


The ATLAS Beam Condition Monitor Commissioning

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Abstract

The ATLAS Beam Condition Monitor (BCM) based on radiation hard pCVD diamond sensors and event-by-event measurements of environment close to interaction point (z=±184 cm, r=5.5 cm) has been installed in the Pixel detector since early 2008 and together with the Pixel detector in the ATLAS cavern since June 2008. The sensors and front end electronics were shown to withstand 50 Mrad and $10^{15}$ particles/cm² expected in LHC lifetime. Recently the full readout chain, partly made of radiation tolerant electronics, still inside of the ATLAS spectrometer and partly in the electronics room, was completed and the system was operated in time of the first LHC single beams and is ready now for the first collisions which will follow after the LHC repair.

I. INTRODUCTION

Potential detector damage resulting from abnormal beam conditions could damage ATLAS Inner Detector which encouraged the implementation of Beam Condition Monitor (BCM) [1] in ATLAS spectrometer. The aim of ATLAS BCM is to monitor the beam conditions and luminosity very close to the ATLAS interaction point, inside the Inner Detector. It consists of 8 detector modules organized in two sets of four modules on each side of the interaction point. The pCVD diamond sensors of each of the BCM modules are located symmetrically around the interaction point at $z=184$ cm and $r=55$ mm and supported on the ATLAS Pixel carbon fibre structure which also serves for the support of BCM supply and signal cables. Figure 1 shows the mechanical mounting and the inside of one of the modules with the diamond sensors and front end electronics visible.

The modules are required to be radiation hard since they will be installed close to interaction point and close to the beam-pipe in the place where expected radiation will reach doses of about 50 Mrad and fluences of about $10^{15}$ particles/cm² in 10 years of operation of ATLAS at nominal luminosity. pCVD diamonds were chosen for their radiation hardness and fast signal response which allows to measure the beam conditions on the bunch by bunch basis. They were also shown to draw only tiny leakage currents allowing for no active cooling which is neither required for the amplifiers that can dissipate the heat by convection to the surrounding Pixel gas volume.

Each BCM module consists of two polycrystalline CVD (Chemical Vapour Deposition) diamond pad sensors mounted on top of each other and connected in parallel [2]. Signals created in the diamond sensors by charged particles are amplified in two stage amplifier build of off-the-shelf components [3] which were chosen for their satisfactory performance after the irradiation. Further away from the interaction point (in radiation less harsh environment) the precise timing information and amplitude is encoded into digital signals sent to the back end electronics based on sophisticated FPGA board. The principle of operation is shown on Figure 2 where interactions at interaction point will cause the appearance of signals in modules on both sides simultaneously (“in time events”) and the background events which will cause time difference between the recorded signals on the two sides of 12.5 ns (“out of time events”), about ½ of the bunch to bunch time spacing due to adequately chosen BCM module locations.

In addition to beam condition monitoring the BCM will provide valuable complementary luminosity monitoring information which could be used for example for correcting the trigger for bunch to bunch luminosity variations. During the LHC early commissioning when the conditions will not yet be stable and the Inner Detector will most likely be switched off, the BCM might be the first detector system to report proton-proton collisions inside ATLAS spectrometer.
A. Beam Accidents simulation and past experiences

The ATLAS experiment is rated to be as the ‘safest’ of all interaction points in terms of possible beam failure scenarios because it is located furthest away from beam extraction and injection points. ATLAS is also shielded with so called Target Absorber Secondaries (TAS) collimators which are 1.8m long copper block located at z=±18m from the interaction point and are intended to protect the inner triplet of cryogenic quadrupoles from excessive heat load due to particles from collisions. Additionally, TAS also protects the Inner Detector from a variety of beam failures. The beam interlock system (BIS) at LHC comprises two redundant optical loops per beam, which transport BeamPermit signal around the LHC ring. In each insertion region two beam interlock controllers (BIC) are used to make a logical AND of many UserPermit signals provided by user systems (experiment BCMs, machine beam loss or beam position monitors...). If BeamPermit signal is set to false the beam dump is initiated or beam is not allowed to be injected from SPS. The extraction of beam is triggered by the BIS and is completed within 270 μs after the UserPermit signal was removed at the BIC. Each user system is connected to BIS through user interface CIBU (Controls-Interlocks-Beam-User), which takes the UserPermit signal and transmits it to the nearest BIC. The most likely beam losses are due to failures or wrong settings in the magnet and powering system with about 8000 magnets powered in 1700 electrical circuits. Beam losses occur at different time scales. They can happen either in a single-turn (or a fraction of turn) with a sudden beam loss or during several turns resulting in progressive losses. Figure 3 shows possible scenario of a beam hitting a collimator and causing showers that can be a potential risk to the Inner Detector.

Figure 1: Four ATLAS BCM modules installed on the side-C of the ATLAS Pixel system support frame (upper picture). The beam-pipe going through the support structure as well as Pixel detector in the background can also be seen. The lower two pictures show BCM module soldered close (lower left picture) and BCM module prior to installation of the covers where pCVD diamond sensors and two stage amplifier is visible (lower right picture).

Figure 2: Principle of operation of Beam Condition Monitor. In case of the normal proton-proton interaction at interaction point (green) secondary particles would reach both sides of BCM system simultaneously. In the case of anomalous event such as proton hitting a collimator (red) one side of BCM system would detect secondary particles before the other. The $z = ±184$cm defines the time difference between the two sides to ~12.5 ns almost exactly ½ of the time interval between two consecutive LHC bunches.

Figure 3: An example of one of the possible scenarios, where beam hitting a TAS collimator at beam injection causes a shower in Inner Detector.

LHC will circulate 2808 bunches per colliding beam, each bunch consisting of $1.1 \times 10^{11}$ protons at energy of 7 TeV – about 200-times more energy stored in beams compared to maximum value in previous accelerators like HERA or Tevatron. Already at Tevatron accidents happened such as the one depicted in Figure 4 where the proton beam caused damage to a collimator due to misfiring kicker magnet.
II. THE ATLAS BCM SYSTEM

Figure 5: Schematic view of locations of BCM detector modules within ATLAS Inner Detector.

Figure 5 shows schematic view of positions of the 8 BCM modules inside the ATLAS Inner Detector. The location is conveniently chosen to make the time of flight between the two sides approximately $\frac{1}{2}$ of the bunch to bunch spacing in LHC.

A. Detector module

The polycrystalline CVD diamond sensors of $1 \text{ cm} \times 1 \text{ cm}$ size and 500 $\mu\text{m}$ thickness were developed by a collaboration of RD42 [5] and Element Six Ltd. [6] (later named Diamond Detectors Ltd.). They were proven to be radiation hard and to produce very fast signals (rise time < 1 ns, signal width ~2 ns). They are also attractive choice due to low leakage currents even after irradiation which does not exceed 1 nA/cm$^2$ thus no active cooling is required to cool the sensors. Two pad sensors are assembled back to back on a Al$_2$O$_3$ ceramic baseboard which brings high voltage ($\pm1000\text{V}$) to the lower surface of the bottom diamond sensor and to the pad on the side which is used to connect the high voltage to the upper side of the top diamond sensor through several bond wires. The middle surfaces of the two sensors are conductively glued together with small pieces of ceramic distance holders and connected to the signal line on the ceramic baseboard through multiple bonds (see Figure 7). All parts are glued together with thermoplastic conductive adhesive pads (Staystik 571, a material proven to be radiation hard).

Ceramic module with two diamond sensors was assembled into the front end electronics box [3] based on commercially available current amplifiers: 500 MHz Agilent MGA-62563 GaAs MMIC and 1 GHz Mini Circuits Gali 52 HBT chips, each providing an amplification of about 20 db. The first stage Agilent amplifier has an excellent noise performance with its noise figure below 1 db in most of its frequency range.

To avoid electrical interference and pick-up each module was closed by soldering covers to each of the three compartments on the upper side (respectively containing two diamond sensors, first stage Agilent amplifier and second stage Gali amplifier, see Figure 6) and the compartment on the lower side containing the LV/HV power cable connector and temperature sensor.

Figure 6: The two pictures show BCM module soldered close (upper picture) and BCM module prior to installation of the covers where pCVD diamond sensors and two stage amplifier is visible (lower picture).

B. The BCM Readout Chain

The ATLAS BCM will measure the arrival times of the signals and their time over threshold (TOT) for each of the 8 modules. These signals will be processed in real-time into rates, trends of rates for individual modules as well as for different logical combinations of signals taking into account also the timing within 25 ns (“in time” and “out of time” signals). The Figure 8 schematically shows the BCM system architecture. BCM system functionality can be summarized as follows:

- LHC Beam Abort. Two redundant signals indicating that beam conditions in ATLAS Inner Detector have reached the beam abort levels are sent to LHC through ATLAS “CIBU” system and will eventually cause that all LHC bunches being dumped in a controlled manner.
• **ATLAS Detector Safety System.** 4 signals are sent to ATLAS DSS, the hardware interlock system, which will allow for the ATLAS Inner Detector components to react in order to protect their hardware.

• **ATLAS Detector Control System.** In less severe cases and in addition to the hardware based DSS the warnings and alarms will be sent also through the ATLAS DCS. More sophisticated information and histograms will also be available through DCS system to ATLAS and LHC control. All recent information from BCM stored in circular buffer of the back end electronics will also be dumped through this channel.

• **ATLAS Level 1 trigger information.** ATLAS BCM will provide also a 9-bit information for the ATLAS Level 1 trigger system, allowing for triggering on topologically interesting events. BCM can provide in real time bunch to bunch luminosity variation information – a valuable input to the trigger system.

• **ATLAS DAQ stream.** Digitized information of signal arrival times and their widths will be stored into special buffer in the ATLAS DAQ data stream. BCM data bits will be also recorded in the trigger data block.

Signals from BCM modules are taken through 14 m (2 m of Gore 41 in the inside and 12 m of Andrew HELIAx FSJI on the outside of the Pixel volume) of coaxial cables to a region with lower radiation where radiation tolerant electronics can be used. This electronics is based on NINO chip [4] designed by CERN-MIC for ALICE RPC detector for time of flight measurement. The NINO ASIC has 8 channels and features differential input amplifier (1 ns peaking time, 25 ps jitter), discriminator and the time over threshold measurement. It is built in radiation tolerant ¼ µm IBM technology. The NINO electronic board first filters (low-pass fourth order filter with bandwidth of ~300MHz) and splits the signals from each of the BCM FE modules into two parts in ratio of approximately 1:11 to increase the dynamic range of the BCM system. These signals are then fed into two input channels of NINO chip. The ground of each BCM channel separately (BCM module, NINO electronics, HV and LV power supply channel) is kept electrically floating with connection only to the Pixel reference ground through a 1kΩ resistor close to BCM modules. The TOT digital outputs of the NINO chip is converted into optical signals using radiation tolerant laser diodes (Mitsubishi FU-427SLD-FV1) and taken with 70 m optical fibres to the ATLAS counting room where they are received by photo diodes (Lightron LP3A4-SNC1) converted to PECL electric levels and fed into two Xilinx ML410 development boards based on Xilinx Vitrex-4 FPGA chip. Optical receiver board also provides monitoring NIM level outputs. Each Xilinx ML410 boards features 8 RocketIO serial input/output channels that will sample signals received at frequencies of 2.56 GHz. The onboard RAM memory banks act as ring buffers to store the BCM signal information for the time of the last several hundreds of LHC bunch crossings. This information will be used for the post-mortem analysis after a potential beam dump. The processed data from the Xilinx ML410 will be sent through ATLAS standard optical link (“S-LINK”) to the ATLAS DAQ system, via Ethernet to the ATLAS DCS system and electrically to the ATLAS interlock (DSS) system.

**Figure 7:** Schematic view of two diamonds assembly onto ceramic board (upper picture). Since modules are mounted under 45° towards the beam-pipe the two diamond sensors are mounted with slight displacement to mimic this. The two pictures show BCM module soldered close (upper picture) and BCM module prior to installation of the covers where pCVD diamond sensors and two stage amplifier is visible (lower picture).

**Figure 8:** Symbolic BCM connectivity diagram.
III. RESULTS OF INSTALLED DETECTORS

Figure 8 shows the measured noise rated sampled at the outputs of the optical receiver (just in front of the signal input into the backend). The measurements show the RMS of the noise to be in the range from 50 mV to 70 mV as expected from the QA measurements [7,8]. Table 1 summarizes these results.

![Figure 8](image_url)

**Figure 9:** Noise rate of individual channels as measured in the pit.

**Table 1:** Summary of RMS noise measured using the detectors as installed in their final position in the pit.

<table>
<thead>
<tr>
<th>Module</th>
<th>Position [Side, (x,y)]</th>
<th>Noise $\sigma$ [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>F410</td>
<td>A, (+x,0)</td>
<td>68.0</td>
</tr>
<tr>
<td>F405</td>
<td>A, (0,+y)</td>
<td>62.6</td>
</tr>
<tr>
<td>F413</td>
<td>A, (-x,0)</td>
<td>60.3</td>
</tr>
<tr>
<td>F404</td>
<td>A, (0,-y)</td>
<td>53.9</td>
</tr>
<tr>
<td>F424</td>
<td>C, (+x,0)</td>
<td>61.0</td>
</tr>
<tr>
<td>F420</td>
<td>C, (0,+y)</td>
<td>56.7</td>
</tr>
<tr>
<td>F422</td>
<td>C, (-x,0)</td>
<td>51.0</td>
</tr>
<tr>
<td>F408</td>
<td>C, (0,-y)</td>
<td>51.3</td>
</tr>
</tbody>
</table>

References


The ATLAS Radiation Dose Measurement System and its Extension to SLHC Experiments

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Abstract

In LHC experiments, a precise measurement of the radiation dose at various detector locations is crucial. In ATLAS, this task is performed by a set of radiation monitors (RADMON) which are able to record Non-Ionising Energy Loss (NIEL), the Total Ionizing Dose (TID) and measure fluences of thermal neutrons. These measurements are vital for understanding the changes in detector performance during ATLAS operation, verifying simulations and optimising the operation scenario. The RADMONs are multi-sensor boards, containing several RadFETs, diodes and DMILL transistors. It is clear that a similar system will be of even greater importance for SLHC environments due to the increased radiation dose.

I. INTRODUCTION

At the design luminosity of $10^{34} \text{cm}^{-2}\text{s}^{-1}$ the experiments at the Large Hadron Collider (LHC) will be exposed to a hostile radiation environment containing charged particles, photons and neutrons. It will be composed of particles from the proton-proton collisions in the interaction point and the products of these particles from their interactions with detector material. While the innermost parts will mainly be exposed to charged hadrons from the primary interactions, secondary neutrons play a more important role in the outer parts [1].

During 10 years of LHC operation, the electronics in the innermost part of the ATLAS detector will accumulate a Total Ionizing Dose (TID) of more than 100 kGy. The Non Ionizing Energy Loss (NIEL) of hadrons will cause bulk damage in silicon equivalent to the fluences of up to $10^{15}$ 1 MeV neutrons per cm$^2$. Monitoring of these quantities is therefore needed from the very beginning with low luminosity running until the end of operation. It will allow to understand and react on changes in the detector performance, predict the lifetime of components that are sensitive to irradiation and hence make an optimisation of the operation possible. Furthermore it will allow to cross-check simulations already at an early stage.

The planned upgrade of the LHC to Super-LHC (SLHC) will result in a luminosity that is ten times higher than the design luminosity of LHC, i.e. $10^{35} \text{cm}^{-2}\text{s}^{-1}$ [2]. TID and NIEL are thus expected to also increase by a factor of ten [3]. It is clear, that in this case monitoring the radiation levels will be even more important but also more demanding.

II. RADIATION MEASUREMENT TECHNIQUES

In the ATLAS experiment the integrated radiation doses are measured using modules that contain different silicon devices. The readout can be done online and the information is made available in the control room. The Total Ionizing Dose in SiO$_2$ is measured with field-effect transistors. Effects due to bulk damage in silicon diodes are used to monitor the Non Ionising Energy Loss. DMILL npn bipolar transistors are sensitive to thermal neutrons and are used to measure their fluence. In order to be sensitive to low doses on the one hand and cover the full dose range during LHC running on the other hand transistors and diodes of different sensitivity are used.

A. TID Measurement

Radiation sensitive p-MOS Field Effect Transistors (RadFET) are used for the TID measurement. Electrons and holes that are created by ionising radiation in the oxide layer of the gate electrode have different mobilities. While the electrons can escape via the gate electrode, the holes are trapped in the SiO$_2$ layer and lead to a charge buildup. The resulting field must be compensated by a higher negative gate voltage $V_G$ to open the channel. The increase of the gate voltage at fixed drain current is thus a measures of the TID. The relation is given by a power law

$$\Delta V_G |_{\text{drain=const}} = a \times (TID)^b$$

where $a$ and $b$ are constants that are obtained from calibration measurements. The RadFETs are operated in unbiased mode, that means no gate voltage is applied during irradiation. Biased mode would mean a faster charge buildup and therefore a higher sensitivity on the one hand but reduced dynamic range on the other hand. It would require continuous operation. In detailed studies the CERN TS-LEA division has selected RadFETs that are best suited for the use in LHC experiments [4, 5]. Following these recommendations three RadFETs of different oxide thickness are chosen to be used in ATLAS [6]. They account for the need of high sensitivity in the beginning as well as capability of the whole dose range:

- high sensitivity, 1.6 µm oxide thickness, mGy sensitivity, up to a few Gy total dose, produced by CNRS LAAS, Toulouse, France
- intermediate, 0.25 µm oxide thickness, tens of kGy total dose, produced by REM Oxford, Ltd.
- low sensitivity, 0.13 µm oxide thickness, 10$^5$ Gy total dose, produced by REM Oxford Ltd.
B. NIEL Measurements

Two methods, which are both based on effects due to bulk damage in silicon, are used to measure the NIEL in silicon: The change of the forward voltage on a p-i-n diode at given forward current and the leakage current increase in a reversed biased, fully depleted epitaxial pad diode.

Bulk damage in a p-i-n diode leads to a reduced minority carrier lifetime and thus to an increase of the resistance. For the first method, the measured quantity is therefore the voltage change when driving a specific current through the diode. Two diodes are used in ATLAS:

- **high sensitivity**: p-i-n diode from CMRP, Wollongong, Australia, \(10^8 \text{n/cm}^2\) to \(2 \times 10^{12} \text{n/cm}^2\)

- **low sensitivity**: photo diode BPW34F from OSRAM, \(10^{12} \text{n/cm}^2\) up to \(10^{15} \text{n/cm}^2\)

The relation between NIEL and voltage change at given forward current is linear over a large range, as shown in Fig. 2. The BPW34F diodes used in ATLAS have been pre-irradiated with \(3 \times 10^{12} \text{n/cm}^2\) in order to start in the linear regime. Like for the RadFETs the irradiation is done in unbiased mode. At higher fluences, as the forward voltage needed for 1 mA current increases, power dissipation which heats the diode during readout starts to influence the measurement. There are ongoing studies that aim to solve this problem and allow usage of these diodes at SLHC fluences. A possibility is the fluence dependent readout current i.e. reducing the readout current at high fluences. Another option is to apply the sequence of current pulses in order to estimate the change in temperature [7].

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(a) High sensitivity CMRP p-i-n diode.

(b) Low sensitivity BPW34F diode.

Figure 2: Response curves of the high (a) and low (b) sensitivity p-i-n diodes that are used in the ATLAS experiment. The forward voltages at 1 mA forward current are plotted versus the equivalent fluence for irradiation in different radiation environments. Taken from [5].
For the second method to measure the NIEL, a diode is used in reversed biased mode. The leakage current increase is proportional to the NIEL \cite{8}. The 1 MeV neutron equivalent fluence is given by

$$\Phi_{\text{eq}} = \frac{\Delta I_{\text{leakage}}}{\alpha(t, T) \times V}.$$  

$\alpha(t, T)$ is the well measured damage constant which is independent of the silicon type but sensitive to temperature changes and annealing. $V$ denotes the depleted volume. It has to be kept constant by fully depleting the diode also after irradiation. In ATLAS a $0.5 \times 0.5 \text{cm}^2$ silicon pad diode with guard ring structure from C\textit{I}S, Erfurt, Germany is used. Its active thickness of $0.25 \mu\text{m}$ allows depletion with less than $30 \text{V}$ for the whole lifetime of the experiment. Annealing studies have shown, that it can also be used for fluences greater than $10^{15} \text{n/cm}^2$.

![Graph showing leakage current versus fluence](image)

**Figure 3:** Leakage current of the fully depleted epitaxial diode versus the equivalent fluence. The measurement was done immediately after irradiation. The quoted damage constant $\alpha$ is for the unannealed case.

### C. Thermal Neutron Fluence Measurement

DMILL npn bipolar transistors are used in the front-end electronics of the ATLAS Inner Detector. Their current emitter gain factor $\beta = I_c/I_b$ changes with irradiation. In order to understand the degradation in electronics performance it is therefore important to monitor this quantity.

Displacement damage in DMILL transistors is caused by fast hadrons as well as thermal neutrons. The energy of the thermal neutrons is not sufficient to directly cause the displacement damage. Rather it is due to the products of the process $^{10}\text{B(n, }\alpha)^{7}\text{Li}$ as pointed out in \cite{9}. It was also shown in \cite{9}, that the degradation of $\beta$ resulting from irradiation with fast hadrons and thermal neutrons can be written as

$$\frac{1}{\Delta \beta} = k_T \times \Phi_T + k_{\text{eq}} \times \Phi_{\text{eq}},$$

where $\Phi_{\text{eq}}$ is the 1 MeV equivalent fluence and $\Phi_T$ the fluence of thermal neutrons. $k_{\text{eq}}$ and $k_T$ refer to the corresponding damage factors that are determined from calibration measurements as shown in Fig. 4. Since $\Phi_{\text{eq}}$ is obtained from measurements with diodes as explained previously, DMILL transistors allow to determine the thermal neutron fluence.

![Graph showing change in base current](image)

**Figure 4:** Response of the DMILL bipolar transistor. Plotted is the change in base current at $10 \mu\text{A}$ collector current as a function of the fluence. For protons, fast neutrons and for the admixture (fast+thermal, $\Phi_{\text{fast}}/\Phi_{\text{thermal}} \approx 0.7$) fluence is in 1 MeV neutron equivalent. For thermal neutrons the $x$-axis represents the fluence of thermal neutrons.

### III. The Radiation Monitor Hybrid

The highest radiation levels will occur in the ATLAS Inner Detector around the pp-collision point. Due to the large range of doses all sensors listed in the previous sections are used in this part of the detector to cover the entire range of expected doses and provide a high level of redundancy. Three different RadFETs, two different p-i-n diodes, one epitaxial diode and two equivalent DMILL bipolar transistors are combined to one module that also includes an NTC sensor.

Mainly due to the very uncertain temperature conditions at some locations in the Inner Detector, where the expected temperatures are between $-20^\circ \text{C}$ and $+20^\circ \text{C}$, the modules were made of ceramics. They provide mechanical support and electrical connection for the sensors and the bottom side of the ceramics is covered with a thin layer of material with electrical resistance $R = 320 \Omega$ which serves as heater. The heater will be used to keep the board at a constant temperature a few degrees above $20^\circ \text{C}$.

Outside the Inner Detector the ranges of expected dose levels are smaller. Therefore TID and NIEL damage will be measured with modules that contain only two sensors: the most sensitive RadFET and the most sensitive p-i-n diode. It also contains a NTC sensor but no resistive heating.

There are 14 modules placed in the Inner Detector. Simplified modules are located in the calorimeters (6 in Tile and 18 in LAr), in the muon forward detectors (16) and in the so called Patch-Panel-2 area (10) which is in the muon barrel region.

### IV. Readout

Readout of all modules is done online. Standard ATLAS components are used for this purpose to ensure full compati-
bility with the overall ATLAS Detector Control System (DCS) and to simplify the integration. For the readout Embedded Local Monitor Boards (ELMB) are used. They host 64 12-bit ADC channels (0–4.5 V) with the conversion frequency ranging from 2 – 100 Hz [10]. 16 channel 12-bit ELMB-DACs [11] are used as current source. The maximum output current is 20 mA per channel and the maximum output voltage of a DAC channel can be up to 30 V. Up to four DAC boards can be connected to and controlled by an ELMB. Every 15 to 60 minutes a read out cycle will be carried out. It comprises: 1. applying the chosen bias to each sensor, 2. waiting for 50 ms to 1000 ms depending on the sensor type and 3. reading out the voltage or current. The sensors will be biased only during the readout cycles which are much shorter than the total exposure time. Irradiation can therefore be assumed to be taken out in unbiased mode.

Communication between the computer that runs the DCS software and the ELMBs is done via CAN bus. The DCS software is PVSS [12], a commercial SCADA software that is used by all LHC experiments. System status and online values for doses can be monitored from the ATLAS control room. All values are archived in an online database that can easily be queried from the control room. When doses have reached a significant value, the archived data will be used for a detailed offline analysis. This will allow a precise validation of existing simulations. Correlations between doses and luminosity will be determined and used to predict the expected dose levels at SLHC.

V. TESTS IN A MIXED PARTICLE ENVIRONMENT

At the CERN-PS 23 GeV protons of the primary beam can be directed to an irradiation facility called IRRAD1. During the operation the protons produce a radiation field of secondary particles consisting of charged hadrons, neutrons and photons. This low dose rate mixed particle environment can be used for irradiation tests and is called IRRAD6.

Two Inner Detector style RADMON modules where placed in the IRRAD6 environment for more than three month.1 As in ATLAS, the readout of the sensors on the two modules is done with one ELMB and two ELMB-DACs. The aim is to perform a long term study under realistic conditions concerning both the mixed particle environment and the readout chain.

The number of protons that are delivered to the irradiation facility is determined by a Secondary Emission Counter (SEC). In a previous study that has been carried out at the IRRAD6 conversion factors have been obtained that allow to specify the TID and NIEL rates from the SEC measurement [13]. A 50 % uncertainty is quoted for this conversion factors which also takes into account that the beamline has changed in the meantime [14]. For the dose measurements of the ATLAS RADMON modules the uncertainty is assumed to be 20 % [4, 14].

Figure 5 shows TID and NIEL values versus time as they were obtained from RadFET and p-i-n diode measurements respectively. The response shapes of the RadFETs and p-i-n diodes compare well to the SEC result. One has to consider that the SEC does neither account for the dose rates due to activation of the environment nor does annealing play any role for it. Both effects can be observed in the plateau regions, i.e. when there was no beam. From the inserts in Figure 5 it can be seen that the sensitivity of the system is about 10^−3 Gy for TID measurement and 10^9 n/cm^2 for measurements of NIEL.

The response of the high sensitivity RadFET (LAAS) is reduced for protons as can be seen from the calibration curves in Fig. 1(a). The IRRAD6 environment is proton rich and therefore the calibration constants have to be rescaled for this very special case as it was done for the data shown in Fig. 5(b).

VI. CONCLUSIONS

In ATLAS, especially in the Inner Detector, the radiation environment will be very hostile during LHC running. It is therefore essential to monitor the accumulated doses in order to understand and react on changes in the detector performance. Furthermore will the monitoring allow to check simulations and to determine the correlation between dose rate and luminosity. This will be of great importance to predict the expected doses at SLHC. The same method might be used to monitor the dose levels beyond the dynamic range of available sensors.

A set of RadFETs and diodes has been selected as monitoring devices for integrated Total Ionizing Dose and Non Ionizing Energy Loss in the ATLAS detector respectively. Sensors of different sensitivity ensure that measurements will be possible from very low doses up to the maximal doses expected in the experiments lifetime. Furthermore, DMILL bipolar transistors are used to monitor their degradation with irradiation. Together with NIEL measurements from the diodes, they allow to determine the thermal neutron fluence. Extending the maximum doses that can be measured with RadFETs and diodes to SLHC like values is possible but detailed studies and measurements have to be done. The ideas include thinner active volumes, extension of calibrations to non linear regions, usage of higher depletion voltages etc.

Two kinds of hybrid modules have been developed and installed in the ATLAS detector: One for the Inner Detector containing sensors for different dose ranges and a simplified type with only one RadFET and one diode for the other detector parts. The system is fully operational and all modules are read out online in the context of the ATLAS Detector Control System.

A mixed particle environment at the CERN-PS is used for a long term irradiation study under realistic conditions. It proves the applicability of the sensors to such an environment as well as the functionality and stability of the read out chain.

VII. ACKNOWLEDGMENTS

The authors would very much like to thank Maurice Glaser for making the test in the IRRAD6 environment possible. Many thanks to him and Federico Ravotti for sharing their great expertise in the field of radiation sensors and for their help understanding the collected data.

1 At the time of writing the irradiation is still ongoing.
Figure 5: Long term irradiation measurements of the TID (a) and NIEL (b) in the IRRAD6 mixed particle environment. In (a) measurements with the LAAS 1.6 \mu m and the REM 0.25 \mu m RadFET are plotted. High sensitivity LAAS RadFET can be used only up to about 10 Gy. NIEL measurements with both p-i-n diodes in use (CMRP and BPW34F) are shown in (b) where calibration for the CMRP is only valid for values below $2 \times 10^{12} \text{n/cm}^2$. The insert shows the high sensitivity of the CMRP. Also shown are the values obtained by converting the SEC proton counting. The plotted SEC measurement only starts after about five days because before that the beam conditions were very uncertain and the conversion factors cannot be applied for this part.

REFERENCES


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Parallel Session B4

Interconnects
The Origami Chip-on-Sensor Concept for Low-Mass Readout of Double-Sided Silicon Detectors

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Abstract

Modern front-end amplifiers for silicon strip detectors offer fast shaping but consequently are susceptible to input capacitance which is the main contribution to the noise figure. Hence, the amplifier must be close to the sensor which is not an issue at LHC, but a major concern at material budget sensitive experiments such as Belle or the ILC detector.

We present a design of a silicon detector module with double-sided readout where thinned front-end chips are aligned on one side of the sensor which allows efficient cooling using just a single, thin aluminum pipe. The connection to the other sensor side is established by thin kapton circuits wrapped around the edge – hence the nickname origami.

I. INTRODUCTION

The current Silicon Vertex Detector (SVD2)\textsuperscript{[1]} of the Belle experiment at KEK (Tsukuba, Japan) is composed of four layers with a total of 246 double-sided silicon sensors as shown in fig. 1. Its polar acceptance extends from $17^\circ$ to $150^\circ$, which allows to place the readout electronics outside of that region. This is important as the KEK-B is a low-energy machine ($8 \text{ GeV}$ electrons on $3.5 \text{ GeV}$ protons) which requires careful consideration of material in order to minimize multiple scattering. Up to three ganged (concatenated) silicon sensors are read out by the VA1TA\textsuperscript{[2]} front-end amplifier which has a low noise figure of $\text{ENC} = 180 \text{ e} + 7.5 \text{ e/pF}$ due to its slow shaping time of 800 ns.

II. APV25

The APV25\textsuperscript{[3]} readout chip, originally developed for CMS at CERN, was identified to meet all the requirements of the Silicon Vertex Detector of SuperBelle. It has a shaping time of 50 ns and thus intrinsically reduces the occupancy by a factor of 16 (a factor of 12.5 was found by measurement as one has to consider the actual shaping waveform as well as thresholds). Moreover, it has a 192-cell deep pipeline which allows continuous measurement without dead time. Due to the interpretation of 3-bit symbols on the trigger line, there is in fact a very small dead time of 3 clock cycles, or 75 ns, which is however irrelevant in the experiment.

The APV25 is designed for operation at 40 MHz and offers the possibility to read out several sampled values along the shaping curve with each trigger. By means of post-processing, this feature allows to determine the actual particle timing with a precision of a few nanoseconds\textsuperscript{[4]} and will also be implemented in SuperBelle using look-up tables in FPGA devices.

Unfortunately, compared to the slow VA1TA chip, a higher noise figure of $\text{ENC} = 250 \text{ e} + 36 \text{ e/pF}$ inevitably comes along with the faster shaping. Hence, one has to minimize the capacitive load at the front-end in order to keep the noise as low as possible. While the signal size is given by the canonical 300 $\mu$m thickness of the silicon sensors, it is the noise that essentially determines the resulting signal-to-noise ratio (SNR). Thus, if fast shaping is desired, we conclude that the reduction of capacitance is the only practical way to increase the SNR, which influences spatial precision and ultimately the impact parameter resolution. In practice, a minimum cluster SNR (sum of cluster signal divided by the square sum of RMS noise of all strips in the cluster) of ten is considered mandatory for reasonable operation of the silicon detector.
III. LADDER GEOMETRY

Ganging of sensors is possible in the current SVD2 as the noise slope of the VTA chip is shallow. In the innermost layer, there are just two sensors per ladder, which are individually read out from either side. As the ladders get longer with increasing radius, readout is still done at the edges in the same way as in the innermost layer while sensors are ganged (concatenated). This results in spatial ambiguities but allows the same number of readout chips for each ladder and avoids any readout electronics inside the active volume. In case of the long strip dimension, ganging is simply accomplished by connecting adjacent sensors with bond wires. For the opposite side, with strips orthogonal to the ladder axis, thin flex circuits are used to contact the same strip of each sensor to a single readout channel. The layer four ladders are composed of six silicon detectors of which three are ganged and read out from either side. Fig 2 shows a photograph of all four ladder types.

In SVD2, the outermost layer is located at a radius of 8.9 cm. Despite of ganging, the minimum cluster SNR is in the order of 13 due to the slow shaping. For SuperBelle, the SVD shall extend to significantly larger radii (≈ 14 cm) and consist of five layers, where the innermost is a double layer and will probably be equipped with DEPFET pixel detectors [5].

IV. GANGED SENSORS WITH APV25

As indicated in the previous section, the noise figure of the APV25 is significantly influenced by the load capacitance presented at its input which is the sum of the total strip capacitance and the intermediate connections (flex circuits). Hence we can suspect that ganging of sensors would lead to a poor SNR, especially in larger structures than the current SVD2.

Using prototype double-sided silicon sensors made from 4” wafers for the future SVD, we built a module with two ganged sensors read out by four APV25 chips on each side. In order to compare the SNR of a single sensor with that of two ganged sensors, the connections between first and second sensors were only partially bonded. Thus, we indeed found that the SNR of a single sensor is good, but with two ganged sensors it already drops to an unacceptably low value, as shown in tab. IV. Consequently, there is no chance to operate the APV25 with more than one sensor, especially as those might be made from 6” wafers in the future.

<table>
<thead>
<tr>
<th></th>
<th>ganged p-side</th>
<th>ganged n-side</th>
<th>single p-side</th>
<th>single n-side</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cluster SNR</td>
<td>9.4</td>
<td>10.1</td>
<td>13.1</td>
<td>13.9</td>
</tr>
</tbody>
</table>

Table 1: Cluster SNR comparison between a single and two ganged 4” double-sided sensors using the APV25. The readout pitch is 50 µm on the p-side and 152 µm on the n-side; both are equipped with a floating intermediate strip. The values were obtained in a beam test with 3 GeV electrons.

V. CHIP-ON-SENSOR

Hence, the only way to maintain a good SNR is to put the APV25 as close as possible to the sensor strips, which leads to the chip-on-sensor concept. This means that the readout chip, together with its hybrid circuit, sits on top of the sensor such that there is no need for long flex fanouts anymore. A schematic view of such an assembly is shown in fig. 3, where the “hybrid” is made of a (double-layer) kapton circuit which is separated from the sensor by a layer of rigid foam called Rohacell [6] which provides both electrical isolation and thermal insulation. The APV25 chip can be thinned down to 100 µm (or less) to reduce the overall material budget and make the whole assembly more homogeneous. Mechanically, the structure is held by both the cooling pipe and the plastic rib in parallel which could be made of Zylon [7], which was already used in the SVD2, or another stiff and light-weight material.

A. Flex Module

In 2006, we built a demonstrator prototype module called “Flex Module” where the short strips (n-side) are read out using the chip-on-sensor concept, while the long strips on the p-side are connected in a conventional way even though the associated “hybrid” is also made on kapton. This module uses a carbon fiber pipe for both cooling and as a stiffener, which turned out to be more massive than other solutions to be discussed later. Fig. 4 shows photographs of both sides of this module.

As expected, this concept of short front-end connections on the n-side yields much better signal-to-noise than the traditional
assembly where all strip signals are routed to the side of the sensor using long fanouts. Tab. A. compares the cluster SNR values of this module to the ones of the conventional module with a single sensor already shown earlier in tab. IV.

![Figure 4: Both sides of the Flex Module. The n-side (top) is built according to the chip-on-sensor concept, while the p-side (bottom) is conventionally read out from the edge.](image)

<table>
<thead>
<tr>
<th></th>
<th>Flex Module</th>
<th>Conventional</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cluster SNR</td>
<td>13.8</td>
<td>18.4</td>
</tr>
<tr>
<td>n-side</td>
<td>13.1</td>
<td>13.9</td>
</tr>
<tr>
<td>p-side (long strips)</td>
<td>13.8</td>
<td>18.4</td>
</tr>
</tbody>
</table>

Table 2: Cluster SNR comparison between the Flex Module utilizing the chip-on-sensor concept for the n-side readout and the conventional readout where all strips are fanned out to the edge of the sensor. These measurements use the same sensor design and were performed in the same beam test setup as described in the caption of the previous table.

Obviously, there is little difference on the p-side as both modules are read out from the side in the same way with just slightly different lengths of the fanouts. On the n-side, however, the difference is substantial and moreover, the chip-on-sensor figure does not depend on the number of detectors lined up in a ladder, as each sensor is read out independently.

B. Cooling

As each APV25 dissipates about 350 mW and finally there will be several thousand chips built into a small and sealed volume, cooling of the chips is absolutely mandatory. In order to explore various cooling options, we built a thermally insulated cooling channel with dimensions that resemble those of the space around a ladder in the future SVD. 24 SMT resistors are lined up on a carrier board and fed by a current as to dissipate the same amount of power as APV chips. Four different methods of cooling were tested:

- Air
- Water
- Heat pipe
- TPG

Air cooling suffers from the problem that its heat capacitance is very low. Hence, guided air would need extreme pressure and flow which is not feasible in practice. Alternatively, even free air flow without a pipe would need flow rates that could become dangerous to bond wires and moreover, there would be the problem of bottlenecks at inlet and outlet. Thus we conclude that air cooling is unrealistic.

Water has an enormous heat capacitance and thus is well suited for cooling requiring very little flow. Hence, one can use a pipe of small diameter and with thin walls in order to achieve a low material budget. We found aluminum pipes with an outer diameter of 2 mm and a wall thickness of 0.2 mm to be sufficient. Using a flow of only 1 ml/s, we could achieve a coolant temperature difference of only 3°C, which is in good agreement with theoretical calculation. Clearly, water cooling has a significant damage potential in case of leakage. In particular, there are worries about the long-term behavior of aluminum with water and it was suggested to use paraffin oil instead, which has already successfully been used to cool the beam pipe of the Belle experiment.

We also tried heat pipes which contain a liquid in a sealed volume where heat transfer is obtained by means of internal evaporation on the hot side and condensation at the cold side. Unfortunately, thin heat pipes did not meet the requirements of heat transportation, whereas thick heat pipes present too much material, as they are usually made of copper which has a low radiation length. Even though special aluminum heat pipes were made for space applications, their long term reliability remains doubtful.

The last option relies on heat conduction rather than the flow of a coolant and thus would completely avoid any risk of leakage. We used a bar of thermal pyrolytic graphite (TPG) [8], which features extremely high thermal conductivity – about four times higher than that of copper – along two axes. Despite that property, we did not achieve satisfying results with a cross-section of $5 \times 2$ mm$^2$ as the conductance is still too low. This could be improved by using a larger cross-section, but then also the material budget would increase accordingly. In conclusion, the TPG might be marginally suitable for an inner layer with limited length and heat load, but certainly not for the outer layers.

Overall, liquid cooling appears to be the only feasible option, but great care has to be taken to avoid potential risks due to leakage.
C. Origami

The chip-on-sensor technology presented above allows read-out of single-sided silicon detectors, but it is not straightforward to apply this concept to double-sided sensors. This would imply a duplication of “hybrid” as well as cooling and moreover present some challenges in routing of fanouts and/or the cooling pipe when dealing with the long strips (parallel to the ladder axis).

The Origami chip-on-sensor concept is a solution which overcomes these limitations by putting all the chips aligned onto the sensor side with the short strips, which allows a single straight cooling pipe to serve all dies. The short strips are routed to the chips with an integrated pitch adapter as done in the Flex Module (fig. 4), whereas the long strips of the opposite side are connected by flex fanouts wrapped around the edge, as shown in fig. 5. A 3D rendering in more realistic colors can be found in fig. 6.

One could argue that the cooling pipe, being round, cannot establish a good thermal contact with the chip. This can easily be solved by slightly flattening the pipe locally at the chip positions, which we confirmed with test in the thermal channel. Moreover, thermal grease will be used to improve the heat transfer. The position of the pipe will be chosen such that the preamplifier/shaper part of the chip is touched which is not only the noise-sensitive element but also dissipates about half the power consumed by the whole chip.

The APV25 chips reside at the voltage potential of the strips that they read out, which implies that readout chips for p and n sides, even though they are all lined up, are separated by the bias voltage of the sensor, typically 80 V at Belle. Hence, the kapton hybrid will be manufactured with four layers, where two layers are devoted to each side in order to achieve the best isolation possible. Naturally, the cooling pipe must also be isolated from the chips, which can be achieved by a thin heat-conductive foil with high electric strength.

D. Material Budget

![Perspective view of the Origami module.](image)

Clearly, the most challenging aspect of the Origami module is its assembly. Several jigs will be required for proper handling and the order of gluing and wire-bonding steps must be well considered. Probably the most critical item is the wrapping of the p-side flexes which will then get close to the underlying wire bonds of the n-side strips (see fig. 5 b). One option would be to protect those by a glob-top, but there are some worries about its long-term reliability, especially in conjunction with thermal stress and radiation. Hence, we prefer a purely mechanical solution such as a small piece of Rohacell glued onto the fanout behind the bond wires which would simply avoid the bent flex from falling down onto the bond wires. The third and most expensive solution would be to integrate the fanout into the sensor by using a second metal layer routing. The drawback of that option would be an increased capacitive load which is exactly what should be avoided by the chip-on-sensor concept.

<table>
<thead>
<tr>
<th>Material Budget [%X₀]</th>
<th>Conventional</th>
<th>Origami</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.48</td>
<td>0.72</td>
<td></td>
</tr>
</tbody>
</table>

Table 3: Comparison of the averaged material budget between conventional and Origami chip-on-sensor concepts.

The Origami chip-on-sensor concept is a trade-off between material budget and signal-to-noise. A simulation of the SuperBelle Silicon Vertex Detector showed that additional material is prohibitive in the innermost two layers due to degradation of the vertex resolution by multiple scattering, but no problem
for layers three to five, where the impact onto the vertex accuracy is limited. Fig. 7 shows a possible layout of the SuperBelle SVD, where DEPFET pixel detectors are foreseen in the innermost (double) layer. All double-sided silicon strip sensors are assumed to be made from 6" wafers and thus will likely need six readout chips on each side. We currently do not anticipate any problems arising from the transition from four to six APVs regarding the Origami concept.

As seen in fig. 7, the sensors closest to the edge will be read out in a conventional way since sufficient signal-to-noise can be achieved in that configuration (see tab. A.). The detectors inside the ladders, however, are read out using the Origami chip-on-sensor concept as ganging is not possible with the APV25 chip. Thanks to the choice of 6" wafers, the arrangement is perfectly compliant with the simulation requirements mentioned above, i.e. additional material is only introduced from layer three on.

Figure 7: Conceptual design of the Silicon Vertex Detector for SuperBelle, consisting of a double pixel layer surrounded by four silicon strip layers. The edge detectors will be conventionally read out from the sides, whereas the inner sensors will make use of the Origami chip-on-sensor concept. All silicon strip sensors are made from 6" wafers.

VI. SUMMARY AND OUTLOOK

Motivated by the upgrade of the Belle Silicon Vertex Detector – but not restricted to – we have presented the Origami chip-on-sensor method which can be used to read out double-sided silicon detectors with cooling of the readout chips. The main focus lies on minimization of the material in the active volume which is achieved by aligning all thinned APV25 chips on one side and wrapping kapton flexes around the edge to connect half of the chips to the strips on the opposite side.

The averaged material budget of such a module was calculated to be 0.72% X₀ in comparison to 0.48% found for the conventional construction where the readout hybrid sits on the side and thus, in case of Belle, outside of the active region. Such an assembly, in conjunction with sensor ganging, is possible with slow amplifiers, but prohibitive with fast shaping which is inherently more susceptible to noise and thus capacitive load. Yet, fast shaping is a requirement imposed by high luminosity and thus the Origami chip-on-sensor concept appears to be the only viable solution for silicon strip detector readout in SuperBelle.

In the near future, we will design the flex circuits and build a prototype Origami module in order to gain experience with the challenging assembly procedure which may lead to design optimizations. Source and beam tests will be performed to evaluate the performance of the module, even though we have no doubt about its functionality, as we already performed measurements with prototype assemblies such as the “Flex Module” which employed the chip-on-sensor concept on one side.

Eventually we will move to a 6" sensor design implying the readout of six APV25 chips for each side, which appears to be straightforward from our current point of view.

REFERENCES

[7] Zylon (http://www.toyobo.co.jp/e/seihin/kc/pbo/) is a stiff, but light-weight material made by Toyobo.
PMF: the front end electronic of the ALFA detector

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Abstract

The front end electronic (PMF) of the future ATLAS luminometer is described here. It is composed by a MAPMT and a compact stack of three PCBs which deliver the high voltage, route and readout the output signals. The third board contains a FPGA and MAROC, a 64 channels ASIC which can correct the non uniformity of the MAPMT channels gain thanks to a variable gain preamplifier. Its main role is to shape and discriminate the input signals at 1/3 photo-electron and produce 64 trigger outputs. Laboratory tests performed on prototype and pre-series PMFs have showed performances in good agreement with the requirements.

I. INTRODUCTION

The PMF (section B) is the front end electronics designed for the ATLAS luminometer (section A). It consists of a 64 channels photomultiplier (MAPMT) and a very compact stack of three different PCBs, mounted directly on the back and in the shadow of the MAPMT. The ASIC MAROC (section C) is used for the signal readout and treatment.

A. ALFA detector

ALFA stands for Absolute Luminosity For ATLAS [1]. This detector is located at 240 m from the interaction point (Fig. 1) and is meant to detect high energy diffused protons from the LHC beam. It is made of 20 staggered U-V scintillating fiber layers (Fig. 2) inserted in Roman Pots (eight in total). Each of these plans is made of 64 fibers which produce light when a particle comes through them. The light is then collected by multi-anode photomultiplier tubes H7546 from Hamamatsu [2], that will run at 800 to 950 V which corresponds to a gain of $3 \times 10^5$ to $2 \times 10^6$. These PMTs have an important non-uniformity that can not be corrected by applying a different high voltage to each channel. Therefore one has to amplify the output signal with different factors for each channel.

B. PMF

The Photomultiplier Front end (PMF) electronic is represented on the Fig. 4. It is made of a MAPMT and three boards (3 cm × 3 cm) in its shadow:

- The HV board which brings the high voltage to the MAPMT;
- The passive (or intermediate) board which routes the signals to connectors located on the edge;
- The active board which has the read out chip MAROC directly wire-bonded on the PCB on one side and a FPGA (Lattice) on the other side.
The PMFs will be arranged in a 5 by 5 matrix for each Roman Pot. Each line of up to 5 PMFs will be linked to the mother board through a kapton cable. In total 23 PMFs per Roman Pot will be installed, 20 for the standard scintillating fibers layers and 3 for another detector (overlap detector) described in [1].

The active board is technologically challenging since it consists of 10 different layers, has MAROC located on the sixth layer through a hole in the upper layers and needs different types of vias (see Fig. 5). The bonding wires (< 1cm long) are split between the first two layers.

### C. MAROC

MAROC (Multi Anode ReadOut Chip) is a 64 inputs ASIC which allows correcting for the gain spread of MAPMT channels thanks to a 6 bits variable gain preamplifier. For each channel the signal is shaped (fast shaper, 15 ns) and discriminated to produce a trigger output. The discriminator thresholds are set by an internal 12 bit DAC, made of a 4 bit thermometer DAC for coarse tuning and a 8 bit mirror for fine tuning [4].

A multiplexed charge output is also produced both in analog and digital thanks to a Wilkinson ADC. The block diagram represented on figure 6 summarizes the different features of this chip [4].

The main requirements are the following: 100 % trigger efficiency for a signal greater than 1/3 of a photoelectron, a charge measurement up to 30 photoelectrons with linearity of 2 % or better and a low cross talk. The performances of the second version of MAROC were checked successfully during the year 2007 at LAL-Orsay [5]. A nice dispersion of the trigger output (± 5 fC) was, in particular, observed.

### II. LABORATORY TESTS

#### A. Description

Lots of PMTs and PCBs were tested separately respectively at DESY and LAL-Orsay.

As far as what concerns the PCBs, the critical one to test is the active board due to its complexity and the many steps in its production. It is tested coupled with a passive board. A capacitor is used to inject signal in a single channel. A dedicated test board (left part of figure 7) has been designed for this purpose. Its role is to communicate with up to 5 PMFs via a kapton cable (central part of figure 7) sending configuration and collecting output signals. Standalone C and Labview programs were developed in order to enable testing.

A first batch of 8 active boards, considered as the prototype, was produced during autumn 2007. Thorough laboratory tests were performed at LAL after a period dedicated to the development of both test board (Xilinx) and PMF (Lattice) FPGA firmwares.

One of this active board was used to build a full PMF (3 PCBs and a PMT) in order to carry out a test with a LED illuminating a single scintillating fiber or the whole PMT (right part of the figure 7).

#### B. Prototypes

1) **Standard electrical tests**

All the main characteristics were measured for five active boards out of 8: pedestals, DAC linearity, S-curves (trigger efficiency as a function of the injected charge or the threshold), cross talk and charge.

All of them were found in good agreement with the results obtained during the characterisation of MAROC2 with particularly a nice homogeneity of the pedestals and s-curves.
2) Tests with a LED

Trigger measurements were performed illuminating one or all channels of the MAPMT with a LED for different settings. The parameters tuned were the threshold, the diode pulse amplitude (Vdiode) and the high voltage (HV).

![Image]

Fig. 8. Left: S-curves of 8 channels for a fixed Vdiode value. Right: S-curves of a single channel for four different Vdiode values.

Left part of figure 8 represents the trigger efficiency, for fixed Vdiode and HV, as a function of the threshold applied to the PMF for 8 different channels. As expected the so-called s-curves are observed with a trigger efficiency going from a constant (plateau) value to 0.

Increasing the amplitude of the LED increases the level of this plateau as it can be seen on the right side of the figure 8.

A test of the gain equalization was tried by illuminating all channels as uniformly as possible. Figure 9 shows the trigger efficiency as a function of the channel number before and after gain equalization. Dispersion was improved by a factor 3.5 from 13.3 % to 3.8 %.

![Image]

Fig. 9. Trigger efficiency as a function of channel number before and after gain equalization.

C. Pre-series

Here are presented results of the measurements performed on 28 active boards out of the 32.

1) Pedestals

Fast shaper pedestals were measured and a good homogeneity was found as it can be seen on figure 10 which represents the distribution of the pedestal for all the channels of the 28 active boards (i.e. 1792 channels in total). The dispersion is small and equal to 0.4 %.

![Image]

Fig. 10. Fast shaper pedestal distribution for pre-series active boards.

2) DAC linearity

Similarly the DAC linearity of the 28 active boards has been measured. It consisted in measuring the amplitude (Vdac) obtained for different DAC register values. Top part of figure 11 gives the evolution of Vdac as a function of this register for all boards. The nice homogeneity observed is confirmed by the linear fit parameters represented as a function of the PMF number (bottom part of figure 10).

![Image]

Fig. 11. Top: DAC linearity for the 28 active boards. Bottom left: slope of the DAC linearity fit as a function of PMF number. Bottom right: intercept (Vdac at DAC=0) of the DAC linearity fit as a function of PMF number.

3) Trigger outputs

The trigger output behaviour was studied by scanning the injected charge for a fixed threshold value and a unity gain applied to all channels.

Figure 12 represents the s-curves obtained for 1785 channels out of 1792. The 7 remaining ones are a bit shifted but nothing that can not be corrected by tuning the gain.

![Image]

Fig. 12. S-curves for the 28 active boards distinguished by different colors.
The good homogeneity observed can be characterized by the distribution of the injected charge needed to get 50% trigger efficiency represented on figure 13.

Fig. 13. Distribution of the injected charge needed to get 50% trigger efficiency among all 1792 channels.

III. CONCLUSIONS

The laboratory tests carried out on prototype and pre-series PMFs have showed that they are matching the requirements. The technological challenge consisting in producing a 10 layers PCB with several different vias and an ASIC bonded directly on it seemed to be achieved.

The pre-series batch of active boards showed a really high yield with no board rejected. Only 0.4% of the channels (7 out of 1792) had an s-curve shifted with respect to the others.

LED tests performed at CERN and DESY proved that the full PMF was also working well.

23 pre-series PMFs were used during beam tests of a complete Roman Pot which took place during August 2008. Results should give the final green light for full production of all three kinds of board.

IV. REFERENCES

Custom DC-DC converters for distributing power in SLHC trackers


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Abstract

A power distribution scheme based on the use of on-board DC-DC converters is proposed to efficiently distribute power to the on-detector electronics of SLHC trackers. A comparative analysis of different promising converter topologies is presented, leading to the choice of a magnetic-based buck converter as a first conversion stage followed by an on-chip switched capacitors converter. An overall efficiency above 80% is estimated for the practical implementation proposed.

I. SLHC POWER DISTRIBUTION NEEDS

In the design of upgraded trackers for SLHC, the required increase in the number of readout channels should not lead to a heavier tracker. Since cables and cooling are amongst the main contributors to the material budget, and they are both dependent on the amount of power burnt in the tracker, on-detector power management is necessary. It is important to both decreasing the power per function ratio of Front-End (FE) electronics, and to distributing the power efficiently.

The first objective can be reached in a straightforward manner by decreasing the voltage supply. This is not possible for the analog readout circuitry, whose design will already be challenging in the low-voltage CMOS processes in the 130nm node or below (typical maximum $V_{dd}$ around 1.2V). On the contrary, the supply voltage of the digital circuitry can be sensibly decreased below 1.2V, since standard cells in these advanced technologies are capable to run – at nominal $V_{dd}$ – much faster than the 40-160MHz required for the FE ASICs.

The above considerations lead to separate analog and digital power domains to be provided to SLHC tracker’s staves. In fact an additional domain will be needed, because optoelectronics components at the end(s) of the stave will require a voltage of at least 2.5V. The 2.5V will possibly be needed also by the stave and hybrid controller ASICs, in particular for the Input/Output (I/O) circuitry. The presence of 2 voltages on-chip, 2.5V for the I/O and 1.2V (or less) for the core, is a normal feature of advanced commercial digital circuits, and is commonly supported by CMOS technologies.

The number of power domains is not sufficient to draw a specification for the power distribution system without an estimate of the required current. Although the design of FE readout circuits for SLHC trackers is still in a very preliminary phase, a projection based on available estimates can be very useful. The following projection refers to the ATLAS tracker, for which a strawman design [1] and estimates for both analog [2] and digital [3] power consumptions exist. In Table 1, the projected needs for a portion of the tracker, the Short Strips barrel detector, is compared to the barrel SCT detector which is currently installed at comparable radius. In the table, we call “active power” the total power actually consmumed by the electronics. The basic assumptions for the projection are:

- Current for the analog readout circuit: 130μA/channel
- Total current for the on-chip digital circuitry: 80mA
- 128 channels in each FE ASIC
- 20 FE ASICs per hybrid
- Only FE readout ASICs are considered.

There are two fundamental concepts emerging from the comparison of the two systems. First, the current to be provided to the load increases by a factor of 6. Since the power lost in a cable is proportional to the square of the current, this implies a 36-fold increase in losses if the power distribution system remains the same as today. Second, a large amount of power is wasted (about 4kW out of 16kW, or 25%) if the distribution system is unable to provide different voltage domains for analog and digital circuitry, and the whole of every FE ASIC is biased at 1.2V. It clearly appears that, to be efficient, the new distribution system has to achieve a large decrease of the current in the cables from the power supplies (off-detector) to the hybrids, and has to support the distribution of different voltage domains.

| N of layers | 4 | 3 |
| Min and max R [cm] | 30, 51 | 38, 60 |
| Barrel length [cm] | 153 | 200 |
| N of FE ASICs | 25000 | 173000 |
| N of readout hybrids | 2100 | 8600 |
| Active power [kW] | 11.6 | 16.2 (1.2 & 0.9V) |
| | | 20.3 (1.2V only) |
| Load current [kA] | 2.75 | 17.2 |

1 We call stave a tracker detector assembly of several modules, each module being a silicon strip detector read-out by 1 or 2 hybrids. Each hybrid contains several FE ASICs and a controller ASIC.

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II. DISTRIBUTING POWER WITH DC-DC CONVERTERS

In commercial applications such as computing and networking, power is typically distributed using AC-DC and DC-DC converters [4]. A first AC-DC converter takes power from the mains and produces a regulated and filtered main bus voltage, which is distributed to a number of DC-DC Intermediate Bus Converters (IBC). Each of them supplies a power domain with an Intermediate Bus Voltage, where Point of Load converters take power to provide the loads with a regulated voltage. The low voltage required by the load is hence produced close to it, the required power being distributed at higher voltage ($P=V\cdot I$).

A similar but simpler scheme could be used to distribute power in SLHC trackers, since on-stave and/or on-hybrid voltage conversion would indeed enable the desired reduction in current along the cables connecting the power supplies to the stave/hybrid. Such scheme is also capable of locally providing different voltage levels through the integration of different converters on the hybrid. This principle is shown schematically in Figure 1, where 2 step-down converter stages (thus named because $V_{\text{out}}<V_{\text{in}}$) are used. First, a conversion stage 1 on stave or hybrid provides two intermediate bus voltages: an “analog” 2.5V and a “digital” 1.8V. These buses locally run across one hybrid or a few neighbour hybrids. A second conversion stage, integrated on-chip, acts as a divider by 2 to supply the required voltage to the analog and digital circuitry on both the controller and readout ASICs. The overall conversion ratio achieved is closed to 10, for a comparable decrease in the current on the 10V line coming from the off-detector power supplies.

A possible implementation of this scheme is shown in Figure 2, where a full stave is powered via a unique 10V line (the other line at the left of the stave is the optical link for communication purposes). At the left of the stave, one converter (stage 1) supplies 2.5V to the optoelectronics and the stave controller, where the required core voltage of 1.2V is generated on-chip by a conversion stage 2. In both Figure 1 and 2 the intermediate bus voltage is ideally divided by 2 on-chip, hence producing a 1.25V analog voltage, whilst in reality unavoidable losses will decrease it a little below this nominal value, making it closer to 1.2V. The same applies for the digital line.

The main features of this implementation can be summarized as follows:

- Different voltage domains are generated locally from a unique 10V line. FE analog and digital circuitry can be efficiently powered at the required $V_{\text{dd}}$.
- The current along the 10V line is decreased by a ratio of about 10 with respect to the load current. Power losses on this line are minimized ($P=RI^2$).
- Load current does not need to be constant in time. This is compatible with the presence of switching loads (for instance, for clock gating).
- High modularity in the distribution of power allows for individual or grouped turning on/off of ASICs, greatly facilitating system start-up. In case of FE ASIC failures, only individual groups can be turned off without loosing full hybrids.

![Figure 1: Power distribution scheme providing multiple voltage domains to the controller and readout ASICs from a single 10V line.](image)

![Figure 2: Possible implementation of the proposed distribution scheme. The choice on whether to have the conversion stage 1 on-hybrid or on-stave (to serve several neighbour hybrids) depends on the power rating of the converter and hybrid and on available space.](image)
All these attractive features require some fundamental problems to be solved for a successful implementation. In the first place, both conversion stages being embedded on stave, each converter needs to be tolerant to both the radiation and magnetic field present in the tracker. Commercial step-down converters being designed to use ferromagnetic inductors that saturate in the 2-4 T magnetic field, and not being engineered to reliably tolerate high levels of radiation, are not usable. Therefore a dedicate development is needed (ASIC). An additional concern is the integration of switching converters at close proximity to the very sensitive readout ASICs and silicon detectors. Due to their switching nature, these converters introduce noise sources that might affect the system’s performance. This last aspect is discussed in more detail in [5], [6].

III. PRACTICAL IMPLEMENTATION

The practical implementation of the distribution scheme proposed in II requires the analysis and comparison of different converter topologies in order to select the most appropriate for each conversion stage. The following five step-down topologies have been identified as the most attractive for our applications and have been evaluated:

- Buck converter (Figure 3). This is the simplest topology and the one making use of the smallest number of components, but at the same time it requires a large output capacitance for ripple cancellation and it functions with the larger RMS current in the inductor – not ideal for electromagnetic noise. A first prototype of this topology for our applications has already been designed [7] and tested [8].

Figure 3: Schematic of the buck converter. S2 and S4 are the power switches, and the control circuitry is not shown.

- Four-phase interleaved buck converter. In this topology, the power switches and inductor of Figure 3 are divided into 4 parallel branches each switching with a delay of ¼ of the period. In this way, it is possible to reduce the RMS current in each branch and to achieve a reduction of the output ripple (actually, for a conversion ratio of 4 the ripple is ideally cancelled). This topology requires a large number of components – amongst which 4 inductors – and a complicated control circuit.

- Two-phase interleaved buck with integrated voltage divider (Figure 4). This topology, inspired by a similar step-up implementation [9], allows a conversion ratio of 4 with the use of only 2 interleaved branches, still achieving ripple cancellation. With respect to the four-phase interleaved, it minimizes the number of components and greatly simplifies the control circuitry.

Figure 4: Schematic of the two-phase interleaved buck with integrated voltage divider.

- Multi-resonant buck converter. This topology, originally proposed in [10], has the interest of reducing the switching losses because all switching takes place in either Zero-Voltage or Zero-Current conditions. Nevertheless, this comes to the price of having large RMS currents, hence large conductive losses, and large $V_{ds}$ across transistors – increasing the $V_{dd}$ requirements on the technology. Additionally, the resonance is found for a specific load condition only, and re-tuning is necessary for different loads.

- Switched capacitor voltage divider. This is the only topology that does not require inductances, which is an attractive feature given the limitations imposed to inductors by our application. The simpler implementations of this topology are easy to integrate but do not provide regulation to the output. Overall, this is a good topology to be used as a divide-by-2 in a multi-stage distribution solution.

A. Conversion stage 1

This converter decreases the 10V input voltage to an intermediate bus voltage of 2.5 or 1.8V, which implies that the technology used for its fabrication must be capable of sustaining 10V with some safety headroom. At the same time, the full integration of both the power switches and the control circuitry on a single chip is a desirable feature to reduce component footprint, parasitic capacitance and inductance, and to simplify packaging and qualification tests. The best solution is therefore the use of a technology requiring both high-voltage and low-voltage transistors. Several such technologies, mainly aimed at the automotive market, are available today, and a market survey completed by irradiation tests is currently on-going. A technology in the 0.35μm node is currently being used for a first prototyping phase [8], and irradiation tests are scheduled for 0.18 and 0.13μm technologies.

Since ferromagnetic materials can not be used in the tracker’s magnetic field, the converter has to rely on air-core (or ‘coreless’) inductors [11]. These can be manufactured in very different topologies, but in this paper we will assume all inductors to be commercial and taken from the Coilcraft RF 132 series. These components are solenoid copper coils of reasonably small size (9.6x5.8x6.6...
mm³) and very low DC resistance – 2 to 83 mΩ depending on the inductor value (maximum = 709nH). This latter property has a large impact on the converter efficiency.

To select the most appropriate topology for conversion stage 1, the five topologies listed above have been compared for a conversion ratio of 4 \((V_{in}=10V, V_{out}=2.5V)\) and an output power of 6W. For each topology we have determined the current and voltage waveforms and estimated the main losses to eventually computing the efficiency. Calculations were carried out with Mathcad worksheets for each topology, making it easy to change the converter requirements (voltages, power) and the parameters of the inductor. Results are summarized in Table 2, where parameters for a 0.18\(\mu\)m high-voltage technology have been used. For the switched capacitor solutions, 2 stages in series – each divide-by-2 – were used. It has to be pointed out that the results in Table 2 have been obtained without modelling in detail the switching losses; hence the obtained efficiency is optimistic for all topologies and should be used in a relative fashion to compare them.

Table 2: Relative comparison of different converter topologies for \(V_{in}=10V, V_{out}=2.5V, P=6W\). Figures of merit are efficiency and number of components required (power switches, capacitors and inductors). NB: the multi-resonant requires an additional diode.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Efficiency (%)</th>
<th>Freq. (MHz)</th>
<th>N. of switches</th>
<th>N. of caps</th>
<th>N. of induct.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck converter</td>
<td>86</td>
<td>5</td>
<td>2</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>4-phase interleaved</td>
<td>88.3</td>
<td>5</td>
<td>8</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>2-phase interleaved with voltage divider</td>
<td>89.7</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>Multi-resonant</td>
<td>82.5</td>
<td>8.8</td>
<td>1</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>2 cascaded SW Cap</td>
<td>87.3</td>
<td>2</td>
<td>8</td>
<td>7</td>
<td>0</td>
</tr>
</tbody>
</table>

From the comparison table, and from the generic properties of each configuration listed above, it appears that the most appealing topologies are the buck converter (for its small number of components) and the 2-phase interleaved with voltage divider (for its efficiency, relative small number of components and complexity). Although a final choice between the two topologies has been delayed until a more thorough comparison can be made, a detailed parametric calculation for the 2-phase interleaved has been used in the following to estimate the system’s efficiency. In this exercise, we refined our model to more precisely take into account the switching losses by including simulation results from the 0.18\(\mu\)m technology.

At first, we concentrated on the choice of the optimum switching frequency of operation. The typical picture is that at low frequency, where a larger inductance is needed, conduction losses in the larger ESR of the inductor decrease the efficiency. At high frequency, more energy is dissipated in the switching. The highest efficiency is therefore found at some “intermediate” frequency, in our case about 1MHz. This is shown in Figure 5 for both the “analog” \((V_{out}=2.5V)\) and “digital” \((V_{out}=1.8V)\) converters in stage 1 and for an output power of 6W. The optimum inductor size changing with the frequency, for each point in the chart a different inductor from the Coilcraft RF 132 series was taken and its resistance was corrected for skin effect as appropriate for each frequency.

We then performed calculations for different loads and determined the size of the power switches leading to the highest efficiency in our distribution scheme. This will drive the development of converter prototypes. From our calculations, in the 0.18\(\mu\)m technology considered, the optimum size for the power switches gives an on-resistance of 30mΩ. The inductor to be used for the converter is chosen as a function of the load current and its value, together with the estimated efficiency for the converter, is reported in Figure 6 for both the analog and digital conversion stage 1 (inductors from the Coilcraft RF 132 series). An efficiency of around 90% can be reached for the conversion stage 1 of the analog power distribution, whilst a peak of about 86% is possible for its counterpart in the digital power distribution, in both cases for output currents in the range 3-5 A.

B. Conversion stage 2

In the proposed distribution scheme, converter stage 2 is integrated in the front-end readout or controller ASICs, and has therefore to provide a more modest level of current (20-100mA). The possibility of using a magnetic converter for this stage would be attractive only if the inductor could be embedded on-chip, which is not possible because of the large ESR of on-chip inductors (about 1Ω for a 15nH inductor in state-of-the-art 130nm RF technologies). A switched capacitor converter, used as a divide-by-2 stage, seems to be the most adequate solution in this case even in the absence of regulation from the converter (regulation is provided by a stage 1 converter a few cm away).

The schematic of the switched capacitor converter considered in our work is shown in Figure 7 [12].
“flying” capacitor C1 is alternatively connected in parallel to either C2 for recharge or C3 to provide power to the load. Such switching sequence is driven by a control circuit that drives the gate of transistors Q1 to Q4. A quick simulation has been run for this topology in a 130nm technology, using I/O transistors as switches, and gave an efficiency of 93% for a switching frequency of 20MHz. It seems therefore likely that, after careful choice of the most appropriate operating parameters (frequency in particular), an efficiency larger than this value can be obtained.

Figure 6: Estimated efficiency and required inductance for the ASIC used as conversion stage 1 for the “analog” (Vout=2.5V, top) and “digital” (Vout=1.8V, bottom) power distribution for different output loads

Figure 7: Schematic of the switched capacitor converter considered in this work.

IV. CONCLUSION

A power distribution scheme based on the use of on-hybrid and/or on-stave switching converters can satisfy the requirements for the SLHC generation of experiments. A comprehensive comparative study of different converter topologies led us to the choice of a 2-stages scheme. A first stage with a ratio of 4 is implemented as a 2-phase interleaved buck converter with integrated voltage divider or as a simple buck converter and requires the use of a technology rated for high-voltage (15-20V) applications. A second stage with a ratio of 2 is implemented as switched capacitor converter on-chip. Our calculations show that, combining the efficiencies of first and second conversion stages, an overall efficiency larger than 80% is achievable.

The proposed distribution scheme allows for distributing multiple voltages on-stave from a unique 10V input line from off-detector power supplies. Different voltages for analog and digital functions can easily be supported, achieving superior system efficiency. It also provides large modularity for grouping on-hybrid ASICs in power groups and facilitating system start-up and turn off of defective circuits.

V. REFERENCES

System Tests with DC-DC Converters for the CMS Silicon Strip Tracker at SLHC

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Abstract

The delivery of power is considered to be one of the major challenges for the upgrade of the CMS silicon strip tracker for SLHC. The inevitable increase in granularity and complexity of the device is expected to result in a power consumption comparable or even higher than the power consumption of today’s strip tracker. However, the space available for cables will remain the same. In addition, a further increase of the tracker material budget due to cables and cooling is considered unacceptable, as the performance of the CMS detector must not be compromised for the upgrade. Novel powering schemes such as serial powering or usage of DC-DC converters have been proposed to solve the problem. To test the second option, substructures of the current CMS silicon strip tracker have been operated for the first time with off-the-shelf DC-DC buck converters as well as with first prototypes of custom-designed DC-DC converters. The tests are described and the results are discussed.

I. INTRODUCTION

A. Power Distribution in the CMS Strip Tracker

The current CMS silicon strip tracker [1] is built of 15 148 silicon strip modules. The power consumption per module including the optical conversion is 1.8 or 2.7 W (depending on the module type); the whole strip tracker consumes about 33 kW. Groups of 2-12 modules are powered in parallel via roughly 50 m long copper low impedance cables from CAEN power supplies that are located on the balconies of the experimental cavern. The voltage drop on these long cables leads to a loss of 34 kW, i.e. 50% of the total delivered power is lost in the cables. The current power system is described in detail in [2]. The power lost inside the cold volume of the tracker contributes to the total heat load, which has to be removed to ensure that the sensors are kept at temperatures below $-10^\circ$C, as required to avoid thermal runaway effects. Power cables and cooling structures increase the material budget of the tracker considerably. The routing and installation of the services has been one of the most complex tasks during tracker commissioning.

Currently plans for an upgrade of the CMS strip tracker are developed in view of a potential luminosity upgrade of the LHC, the Super-LHC (SLHC). While the design is still under study, it is obvious that the granularity of the tracker will have to be increased, while additional complexity will have to be added; in particular, if the tracker information is to be used in the first level trigger stage. On the other hand it is expected that the front-end electronics will be developed in a smaller feature size process, such as 0.13 $\mu$m CMOS. For this process and a sensor capacitance of 5 pF (current strip sensor capacitances range from 10-25 pF) a decrease of the front-end power per channel by roughly a factor of 5 was estimated [3], an advantage that is partly canceled by lowering the operating voltage from 2.5 V to 1.2-1.3 V. In total, while the power consumption of the upgrade tracker is not precisely known as of today, it is very likely that it will equal or exceed the current power consumption. While an increase of the number or cross-section of cables is not desirable due to the expected increase of the material budget and the accompanying negative effect on the detector performance, it is even considered practically impossible since the tracker services are buried beneath the services of the electromagnetic calorimeter, and since the space available in the service channels is already occupied by the current services.

B. DC-DC Conversion

To deal with the problem, which affects both the ATLAS and CMS trackers, two solutions have been proposed: Serial Powering (SP) and powering with DC-DC converters. While in SP a number of modules are connected in series to a constant current source, DC-DC converters [4] are used to convert a high DC input voltage to a lower DC output voltage. In this paper, we concentrate on the latter option.

The ratio of the output to the input voltage, $V_{\text{out}}/V_{\text{in}}$, is called the conversion ratio, here denoted as $r$. If $r$ is small, ideally much smaller than 1, the input current can be smaller by the same factor, leading to a reduction of the power loss by $r^2$. In a simple approach, one converter could be installed per module. Several technologies exist, but mostly inductors or capacitors are used as energy storage elements. For each technology there is a great variety of topologies and designs. The simplest inductor-based step-down (i.e. $r < 1$) converter type is the “buck” converter. Its basic circuit consists of a switch, which is typically implemented as two transistors, an inductor for energy storage, and a filter capacitor. Realistic devices feature also a feedback circuit based on Pulse Width Modulation (PWM). DC-DC converters are flexible: with the same basic circuit, various output voltages can be achieved with minor reconfigurations, and several converter stages can be combined. In contrast to capacitor-based approaches, inductor-based designs can in general provide currents of several Amperes. Challenges are the achievement of an efficiency as high as possible, the need for a radiation-hard technology that supports the high input voltage (expected to be around 10 V for SLHC applications), as well as the potential generation of switching noise. Another issue for inductor-based layouts is the requirement to operate in a high
magnetic field (4 T for CMS): since ferrite materials saturate, air-core inductors must be used. To achieve the necessary inductances, these coils must be relatively large and massive. Due to the far extension of the magnetic field, the radiation of electromagnetic noise is a potential issue.

To understand better the opportunities and challenges related to this proposed solution to the power problem, we have performed system test measurements with commercial and custom DC-DC converters.

II. THE SYSTEM TEST

A. Set-up Description

In the absence of any prototype structures for the tracker upgrade, substructures of the current tracker end caps, referred to as petals, have been used. While future devices will be different in many respects, we believe that lessons can be learned from operating current tracker structures with DC-DC converters.

The petals as well as the data acquisition chain are described elsewhere [1]. Here only aspects of the front-end (FE) electronics relevant for the system test are described. The test petal was equipped with four ring-6 modules. This module type carries two daisy-chained sensors with AC-coupled p-doped strips implanted in a 500 μm thick n-doped bulk. The sensor capacitance amounts to about 20 pF. The connections between sensors and between the first sensor and the FE-electronics are realized with wire bonds. The FE-hybrid carries six APV25 readout chips [5], which are manufactured in a 0.25 μm CMOS process. Each chip processes the data of 128 channels. The read-out is fully analogue. For each channel, a charge-sensitive pre-amplifier, a CR-RC filter with a time constant of 50 ns, and a 192 cells deep pipeline are implemented. The data are sampled at 40 MHz. Two readout modes can be selected: in peak mode only one sample is used per event; in deconvolution mode a weighted sum of three consecutive samples is formed to reduce the effective shaping time to 25 ns. On receipt of a level-1 trigger, the data are output with a rate of 20 MS/s. Data of two APVs are multiplexed onto one optical channel by the APVMUX chip, resulting in a 40 MS/s serial output stream. The APV25 is powered from two supply rails, namely 1.25 V and 2.5 V. Typical currents are 60 mA and 120 mA, respectively [2]. All other chips on the hybrid as well as the analog-optical converters (Analog-Opto Hybrids, AOH) and the controller chips (Central Control Units, CCU) operate with a supply voltage of 2.5 V.

All modules have been powered and read-out during the measurements. The petal was equipped with the original motherboards (InterConnect Board, ICB), AOHs and CCU modules. Both readout and digital signalling (trigger, clock, fast controls) was realized optically. PCI-based prototypes of the ADC card (Front End Driver), the trigger card (Trigger Sequencer Card) and the controller card (Front End Controller) have been used. The petal has been thermally stabilized at +15 °C. It was housed in a grounded metal box. The set-up was very similar to test systems used during integration of the CMS tracker [6].

The modules have been commissioned with a well-known procedure and operated with fully depleted sensors, mostly in peak mode.

B. Analysis Method

The analysis method is described in [6]. The raw or total noise is calculated as the RMS of the fluctuations around the pedestal value, which is the mean strip signal without particles traversing the detector. The common mode (CM) is defined as a common event-wise fluctuation of all strips of an APV, and is calculated as the median of the signals after subtraction of the pedestals. It is included in the raw noise. The common mode noise is the RMS of the common mode. At least 100 000 events have been taken per run to assure stable conditions, of which 10 000 events, starting from event 90 000, have been analyzed.

III. MEASUREMENT RESULTS

A. Commercial DC-DC Converters with Internal Ferrite Inductors

Since custom radiation-hard DC-DC converters were not available when we started our investigations, we used commercial buck converters. The first tests were performed with buck converters with internal coils.

A market survey was performed to identify a device with high switching frequency (i.e. small size of passive components), low conversion ratio, a suitable output voltage range and sufficient output current. The Enpinor buck converter EN5312QI [7] was chosen: with dimensions of 5x4x1.1 mm³, a switching frequency of 4 MHz and a maximum current of 1 A it is appropriate for our application. A disadvantage is the relatively low recommended maximal input voltage of 5.5 V. The device implements an internal planar inductor in MEMS technology. Due to the deployment of magnetic cores it is not usable in a strong magnetic field.

Two such devices, configured to provide 2.5 V and 1.25 V, respectively, were mounted on a four-layer PCB, together with input and output filter capacitors and connectors (Figs. 1 and 2). This PCB can be plugged between the ICB and the module. Two versions of the PCB have been tested: the L type (Fig. 2, left) is slightly larger, the S type (Fig. 2, right) is smaller and more modular in design (separate PCB for connector).

![Schematics of the L type PCB with two EN5312QI buck converters](image-url)
The raw noise distribution of one module is shown in Fig. 3 (the results for other modules are similar and not shown here). The noise level is slightly increased by up to 10% (note the zero-supression on the y-axis). The additional contribution is common mode, as reflected e.g. in a broadening of the CM distribution. With the S type board, the increase of noise is almost negligible. The difference between the boards has been traced back to the additional connection between the main and “connector PCB”. Clearly a careful PCB design is very important to achieve an optimal noise performance. Further studies have mostly been performed with L type boards.

Edge strip channels are known to be sensitive to noise effects, such as coupling from the bias ring or common mode due to bad grounding. With converters, the noise on module edge strips increases by up to a factor of 10 (Fig. 4). Furthermore, the noise on disconnected channels increased from a low level to a level even above the mean. For the interpretation the common mode subtraction inside the APV has to be considered [8]. Each APV channel implements an inverter stage. These are powered from 2.5 V via a common resistor, located on the FE-hybrid. If a common mode signal is present at the inputs of the inverters, a voltage drop is created across the resistor that drives down the inverter output and effectively subtracts the common mode from it. This, however, does not apply to channels which see a lower than normal CM, such as disconnected channels, or a higher than normal CM, such as edge channels. If a certain common mode is present in the system, the CM they see will be over-compensated or not completely subtracted, respectively. Their signal is thus a sensitive indicator of the CM actually present in the system. Further studies have shown that connecting the converters only to 1.25 V, used to power the pre-amplifier, does not lead to any increase of CM on normal strips, while connecting converters only to 2.5 V, used in all other stages of the chip, does increase the noise. The edge strip noise is increased in both cases. The current understanding is that noise coupled in before the inverter can effectively be subtracted, except on edge strips and bad channels. Noise coupled in after the inverter, i.e. via 2.5 V, cannot be subtracted and is visible.

To study potential cross-talk effects, the correlation matrix between all pairs of strips has been computed for two adjacent modules that were powered with converters. The correlation coefficients are defined as $corr_{ij} = \langle r_i \cdot r_j \rangle / (\sigma_i \cdot \sigma_j)$, where $r_i$ and $\sigma_i$ are the raw data and noise of strip $i$, respectively. With ordinary powering, correlations amount to around 5% both for strip pairs within and between modules. With converters, correlations of 10-20% are observed for strip pairs within modules, reflecting the increased common mode. The correlations between modules are however not increased significantly, i.e. cross-talk between modules is not observed.

To investigate the potential effect of a Low DropOut regulator (LDO) on the voltage ripple and thus the noise, another PCB was developed. The LDO LTC3026 from Linear Technology [9] was connected to the output of EN5312QL. A ripple rejection of around 45 dB for the switching frequency of 4 MHz is quoted in the data sheet. Tests were performed with dropouts of 50 and 100 mV. As visible in Fig. 5 for a dropout of 50 mV, a beneficial effect is observed: the raw noise is no more increased and the noise on edge strips is “only” a factor of 2 above the normal level. We conclude that the noise in our system is mainly caused by a conductive coupling of a differential mode component of the converter noise.
Effect of shielding

Raw noise [ADC counts]

2.4 1.6 1.8 2.2 2.6

Effect of different inductors

No converter Internal inductor Ext. ferrite inductor Ext. air-core inductor Ext. air-core inductor, LDO

Effect of LDO with internal inductor

No converter Without LDO With LDO

Figure 5: Raw noise for conventional powering (black) and powering with a L type PCB with (blue) and without (red) LDO.

B. Commercial DC-DC Converters with External Air-Core Inductors

Since ferrite inductors cannot be used in the final experiment, commercial buck converters have been equipped with external air-core inductors. For these tests, the Enpirion buck converter EQ5382D has been chosen, which is similar to EN5312QI, but has no internal inductor. PCBs similar to the L type have been fabricated and equipped with various coils: planar ferrite inductors (Murata LQH32CN1R0M23, \(L = 1 \mu H\)), air-core solenoids (Coilcraft 132-20SMJLB, \(L = 538 \text{nH}\)) and custom-made air-core toroids \((L \approx 600 \text{nH})\). With air-core inductors, the noise increases drastically compared to internal or external ferrite inductors (Fig. 6). For toroids the increase is a factor of 2-3 lower than with solenoids. The edge strip noise increases enormously, up to about 90 ADC counts. When a module was operated with an air-core coil, the noise increased also on its conventionally powered neighbour modules.

The wing-shaped noise has been traced to a pick-up of radiated noise in the FE-hybrid region. This has been proven in tests where the module was powered conventionally but exposed to the radiation of noise by powered but unplugged converter boards or individual coils operated with a frequency generator. In both cases, wing-shaped noise was induced in the module. In one test the PCB was placed above the conventionally powered module and the position of the converter board was varied systematically. For each position the mean module noise was computed. The biggest effect was observed when the PCB was placed above the FE-hybrid, while the effect was very small when the board was located above the connector. With air-core coils the conductively generated noise is increased as well, presumably by noise coupling from the coil into the PCB itself. Further studies are needed to understand the details of the coupling mechanisms and the shapes of the distributions. As expected, using a LDO does decrease the conductive part, but not the wings (Fig. 6).

Tests have been performed with shielded converters. The PCB was wrapped in copper or aluminium foil of 35 and 30 \(\mu \text{m}\) thickness, respectively. The noise decreased significantly (Fig. 7). Grounding the shield did not improve the situation. No further improvement was obtained with thicker shields.

The chosen foils might already be thicker than necessary and thinner shields should be tried. The noise contribution remaining with shielding is probably induced conductively. While shielding is in general not desirable due to the associated material, adding an aluminium box of (3 cm)\(^3\) (a very conservative assumption) and a thickness of 30 \(\mu \text{m}\) for instance to each module in the end caps would increase their mass by only 1.5 kg (2 per mille).

Finally the distance between the converter PCB and the FE-hybrid has been varied. For this test, the L type board with external air-core solenoids has been equipped with an S type connector. A cable has been plugged between the board and the “connector PCB”, so that distance and cable length could be varied. The noise effect depends strongly on the distance. When the distance is increased by a few centimetres, the increase of noise is almost negligible. It should be noted that the conductive noise is decreased as well due to passive filtering in the connector and cable. While space around single modules is expected to be very constraint in a new tracker, an operation of buck converters on the substructure level could thus be feasible.
C. Custom DC-DC Converters

1. The SWREG2 Buck PWM Controller (CERN)

A single phase buck PWM Controller with Integrated MOS-FET is being developed at CERN [10]. The first prototype chip (SWREG2) in AMIS I3T80 technology became available shortly before the conference. The chip accepts input voltages from 3.3-20 V; the maximum output current is 2 A. The SWREG2 implements the transistors and the logic of the feedback control circuit. Together with external components like voltage references, filter and bootstrap capacitors and of course the air-core coil it is mounted on a 4-layer PCB (RWTH Aachen). The output voltage is configurable via a resistor. A tunable saw-tooth signal for the PWM is provided from a separate PCB and thus the switching frequency can be varied between 250kHz and 3 MHz.

During the test the SWREG2 provided the 2.5 V for the FE-hybrid, while the 1.25 V was supplied by an external PS. The distance of the board to the FE-hybrid amounted to several centimetres, so that the effect from conductive noise could be isolated. Data have been recorded for an input voltage of 5.5 V and several switching frequencies between 0.6 and 1.25 MHz (Fig. 8). Independently of the frequency, the noise level is increased by about 20%, and a noise ripple with a period of eight strips is observed. When the data are plotted in the order which is realized after the multiplexing stage of the APV, the ripple is eliminated and the noise varies smoothly with the sample number. This indicates that the noise couples into the back-end stages of the APV, i.e. in the stages after the multiplexer. This phenomenon has not been observed with any commercial converter.

2. Charge Pump (LBNL)

DC-DC converters that utilize capacitors instead of inductors as energy storage elements are commonly referred to as charge pumps. For a step-down converter, a number of capacitors are charged in series during the first phase and discharged in parallel during the second phase of the switching cycle. The output current is equal to the input current times the number of parallel capacitors.

A charge pump with divide-by-four stack configuration with three “flying” capacitors has been developed at LBNL [11]. The PCB implements a 0.35 µm CMOS IC with switches and driver circuits plus 1 µF input and flying capacitors and a 10 µF output capacitor. The switching frequency is 0.5 MHz. Due to the relatively small output current of 0.5 A, two charge pumps are connected in parallel on one “tandem” converter board. The capacitors of the two charge pumps charge either in-phase or with alternating phase. In the latter case, a lower output current ripple is expected. The PCBs have been used to power either 1.25 V or 2.5 V, while the second voltage was provided by an external PS. With the alt-phase PCB providing 2.5 V, the noise increases by about 20%, similar to the SWREG2, while the in-phase version leads to an increase by about 75%. When the converter was used to deliver the 1.25 V, only the noise on edge channels increased, in agreement with observations with the EN5312QI.

IV. Summary

Commercial buck converters with internal and external inductors as well as custom prototypes of a buck converter and a charge pump have been tested with CMS silicon strip modules. An increase of the noise level and the module edge strip noise due to the ripple and switching noise on the converter output voltage has been measured consistently in all cases. In addition, pick-up of noise radiated from air-core inductors was observed. Several countermeasures have been studied: implementation of a LDO, shielding, variation of the distance etc. While operation of buck converters close to individual modules seems to be disfavoured due to noise and space constraints, the operation of buck converters at substructure level in a 2-step approach could be possible. More studies are however needed to understand better the noise coupling mechanisms and to proof the viability of a power distribution scheme based on DC-DC converters.

REFERENCES

[9] Linear Technology, USA; http://www.linear.com/
Design Considerations for High Step-Down ratio Buck Regulators

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Abstract

The buck or step-down DC-DC converter is the workhorse switching power supply topology. It utilizes two switches (two FETS or one FET and one diode) along with an output inductor and output capacitor.

Whether you look at a large computer server, a personal desktop or a laptop computer, a cell phone or a GPS unit all will contain a buck converter in one form or another. This paper will discuss the synchronous buck topology, design considerations, component selection followed by a small signal model of buck converter. Issues that are important in optimizing the efficiency of the design for example MOSFET selection, the impact that the MOSFET driver plays in improving the efficiency will be examined. The paper will finish by contrasting various control architectures.

I. INTRODUCTION

As already mentioned, the buck converter steps down the input voltage from a high voltage to a low voltage. The simplest way to reduce the input voltage is to use a voltage divider circuit, but this is very inefficient and the excess voltage is wasted as heat. The buck converter provides an alternate voltage reducing method that minimizes the energy wasted and is highly efficient.

Referring to Fig. 1, the buck converter does this by alternately turning on and off the two MOSFETs Q1 and Q2 at a specific frequency resulting in chopped version of the input voltage appearing at the common connection point (referred to as Switch node) of the MOSFETs. The chopped voltage is followed by a low pass filter consisting of an inductor L1 and a capacitor C0. A dc voltage equal to the average value of the chopped voltage appears across the capacitor, while the ac voltage appears across the inductor. By balancing the volt-second across the inductor, the input-output conversion ratio of the buck converter is found to be “D” which is equal to Vout/Vin. This is referred to as dc gain of the converter.

Buck converter is the basic building block that drives the power electronics. Various forms of step-down converters exist, in both non-isolated and isolated forms. Isolated versions of the buck converter include push-pull bridge and forward topologies.

Prior to selecting the design approach, it is critical to understand the system needs/specs and design limitations. Considering the switching behaviour of MOSFET is critical in order to evaluate the conduction and especially the switching losses associated with the topology.

Output inductor is another very important part of the design selection, and compromises have to be made based upon loop performance, core and copper losses.

The paper will review the various controller architectures and summarize the pros and cons of each approach.

II. SYNCHRONOUS VS NON-SYNCHRONOUS BUCK

Switching or Inductive buck converter as shown in fig. 1 provides higher efficiency. Q1 is referred to as control Fet and Q2 is referred to as synch Fet.

Note with 7% improvement in converter efficiency, Output power doubles for fixed power dissipation. From the system point of view it is critical to have a converter that has high efficiency, thus the overall system cost can be reduced as less efficient design will require extensive thermal management.

A non-Synchronous Buck converter (when Q2 is replaced with a diode D2) has two operating modes. At high load current it is in continuous conduction mode (CCM). As the load current decreases it goes into discontinuous conduction mode (DCM). During discontinues mode (DCM) of operating catch diode (D2) blocks reverse current and voltage across the inductor is collapsed. During DCM there is an interval where no current is passed to the output inductor. Thus the average inductor current provided to the load requires a more detailed analysis. Whereas Synchronous buck converters will always operate in continuous conduction mode as the Sync Mosfet is turned on allowing reverse current to flow. Synchronous buck converter will tend to provide higher efficiency at high loads.
because of sync MOSFET with low on-resistance will result in lower conduction losses than diodes. In order to improve efficiency at light load conditions the converter is allowed to operate in DCM. This is generally done by turning off the sync FET when negative inductor current is sensed. Circuit emulates diode behaviour under this condition.

III. SPECIFICATIONS/ DESIGN CONSIDERATIONS

Before designing any converter topology, it is important to determine the system specifications. The input voltage range, output voltage, load current, output ripple voltage and load transient requirements are typically specified by the customer. Other typical specifications relate to space and thermal constrains.

Space and thermal constrains typically determine the frequency one would design the converter to operate at. Operating at higher frequencies the size of output components ie. Inductor and capacitors will tend to get smaller, but on the other hand operating at high frequency will also tend to increase the switching losses in MOSFETs, Fet Driver circuitry etc. Thus a compromise is required that would tend to meet the size constrains as well as meet the thermal/ cost targets of the design. Buck topology is generally the most cost effective approach due to the low component count.

### Table 1: Typical Specifications

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Max</th>
<th>Tolerance</th>
<th>Req’d</th>
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<tr>
<td>Vin</td>
<td>3.3</td>
<td>15</td>
<td>+/- 3%</td>
<td></td>
</tr>
<tr>
<td>Vout</td>
<td>1.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Iout</td>
<td>0A</td>
<td>10A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Ripple</td>
<td>50mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transient</td>
<td>100A/μsec</td>
<td>+/- 100mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Size</td>
<td>H x L x W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Efficiency</td>
<td>85%</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Ambient temperature</td>
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<td>Enable</td>
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<td>Tracking</td>
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<td>OV protection</td>
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<td></td>
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<tr>
<td>Current limit</td>
<td>x</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cost Target</td>
<td></td>
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</tr>
</tbody>
</table>

The input capacitor to the buck converter is selected based upon the input ripple current that the capacitor will see in the design, along with ensuring that it meets the voltage/ size requirements for the design. Rms value of input capacitor ripple current \( I_{cin, rms} \) can be estimated as indicated below.

\[
I_{cin, rms} = I_o \sqrt{D(1-D)}
\]

Where duty ratio \( D \) is defined as output to input ratio and referred to as “dc” gain of the converter.

\[ D = V_o / V_{in} \]

For high duty ratio, i.e. for output voltages that are close to the input, for example Vout = 9V for Vin = 12V a PWM controller must be picked that is capable of operating at high duty cycle. This constrain is typically specified in the data sheet as either the maximum duty cycle or the minimum off time of the top MOSFET.

For high step-down, where there is a wide separation between input and output voltage for example if Vout = 0.8V and Vin = 15V the PWM controller must be capable of operating at very low duty ratio i.e. min duty cycle. The datasheet of the controller will typically specify this as a minimum on-time for the top MOSFET. The minimum on-time specification will determine the maximum operating frequency of the converter for the specified input and output voltages while taking into consideration the efficiency of the design.

IV. MOSFET SELECTION

There are a number of factors that are critical to ensure high efficiency. Proper component selection i.e. MOSFET, Output inductor, Optimum drive voltage driving the MOSFET, reduced dead time and careful layout all play a major role in the final design to ensure high efficiency.

In order to ensure that the converter provides high efficiency, proper MOSFET selection is critical for the design. As MOSFETs are one of the major loss contributors of the design.

There are a number of MOSFET critical parameters besides Rdson and Qg that must be evaluated i.e. Cgd, Cgs and Cds, but these are not readily defined in the FET datasheet, but can be calculated as follows:

\[
C_{GD} = C_{RSS}
\]

\[
C_{GS} = C_{ISS} - C_{RSS}
\]

\[
C_{DS} = C_{OSS} - C_{RSS}
\]

These parasitic capacitors of MOSFETs are related to the actual geometry of the device. Junction capacitors of semiconductor are non-linear and are inversely proportional to Voltage as indicated below. If we evaluate the charge in capacitor, one can see that the charge at some arbitrary voltage \( V_{in} \) will be twice as much as compared to the charge that a linear capacitor will have at voltage \( V_{in} \).

\[
C = f(V_o) = C_o \sqrt{V_o / V_{in}}
\]

\[
C_{gd}(V_{in}) = 2C_{ox, spec} \sqrt{V_{ds, spec} / V_{in}}
\]

Forward transconductance of the MOSFET is its small signal gain in the linear region of operation. The transconductance, \( g_{fs} \), is relationship between Drain current and gate-source voltage.

\[
g_{fs} = \frac{dI_D}{dV_{GS}}
\]

For high speed switching applications, MOSFET Gate resistance along with Gate driver resistance is extremely critical especially for high speed switching applications.
Turn-on behaviour of buck converter, based upon conventional model can be broken down into four steps. In the first stage, the input capacitor of MOSFET is charged from 0V to Vth, during this phase gate current is charging the Cgs capacitor. This phase is referred to as turn-on delay as drain current and drain voltage remain unchanged.

In the 2nd stage gate is raised from Vth to Miller plateau. This is the linear operation of device, when the current is proportional to gate voltage. Gate current is flowing in Cgs and Cgd capacitors here the drain current is increasing and Vds voltage does not change – in off state. This is the time it takes the MOSFET to carry the entire inductor current.

In the 3rd stage drain voltage is allowed to fall. While drain voltage falls, Vgs stays steady. All the gate current from driver is diverted to discharge the Cdg capacitor, in order to facilitate rapid voltage discharge from Vds. Drain current in device stays constant, as it is limited by external circuitry.

In the 4th stage MOSFET channel is fully enhanced by applying higher gate drive voltage. During this phase gate voltage is increased from Vgs_miller to its final value. This determines the ultimate on resistance of the device. During this phase gate current is split and charges Cgs and Cgd. On resistance is reduced.

Turn-off behaviour is similar to turn-on behaviour and is subdivided in four stages.

In the first stage, turn-off delay, during this phase Ciss capacitor is discharged from its initial value to the Miller plateau level. Current is flowing thru Cgs and Cgd capacitors of Mosfet.

In the 2nd stage Vds rises from Id*Rds on level to Vds(off) This period which corresponds to Miller plateau of the gate voltage. During this phase gate current is the charging current of Cgd capacitor and is subtracted from drain current.

In the 3rd stage gate voltage starts to fall from Vgs_miller to Vth. Majority of current is coming out of Cgs capacitor, as Cgd capacitor is virtually charged from previous stage. MOSFET is in linear mode declining gate-source voltage causes drain current to decay and reach zero by end of the interval.

In the 4th stage turn-off stage is to discharge the input capacitor of the device. Vgs is further decreased and most of the current is coming out of Cgs capacitor.

Profile of losses in both high side and low side Mosfets are quite different, especially for low output voltages where duty cycle is low. For low duty cycles low-side Mosfet are dominated by conduction losses.

$$P_{\text{conduction}_{-\text{HS}}} = I_q^2_{\text{max}_{-\text{HS}}} R_{ds_{-\text{on}}} = I_o^2 R_{ds_{-\text{on}}} D$$

Power Losses in Synchronous buck regulator consists of conduction losses, switching losses, Gate losses, Coss losses (Power loss to charge the MOSFET’s output capacitor) this is loss is dissipated in the Rds of the MOSFET.

In order to minimize switching losses, turn-on and turn-off transitions as highlighted in stage 2 and stage 3 of waveforms must be minimized. These transition times are when the MOSFET is in its linear operation range, when the gate voltage is from Vth to Vmiller. Gate driver’s ability to source and sink current are critical in determine the switching times.

Source Gate current during turn-on transition t2 can be approximated by $I_{g_{-t2}}$ and source gate current during (sink) turn-off transition t3 can be approximated by $I_{g_{-t3}}$.

Switching times can be approximated by $Q_{g_{-sw}/I_g}$.

Switching losses

$$P_{sw} = (1/2)V_{in} f_{sw} (I_{q_{min}} I_{q_{max}})$$

$$I_{q_{min}} = I_o - \frac{\Delta I_t}{2}$$

$$I_{q_{max}} = I_o + \frac{\Delta I_t}{2}$$

MOSFET driver losses can be approximated as $P_{sw_{-drv}} = V_{drv} f_{sw} Q_{g}$ where $Q_{g}$ is total gate charge.

Output capacitor losses; note Coss is non-linear capacitor and voltage dependent. $P_{coss} = 0.5 C_{oss} f_{sw} V_{in}^2$ and diode reverse recovery losses $P_{Q_{rr}} = Q_{rr} V_{in} f_{sw}$.

If external Schottky diode is used then during high side MOSFET turn-on, schottky’s external capacitor needs to be charged. Schottky diode losses $P_{schottky}$ can be calculated as

$$P_{schottky} = C_{sch} V_{in}^2 f_{sw} / 2$$
MOSFET Gate current during turn-on transition $t_2$ can be approximated by eq (1), gate current during turn-off transition $t_3$ can be approximated by eq (2) and the switching times $t_{sw}$ can be approximated by eq (3).

$$Q_{g..sw} = Q_{gs} + 0.5Q_{gr}$$

$$I_{g..t2} = \frac{V_{drr} - V_{th} + (I_{q.min}/g_m))}{R_g + R_{gext} + R_{drv}}$$

$$I_{g..t3} = \frac{V_{th} + I_{gq}(1/g_m)}{R_{gext} + R_{gext} + R_{DRV}}$$

$$t_{sw} = Q_{gw}/I_g$$

$$P_{conduction_{LS}} = I_{rms_{LS}}^2R_{ds_{on}} = I_o^2R_{ds_{on}}(1-D)$$

For the synchronizing fet (low side Mosfet) the major contributor is the conduction losses especially for low output voltages. As the MOSFET conducts current for the major part of duty cycle. Switching losses in the low side MOSFET are practically negligible, since Q2 switches on and off with a diode drop across it.

Conventional model which is commonly used in analyzing buck converters can give one simple and quick estimated losses. But for practical applications, efficiency measurements can provide better indications, when comparing one fet as compared to another. One of the main drawbacks of using conventional model is that it does not take into account the effect of source and drain inductances. These are package related parameters and play a significant role especially when operating at high frequencies. Reference [10] highlights the impact of source and drain inductance in the model. Model when taking leakage inductance into considerations shows that the turn-off losses are significantly greater than the turn-on losses, and measured and calculated error in switching losses is reduced.

High side MOSFET is selected to have low $Q_g$, whereas Low side (Sync) MOSFET is selected to have low $R_ds$ since for low output voltages, sync fet conducts for higher duty cycle, thus conduction losses are the dominant factors.

MOSFET driver plays a significant role in determining the efficiency of the circuit. Rdson of MOSFET is inversely proportional to gate drive voltage $V_{gs}$. This can be observed in any MOSFET data sheet, thus higher drive voltage results in lower Rdson. Typically drive voltage of approx 7V provides the optimum efficiency. This is the reason, one tends to see most design operating at drive voltage of approx. 7V, when input voltage is 12V. When the input voltage is reduced to 5V or below, the internal linear regulator which typically provides 7V drive voltage is bypassed and the drive voltage used to drive the MOSFET is the input voltage. Thus ensuring higher efficiency. MOSFET must be driven from a low impedance source that is capable of sourcing and sinking adequate current to ensure fast switching. Current source and sink capabilities of MOSFET driver must be capable of sourcing and sinking adequate current to ensure fast switching transitions.

V. MAGNETICS

Output inductor is another critical component of the design. It is important that the inductor is designed to ensure that it does not saturate when under the operating or overload condition of the circuit.

Inductor must be designed to ensure that the losses are not exceeded that would result in saturating the inductor implying that the inductance is reduced in the circuit.

There are two classes of materials used in inductors – One is alloys of iron and contain some amount of other elements i.e. silicon (Si), nickel (Ni), chrome (Cr) and Cobol (Co).

Other type of material is ferrites. Ferrites are ceramic materials. Mixture of iron, manganese (Mn), zinc (Zn), nickel and cobalt. Ferrites have high resistively. Iron powder is obtained from iron with low carbon content. Iron powder is resin bonded. Powdered iron cores consist of small iron particles electrically isolated from each other.

DCR losses of the inductor are based upon Inductor rms current square times inductor DCR. Inductor core losses are based upon inductor flux density, frequency of operation and core volume. Core vendors also provide curves that can be used to estimate core losses.

For ferrite cores, Steinmetz equation defines the core losses. $P_L = K_B(\frac{B^2}{10^6})(\frac{f}{1000})$ where frequency is in Khz, and core volume in cm

VI. OUTPUT CAPACITOR SELECTION

Output capacitor is selected based upon two critical criteria’s, for example equivalent series resistance (esr) of the capacitor which along with the inductor ripple current will determine the output ripple voltage to meet the customer specifications. Secondly the bulk capacitance, which along with the converter bandwidth determines the maximum overshoot and undershoots during transient conditions.

VII. SMALL SIGNAL MODEL OF BUCK CONVERTER

Once the power components have been specified, it is necessary to design a feedback compensator for the converter. The compensator will ensure that the output voltage remains at a fixed, stable value in spite of changes or perturbations in the input voltage and load current. This task is complicated by the fact that a dc-dc converter is a non-linear system, so an easy-to-understand mathematical description or dynamic model of the converter is not immediately evident. Such a model must first be derived, first by averaging the dc-dc converter to eliminate the effects of switching. This leaves a non-linear system, which can then be perturbed around an operating point, and then linearized to allow the use of well-understood linear system analysis.

The resulting dynamic model of the converter consists of a set of small-signal transfer functions that show how the variations of the input voltage and duty ratio affect the output
voltage of the converter. The feedback compensator is designed to stabilize the dynamic model directly or indirectly through the duty ratio to output voltage transfer function.

There are various analysis techniques to derive the small signal transfer function, most notably state-space averaging and PWM switch analysis.

In a converter operating in CCM mode switching ripple is small, so what we are interested in modelling the ac variation in the converter waveform. The model approach being discussed is applicable not only to buck converter but to any topology. Switching ripple in the inductor and capacitor waveforms are ignored by averaging over the switching period.

![PWM switch model](image)

Fig 3 – Buck converter with PWM switch

We are interested in creating a model of the PWM switch [Ref 3]. The switch network terminals can be defined by two voltages (V1, V2) and two currents (I1, I2). Two of the four terminal can be taken as independent inputs to the switch and the remaining two are dependent. The choice of which terminal is classified as independent is arbitrary, as long as inputs can indeed be independent in the converter. We can draw the waveforms at 1V1, 2V1, 1I1 and 2I1 over a switching period. If we define 2V and 1I as dependent variables and 1V and 2I as independent variables and then express the dependent variables 2V and 1I as a function of independent variables 1V, 2I and d duty cycle.

\[ V_2(t) = D(V_1(t) + \tilde{V}_1(t)) + \tilde{d}(t) V'_1 \]

\[ I_1(t) + \tilde{i}_1(t) = D(I_2(t) + \tilde{i}_2(t)) + I_2 \tilde{d} \]

Now the above equations can be expressed as shown below is equivalent model of PWM switch.

![PWM switch model](image)

Fig 4 – PWM switch model

PWM switch model can be incorporated into the buck converter thus allowing us to analyze the complete circuit.

![PWM switch model](image)

Fig 5 – Buck converter with PWM switch Model

For DC analysis we short the inductor and open the output capacitor and duty cycle \( \tilde{d} \) is set to zero. This will give us \( D=V_0/V_{in} \) dc gain. \( \tilde{V}_{cp} = V_{in} & V_{cp} = V_{out} \). For “ac” analysis we short the “DC” input source and analyse the circuit.

The duty ratio to output transfer function is the most important one, as it is utilized to design a feedback loop. It can be evaluated very simply as indicated below, where \( Z_L \) is the output inductor impedance and \( Z_C \) is the output capacitor in parallel with output load impedance.

\[ \frac{\tilde{v}_0}{\tilde{d}} = \frac{Z_C(s)}{Z_C(s) + Z_L(s)} \]

\[ \frac{\tilde{v}_{cp}}{\tilde{d}} = \frac{\tilde{v}_{cp}}{\tilde{v}_0} \]

This is a very straightforward approach but can get fairly complicated to evaluate if multiple output capacitors with different impedances are involved.

An alternate method is to write the differential equation for voltage across the output inductor and current through the output capacitor, and then solve it using matrix methods. This allows us to use software like MathCAD to provide the final results.

\[ L \frac{dI}{dt} = I(t) - (\text{Den}) - \frac{V}{r_c} + V_{cp} \tilde{d} \]

\[ C \frac{dv}{dt} = i(t) + \frac{\text{Den}}{r_c} + v_c (1 - \frac{1}{r_c^2 \text{Den}}) \]

\[ s X(s) = A X(s) + B d(s) \]

\[ s d X(s) = A X(s) + B d(s) \]

\[ (s I - A) x(s) = B d(s) \]

Duty cycle to Output transfer function can be evaluated using Cramer’s rule as indicated below, where \( \Delta \) refers to determinant of the matrix.

\[ \frac{v_o(s)}{\tilde{d}(s)} = \frac{\Delta(v_{cp})}{\Delta} \]
Output LC filter is a low-pass filter used to average the switched waveform. The feedback compensator consisting of an error amplifier and a compensation network is used to compensate the LC filter response and regulate the output voltage.

An intuitive way to look at the output LC is as follows. As frequency increases impedance of output capacitor decreases resulting in reduction in output voltage (open loop condition). Similarly, as frequency increases impedance of inductor increases, which tends to disconnect output from the input, each of these mechanisms resulting in with a slope of $-20\,\text{db/dec}$, this is referred to as a pole in the system. Thus one can see that the number of poles in the circuit is equal to the number of effective reactive elements. If two inductors are placed in series, it will perform as a single effective element and thus result in one pole, similarly if two capacitors are placed in parallel it will be an effective single capacitor and result in single pole. Output LC low pass filter will result in two pole response and depending upon damping or Q factor will result in peaking at the resonance frequency or (splitting the real poles as in the case of current mode control) instead of complex poles. Now as the frequency is increased, the output capacitor impedance will reduce and capacitor series resistor (esr) will tend to dominate. This will add a zero to the circuit. Thus Output LC filter gain performance can be visualized as shown below.

![Output LC gain response](image)

Fig 6 – Output LC gain response

VIII. CONTROL METHOD SELECTION

When high input to output ratio is required, which implies that low duty cycle or very narrow high side on-time pulses must be controlled. Duty cycle for buck converter is equal to $V_{\text{out}}/V_{\text{in}}$.

Various control methods in buck topology are used namely Voltage Mode (VM), Current Mode (CM), Hysteretic and Constant-On-Time (COT) control. Current mode control is the most favoured since it allows simple loop compensation, MOSFET switch protection due to inherent short circuit protection and its inherent line feed-forward compensation. Each approach has its pro’s and con’s.

Voltage Mode forces output voltage to be equal to reference voltage, requires additional circuitry for over current protection.

Hysteretic controllers respond quickly to load transients but its operating frequency is not constant with line and load variations.

COT also responds more quickly to load transients but will still have some variations in its operating frequency.

Current Mode control on the other hand has its issues also namely [Ref 7].

1. On-time of conventional current mode controller is limited by current measurement delays and the leading edge spike of the current sense signal. When the buck FET turns on and the diode turns off, a large reverse recovery current flows. This current can trip the PWM comparator. Additional filtering or leading edge blanking is necessary to prevent premature tripping of the PWM.

2. Conventional current mode is also susceptible to noise on the current signal thus limiting its ability to process narrow pulses.

3. As duty-cycle approaches 50% current mode exhibits sub-harmonic oscillations. Thus a fixed ramp signal (slope compensation) is added to the current ramp signal to address the issue.

4. Current mode control is a single pole system. Due to current loop, the poles of output LC filter split into two pole response and thus resulting in output inductor pole to be at much higher frequency. The current loop forces the inductor to act as constant current source. Thus loop remains as a single pole system regardless of the conduction mode.

5. By clamping the error amplifier, peak current limiting function can be implemented.

6. It also provides ability to current share multiple modules.

An improved version of current mode control “Emulated peak Current mode controller” LM3495 exhibits the advantages of current mode control, without the noise susceptibility problems often encountered from diode reverse recovery current, ringing on the switch node and propagation delays.

![LM3495 Emulated CMC buck converter](image)

Fig 7 – LM3495 Emulated CMC buck converter, Ref [7]
Figure 7 shows a buck converter consisting of Q1, D1, L1 and Cout. For synchronous buck converter diode can be replaced by a MOSFET. LM3495 creates a signal that accurately represents the current thru the buck switch Q1 without making a direct measurement. We can emulate the buck switch current by having a pedestal and a ramp. This is achieved as follows: by taking a sample and hold measurement of the diode current (by using a sense resistor) just before the turn-on of buck switch. The $2^{nd}$ part of the buck switch current is created with a current source proportional to Vin-Vout and a capacitor $C_{ramp}$. Value of $C_{ramp}$ can be selected to set the capacitor voltage slope that is proportional to the inductor current slope.

For duty cycles above 50%, current mode control is prone to sub harmonic oscillations. This is addressed by adding a fixed slope to the current sense ramp.

An added benefit of ECM is its “look-ahead current limiting”. Inductor current is measured near the end of conduction period and prior to turning on the buck switch. During extreme overload conditions, if the inductor current does not decay below the current limit threshold, buck switch will skip cycles to prevent current runaway condition.

Hysteretic regulator is the simplest of all the controllers. In this control method, the switch is turned on when the output voltage is below a reference and turns off the switch, when the output voltage rises above the reference voltage. The output ripple is a function of upper and lower reference threshold. One major disadvantage of this approach is very large variation of switching frequency as the input voltage varies.

Constant on-Time (COT) controller is a variation of hysteretic controller that reduces the variation of switching frequency as the input voltage varies. In this approach, a one-shot timer is inserted in the signal path. The period of one-shot is inversely proportional to the input voltage. On-time programming requires only one resistor connected to Vin. Upper threshold is eliminated and replaced by the programmed on-time. Lower threshold still requires the output voltage to have enough ripple to be distinguish the falling output turn-on point. The regulator comparator looks at the output voltage thru feedback divider. This approach will work properly, as long as output capacitor has enough esr at the switching frequency. It regulates the bottom of the output ripple, and when output decays below the bottom level, a programmed on-time is initiated, which forces the output higher than the feedback pin voltage.

In order to ensure minimum output ripple a variation that incorporates two capacitors and one resistor is highlighted. Vout is at “ac” ground. Switch pin switches between Vin and “ac” Gnd. Ripple is generated by RA and CA. Triangular waveform resulting at RA/CA junction is ac coupled to the FB pin. This configuration makes the design independent of output capacitor esr.

Fig 9 – COT converter with reduced output ripple

In summary, we have reviewed the synchronous buck converter and developed a small signal model that can be used to analyze the circuit. Also reviewed an intuitive look at the Output LC filter, reviewed the MOSFET switching behaviour and criteria’s used in selecting high side and low side MOSFET’s. Output inductor losses and issues relating to it. Finally, various control architectures are reviewed for high step-down ratio converters.


IX. REFERENCES

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Serial Powering of Silicon Strip Modules for the ATLAS Tracker Upgrade

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Abstract
The costs, difficulties and inefficiencies associated with the cabling of silicon detector systems are well known. Serial Powering is an elegant solution to these issues and is being actively pursued by the ATLAS Tracker upgrade community.

Demonstrator supermodules have been produced using the ABCD3TA chip from the present ATLAS SCT together with serial powering circuitry built from commercial components. Two 6 module supermodules have been built, and construction of a third supermodule to a 30 module design is in progress. Recent results from these supermodules will be presented.

I. INTRODUCTION
In the current generation of silicon detector systems for particle physics experiments, it has generally been considered best practice to power each detector module independently. For example, the present ATLAS SCT detector uses 4088 independent power supply channels and cable chains, one for each detector module. Physically routing the cables into the detector volume can be a major challenge in itself, and with return path cable resistances of order 4.5 ohms power efficiency is generally poor due to thermal losses in the cables [1].

Independent powering is not a practical solution for future detectors, where the total channel count may be expected to increase by a further order of magnitude. The ATLAS Tracker upgrade community is actively pursuing the serial powering alternative [2,3]. For chains of many modules with identical power requirements, serial powering offers potentially higher efficiency and lower mass than the use of DC-DC converters. An overview of tracker power distribution R&D is given in [4].

With serial powering, a number of detector modules are connected together in series to a constant current source. Each module has its own shunt regulator and power transistor combination to provide digital power and, as low power front end amplifiers typically operate at a lower voltage than their digital back ends, a linear regulator is used to provide analogue power. Each module will now be at a different potential with regard to the off detector readout electronics, so it is also necessary to provide AC or opto-coupling for all clock, command and data signals.

Demonstrator "supermodules" have been produced to two designs using the ABCD3TA chip from the present ATLAS SCT together with serial powering circuitry built from commercial components. Looking ahead, elements of the serial powering scheme have been incorporated into new, radiation hard, custom integrated circuits: the ABCN readout chip and the SPl serial powering chip. These developments and their application to future demonstrator supermodule will be outlined.

II. SIX-MODULE STAVES
Demonstrator staves have been made based upon a design for the Run IIb upgrade of the Collider Detector at Fermilab (CDF) [5]. Two such staves were built, one at LBNL and one at RAL. The stave assembled at RAL is shown in figure 1.
The mechanical stave, a carbon fibre and foam sandwich with embedded PEEK cooling tubes, was designed to support six silicon detector modules of detector dimensions 96.4 by 40.6 mm, the readout electronics being glued directly onto the detector surface. The silicon detectors have p-in-n strips of 75 μm pitch and, in common with the support staves, were spare components from the CDF Run IIb project. A new flexible bus cable with copper tracking and an aluminium screen layer and a new thick film hybrid were designed at LBNL and a companion serial powering board was designed at RAL. The resultant bus cables, hybrids and serial powering PCBs were all sourced from commercial vendors.

Each module comprises a silicon detector, the hybrid with four ABCD3TA [6] chips and the serial powering board. Both the hybrid and serial powering board are glued directly on top of the silicon sensor, and the resulting assembly is tested standalone before being glued to the stave. Communication with the modules utilises a number of LVDS signals passed down the bus cable: multi-drop clock and command buses which service all modules and six, single-drop data buses, one for each module. As each hybrid in the serial chain sits at a different potential with respect to the ground of the readout system, the LVDS signals are AC-coupled on each serial powering PCB. To facilitate better comparison between hybrid and module noise figures, a bare hybrid was mounted at one position of the pictured stave.

Early results from the RAL stave showed evidence of pickup between the detector bias traces on the bus cable and the silicon strips but, after a noisy high voltage supply had been eliminated from the test system, the results shown were obtained.

![Figure 2: Gain (mV/fC) for all channels of the six-module stave.](image)

Figure 2 shows the gain of each channel of the stave. The channels of each module are shown in a different colour. Figure 3 shows the output noise of each channel of the stave. In addition to the bare hybrid placed at position 4, it can be seen that a number of channels were deliberately left unbonded at the first position. The bonded channels return of order 1100 ENC and the unbonded channels 600 ENC. These figures are in agreement with the expected performance of the ABCD3TA chipset, and the absence of spikes demonstrates that there is no pickup from the bus cable.

![Figure 3: Input Noise (ENC) for all channels of the six-module stave.](image)
Additional studies were performed in which noise currents were injected directly into the serial powering chain, but no effect was noted upon the operation of the detector modules. Similarly if one module is left unbiased, the performance of the remainder of the serial module chain is not degraded. The first serially powered chains of silicon microstrip detector modules were found to operate cleanly under all tested circumstances.

III. THIRTY-MODULE STAVES

The next stage in the development chain was chosen to be the preparation of a thirty-module stave of dimensions more representative of the needs of the ATLAS tracker upgrade. For this project, a new thick film hybrid, bus cable and stave were designed by Carl Haber of LBNL.

The hybrid is shown in figure 4. At the top of the image there are six ABCD3TA readout ASICs. Along the bottom edge six smaller, commercial ICs may be seen: toward the left are three LVDS transceiver chips used as part of the AC coupling scheme for clock, command and data signals; toward the right are the analogue regulator, digital regulator and shunt transistor at the heart of the serial powering circuitry. In a final implementation the data AC coupling would be placed off hybrid at the end of a stave, and the remaining commercial ICs would be replaced by a single custom, radiation hard die with an estimated footprint of order ten square millimetres (see Section IV).

From figure 4 it may also be seen that the present circuit uses several large ceramic capacitors, six of which form part of the AC coupling circuitry. The size of these components is driven by the desire to build a stave of 30 modules each running at 4.0V, hence each coupling capacitor needs to be able to withstand a little more than 120V. In the final solution, using a smaller number of hybrids each running at lower voltage of 1.2 to 1.5V, the real estate needed for the coupling capacitors again will be considerably reduced.

Due to limitations imposed by the number of address pads available on the ABCD chip, the thirty-module bus cable provides six differential command buses, one to each group of five hybrids. Three differential clock signals are available, but there is also an option to use a single clock bus. The present bus cable is actually made in two sections connected together by wirebonds: vendors that can make the necessary length in one piece have subsequently been identified.

Before proceeding to the construction of the thirty-module stave, a “test vehicle” was assembled comprising thirty hybrids attached to a bus cable, but mounted on a copper clad board in place of the carbon fibre stave. The resultant thirty hybrid assembly, recently completed at LBNL, is shown in figure 5. This has provided a valuable tool for the study of signal propagation along the bus cable, and has led to small revisions being made to the communication scheme.

Work to populate the thirty-module stave continues. Figure 6 shows the stave when five modules had been mounted upon the support structure: at the time of writing a total of seven modules have now been mounted and operate reliably together. A preliminary result showing the input noise of all channels of one module operated on the serially powered stave is shown in figure 7. Although the programme has not yet been completed, to date the modules have been shown to perform in accordance with expectations.

Figure 4: Thick Film hybrid for six ABCD3TA chips with integrated Serial Powering circuitry.

Figure 5: Thirty Module Stave “Test Vehicle”: thirty-six-chip hybrids with integrated Serial Powering circuitry (without sensors).
Studies will continue, in part, by construction of a further prototype stave using kapton hybrids together with ABCN and custom serial powering circuitry together with n-in-p short strip sensors to ATLAS upgrade specifications. A first prototype of a custom constant-current source has recently been produced [9] which will be made available to power this and future staves, into which protection and monitoring features will be incorporated.

V. SUMMARY

Serial powering is an attractive concept for the powering of the upgraded ATLAS tracker, offering significant reductions in both power loss and material budget compared with other powering schemes. Staves have been built which have successfully demonstrated the application of serial powering to silicon strip detector modules, including the AC coupling of digital signals, with noise levels in agreement with individually powered modules of similar design.

Custom ASICs suited to the ATLAS tracker upgrade development programme have recently been submitted for fabrication, and will enable more fully integrated, serially powered staves to be produced. Studies of system features such as protection and monitoring schemes are now underway. Serial powering remains a most promising choice.

VI. REFERENCES

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[8] M. Trimpl et al., proceedings of this conference
[9] Private Communication, J. Stastny, Prague, Academy of Sciences of the Czech Republic
In this note the Detector Control System (DCS) for the power supply (PS) of the Monitored Drift Tube (MDT) chambers of the ATLAS experiment is presented. The principal task of DCS is to enable and ensure the coherent and safe operation of the detector. The interaction of the detector experts users or shifters with the detector hardware is also performed via DCS. This system monitors the operational parameters and the overall state of the detector, the alarm generation and handling, the connection of hardware values to databases and the interaction with the Data Acquisition system (DAQ).

In this note the Power System (PS) system as a Detector Control Subsystem is presented. Furthermore, it is outlined in detail what is the front-end to be controlled and how the architecture of the back-end is established.

I. DETECTOR CONTROL SYSTEM IN ATLAS EXPERIMENT

The work performed for the LEP experiments concerning the DCS, provided us with a useful and important experience and knowledge. On the other hand the implementation and integration of DCS in the LHC era, seems to be much different [1]. The basic change has to do with the introduction of new tools. The ATLAS Detector follows all the basic DCS guidelines of the LHC experiments, but in parallel, creates its own framework that facilitates the development and ensures further the homogeneity among the various ATLAS detector control subsystems.

A. TOOLS FOR DETECTOR CONTROL SYSTEM

In the late 90-s, the four LHC experiments decided to set up the Joint Controls Project [2]. After a detailed investigation a decision was made to use the commercial PVSS-II [3] as the Supervisor Control and Acquisition System (SCADA) tool to construct the back-end control systems. The very next step was the integration of a software framework based on the chosen package, in order to integrate, sequence and automate the control process of the LHC experiments.

B. PVSS-II

The PVSS SCADA system provides the following main components and tools:

1. A run time database.
2. Alarm generation and handling.
3. Graphical Editor.
4. Graphical Parameterization tool connected to the structure of the database.
5. Scripting language following C syntax.
6. Drivers for the connection between the PVSS and hardware.

C. JCOP and ATLAS framework

Given the increasing constraints on manpower, as well as the evident similarity in technical requirements for controls amongst the experiments, the project should enable more efficient use of resources to be made. The JCOP framework is an integrated set of guidelines and software tools which is used by DCS developers during the implementation of their own control system application. The framework includes as far as possible all templates, standard elements and functions required to achieve an homogenous control system. The framework provides guidelines for

- Integration and development
- Organization of libraries, panels, scripts
- Naming convention (PVSS system, library and panel names)
- Look and feel conventions (panel size, trend display, colors)
- Programming (control script)

Besides the main functionalities given above, the JCOP framework supports its users with even more specific tools. Such tools can be used for DAQ (Data Acquisition) connection, access control or connection with databases. But the most important offer of this framework that should be underlined, is that this is the main component for the organization and automation of the DCS of the back-end system.

Finally, it should be mentioned that except of the JCOP framework described above, the central DCS team of ATLAS experiment has established a special ATLAS DCS framework [4]. This framework provides the DCS developers with extra conventions, libraries and software tools and keeps the hole ATLAS DCS project as coherent as possible.
II. Monitored Drift Tube (MDT) Chambers and the Power Supply

A. The MDT chambers and the geometrical representation

The Monitored Drift Chambers (MDT) are the high precision tracking chambers of the ATLAS muon spectrometer. They are designed to operate reliably in a high rate and high background environment and to provide a good spatial resolution [5]. Each MDT consists of layers of drift tubes filled with a gas mixture of Ar:CO$_2$ (93% : 7%). Each drift tube is constructed with a grounded metallic cathode cylinder and an anode wire, passing through its center, held at a positive potential. A charged particle passing through the tube ionizes the gas along its path. The resulting electron avalanche travels towards the cathode, while the produced ions drift towards the cathode cylinder, generating a trigger pulse that is detected by the detector electronics.

The ATLAS Muon Spectrometer is composed of 1168 MDT chambers which is divided in two main regions, Barrel region, including 656 chambers, and the Endcap region, including 512 chambers, and two sides, side A and C with respect to the interaction point. The Barrel region (pseudorapidity $\eta < 1.2$) is formed of three concentric to the beam axis cylinders. They are positioned at a radii of about 5, 7 and 10 m. These cylinders are called layers and thus there is the Barrel Inner (BI) layer, the Barrel Middle (BM) layer and the Barrel Outer (BO) layer. Finally another useful geometric entity is the sector. The Muon Spectrometer is subdivided into 16 sectors around the $\phi$ coordinate[5].

In the endcap region (pseudorapidity $1.2 < \eta < 2.0$ ) every side is arranged in four vertical to the beam line disks at distances of about 7, 10, 14 and 21 meters from the interaction point. These disks are called again layers and thus there is the Endcap Inner (EI) layer, Endcap EE (EE) layer - for EE chambers, Endcap Middle (EM) layer and Endcap Outer (EO) layer. Endcap region like barrel is subdivided in 16 sectors [5].

B. Power Supply Hardware

The operating voltage for an MDT chamber is 3080 Volts. When LHC will reach full luminosity the maximum (depending on size and position) current requirement is about 0.7 mA [5]. One High Voltage channel supplies one chamber multilayer; each MDT chamber is divided into 2 multilayers. The Low Voltage required for the chamber electronics is 5 Volts. The signals coming from tubes are collected by the mezzanine boards [5]. Each mezzanine board processes signals coming from 24 tubes and requires 5V as an input voltage. The data coming from mezzanine boards are multiplexed in a digital board called CSM (Chamber Service Module). The CSM sends the data to be read out by the DAQ and needs 5V and about 1 A of current to operate too. One low voltage channel supplies in parallel two MDT chambers.

III. Power Supply Project Architecture

The amount of information exchanged between the hardware and the software demands a careful project architecture. This architecture incorporates the use of the computing power needed but also the internal organization of the DCS information inside each project.

A. Back-End Architecture

The back-end structure of Power Supply DCS of the MDT chambers is organized in abstract levels that are called stations. The first station, called Local Control Station (LCS) includes three machines. The first machine defines the first line of communication with the hardware. This machine houses the opc server as well as the opc clients that reads out the hardware values. The PVSS project of this machine is communicating with the server as well as the opc clients that reads out the hardware values. This machine houses the opc server as well as the opc clients that reads out the hardware values.
the PVSS projects of two more machines used for the PS control. One handles data from the Barrel Region MDT chambers while the other one handles data from the Endcap Region MDT chambers.

The Local Control Station of the PS DCS is connected to the next abstract level which is called Subdetector Control Station (SCS). This is a machine responsible for the whole MDT Detector Control Systems, including Gas, JTAG or Temperature DCS, etc. Through the SCS the project is connected to the top ATLAS DCS tree that is supervised from the top abstract level the Global Control Station machine as shown in Figure 2.

![ATLAS DCS Architecture](image)

**Figure 2: The overall ATLAS DCS architecture.**

**B. PVSS Project architecture**

As soon as the communication between the hardware and the DCS projects is established, a careful organization of the data inside the project is vital. The PVSS package, has a very powerful concept for the handling of storage and the data, called "datapoint". The datapoint concept ensures consistent processing and at the same time also allows flexible adaption to specific problems. User authorizations, alarm handling, history configuration, smoothing procedures and many other useful applications make use of datapoints.

In the Power Supply structure, two main datapoint types are used. The first defined during the development of the project has to do with the information connected to a MDT chamber. This datapoint type is called "fw_DUwithScript" and the datapoints themselves have the names of the chambers e.g. "BIS1A02". Under the chamber datapoint, there is the datapoint element of the ".mapping" the ".ML1", the ".ML2" and the ".LV"

The ".mapping" datapoint element, carries information about the mapping of the chambers' multilayer to the hardware channel. This information is a string that refers to the chain of the power distribution board the channel belongs to, the crate this board belongs to and the controller module this crate belongs to.

The ".ML1", ".ML2", ".LV" datapoint elements have two other elements below, the ".flags" and the ".tripHdl". The first element incorporates four boolean flags where in the case that one (or more of them) take the value "TRUE" the channel is switched off and is left in that state. For example in case of a gas problem, the "gasInterlock" flag is activated and the channel switch off, leaving the multilayer safe. The second element (".tripHdl") deals with trip handling and is used as a counter of trips happened in that multilayer and the trip recoveries applied after.

The second datapoint type used is called "fwCaenChannel". The structure of this datapoint type which structure is implemented from the JCOP framework and represents a Power Supply Channel.

**IV. Finite State Machine**

In the Detector Control Systems every ATLAS subdetector is treated as a finite state machine (FSM). This FSM is a modeling of the detector objects (parts or devices) where each object can have a finite number of states, transitions between these states and actions.

**A. State and Status Concept**

The DCS information of any node or any level and part of the hierarchy is decided from central ATLAS DCS and is propagated in two ways in parallel. The first piece of information refers to the state and the second one to the status. These two information routes, are distinct and supplement each other.

- The **State** information defines the operational mode of the system. (e.g. the chamber BIS1A02 is in state READY)
- The **Status** information gives an extra detail on how well is the system working in that particular state. (e.g. the chamber can be in state READY, but the status can be WARNING when reflects a temperature over the nominal value in a mezzanine card)

The concept of State and Status describes the project in more details. Moreover, another important attribute of this concept is the no-loss of the operational conditions. For example, let us suppose that a chamber is ramping up, an operation that can take up to 2 minutes, but during this time a reference voltage of its electronics declines from the nominal value. In this case the status information will carry the alarm information while the state will still be ramping up, giving this way a clear view of the shifter what actually is going on. There are four status names that are fixed and are used in all ATLAS subdetectors.

- **OK**: the system is working fine.
- **WARNING**: Low severity alarm, still the system can go on working.
- **ERROR**: High severity alarm, system has functionality problems.
- **FATAL**: Very high severity alarm, the system can not operate.

**B. FSM Types**

All devises, logical entities or partitions of the ATLAS detector are built from FSM "units" that are called FSM types. In order
to insert a device or a logical node in the FSM hierarchy you have to create first its prototype "unit". This "unit" is a set of FSM rules, state definitions, actions and color conventions. As soon as this prototype building block is ready, a name of the corresponding object is passed and then the FSM hierarchy is built. There are two different kinds of such units, the Device FSM and the Object FSM types.

C. FSM Device Types

The device types that usually represent the hardware inside FSM. For example a High Voltage channel, can have its own device type while a temperature sensor can have another device type. Nevertheless, in order to reduce the granularity and improve the performance, developers form a bigger entity like a chamber as a device unit. This device unit takes into consideration all the hardware that belongs to that chamber and sets the state and the status.

It is worth mentioning, the device unit, is the lower part of FSM, and deals directly with datapoints and PVSS script. On the other hand the Object types deal with the FSM rules based on SML language interacting with PVSS [1]. This language allows the detailed specification of objects, such as the state and actions and enables the finite state machine behavior of the objects inside the control system.

The name of the device unit type in Power Supply DCS project is fw_DU_withScriptATL_MDTPS_CHAMBER. This device unit that images a chamber, has nine different states:

- **ON**: The LV is ON and the HV is ON for both multilayers.
- **ON_50**: The LV is ON and the HV is ON for one Multilayer.
- **STANDBY**: The LV is ON and HV is OFF for both multilayers.
- **OFF**: LV and HV are OFF.
- **NO_LV**: HV is ON but LV is OFF.
- **RAMPING**: the LV is ON and the HV is Ramping Up or down.
- **UNKNOWN**: The chamber state is not defined; e.g. when the communication with the hardware is lost.

The finite state machine modeling of the power supply system, besides the states has actions too. For example if the device unit that represents a chamber is in a **STANDBY** state, the user has a set of actions to choose presented below:

- **SWITCH_LV_OFF**: Action to switch off LV, after this action the chamber is expected to be in state **OFF**.
- **SWITCH_HV_ON**: Action to switch on HV for both multilayers, after this action the chamber is expected to be in state **ON**.
- **SWITCH_ONLY_ML1_ON**: Action to switch on HV only for ML1, after this action the chamber is expected to be in state **ON_50**.
- **SWITCH_ONLY_ML2_ON**: Action to switch on HV only for ML2, after this action the chamber is expected to be in state **ON_50**.
- **RESET_TRIP**: Action to reset the trip of the chambers HV channel. The trip appeared when the channel is switched off but the Trip alarm remains. After this action, the trip alarm disappears.

The other states of the device units have their set of actions too. A MDT chamber is represented by this device unit so all the manipulation of the chamber is performed via these FSM actions.

D. FSM Object Types

The object types are types that represent logical objects or parts inside a FSM. These parts usually follow a geometrical segregation. For example a sector of the MDT chambers can be represented as an object type. Another important logical entity represented from object types are the partitions. Partitions inside the FSM are represented from the object type of partitions.

In detail, in the PS project there are:

- The **MDT_SECTOR_PS** object type that represents the sectors as logical objects. This object type defines the state of the sector according to the state of its children - its chambers.
- The **MDT_PARTITION_PS** object type that represents the partitions as logical objects. This object type defines the state of the partitions according to the state of their children - their sectors.
- The **ATLAS_STATUS** object type that propagates the information for all the various nodes of the hierarchy. The ATLAS_STATUS object is the same for both the sector and partition level.

E. FSM transition diagrams

State diagrams are a graphical representation of finite state machines. These diagrams (Figure 3) are useful during the development of the finite states machine making the code transparent among various FSM developers.

Figure 3: The FSM transition diagram for the object type (left) and the status object (right) of a MDT partition.
V. ALARM HANDLING

The MDT Power Supply DCS project deals with the hardware for the power supply of the chambers. One very important role of the project is the propagation and handling of various alarms coming from the hardware. These alarms, according to their severity, can be used from preventive actions to activating interlock procedures.

A. Channel Alarm

Usually an alarm of the Power Supply system comes from the power supply channel itself. One channel is responsible for the supply of one MDT multilayer. All the information concerning the state of a channel comes from a single OPC item, called status. This can be achieved because this item has a special 16 bit pattern indicating the channel status as shown in Table 1.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0)</td>
<td>ON/OFF</td>
</tr>
<tr>
<td>(1)</td>
<td>Ramp Up</td>
</tr>
<tr>
<td>(2)</td>
<td>Ramp Down</td>
</tr>
<tr>
<td>(3)</td>
<td>Overcurrent</td>
</tr>
<tr>
<td>(4)</td>
<td>OverVoltage</td>
</tr>
<tr>
<td>(5)</td>
<td>UnderVoltage</td>
</tr>
<tr>
<td>(6)</td>
<td>External Trip</td>
</tr>
<tr>
<td>(7)</td>
<td>Over HVmax</td>
</tr>
<tr>
<td>(8)</td>
<td>Internal Trip</td>
</tr>
<tr>
<td>(9)</td>
<td>External Disable</td>
</tr>
<tr>
<td>(10)</td>
<td>Calibration Error</td>
</tr>
<tr>
<td>(11)</td>
<td>Unplugged</td>
</tr>
<tr>
<td>(12)</td>
<td>UnderCurrent</td>
</tr>
<tr>
<td>(13)</td>
<td>OverVoltage Protection</td>
</tr>
<tr>
<td>(14)</td>
<td>Power Fail</td>
</tr>
<tr>
<td>(15)</td>
<td>Temperature Error</td>
</tr>
</tbody>
</table>

Leaving out the first three bits that deal with the information about the operational state of the channel, the rest are connected with alarms. For example, if the bit 9 is raised this means that the channel tripped, which is an indication of bad gas flow in the multilayer. All these alarms belong to the alarm classes such as warning, error or fatal according to their real severity.

B. Board Temperature Alarm

One other alarm item, provided directly from the power supply boards, is the board temperature alarm. The boards are equipped with a temperature sensors expressed in degrees Celsius. Due to the importance of this alarm, there are two levels of interlock actions taken on the board. The first temperature check is done in the software level. The project continuously monitors these temperature values and in the case of an alarm an interlock mechanism is activated switching off the power supply. Furthermore, a hardware interlock mechanism is implemented to protect overheated boards.

C. Alarm Screen

The alarm screen is a self-contained panel for the display of all various alarms that can occur in the detector. This screen is of great importance and the first to look in case of any abnormal response. The alarms contained can be filtered in various ways according always to the importance and the user needs. The alarm screen in parallel with the ATLAS DCS Operation interface (OI) are the two active interfaces that the DCS user needs in order to operate the experiment from the DCS side point of view.

VI. CONFIGURATION DATABASES

The MDT PS DCS project is also connected to a configuration DataBase (DB). This DB is responsible for the storage of the device properties (e.g. trip current limits, trend smoothing details, archiving configuration) and settings (e.g. alarms ranges, output values, operational voltages). The PVSS project uses a tool that is developed from the JCOP framework, called "configuration DB tool".

The concept of recipes is the main idea behind the configuration DB tool. The recipes are a set of predefined settings under one name - the recipe name. The DCS expert, in collaboration with the detector experts, gathers all the appropriate settings that characterize the state of the detector (at least from the Power Supply side of view) and creates a recipe with a meaningful name. This recipe is saved in DB and is ready to be used by the shifter. The panel, Figure 5, is the interface to the configuration DB. The shifter can choose one of the predefined recipes from a drop down list. Moreover, this interface, allows us to create a new recipe, under the name "custom". In this case the user can choose a set of chambers to apply the new settings with their
corresponding values. The configuration DB tool is powerful enough to ease the detector manipulation from DCS side, while at the same time ensuring coherency and safety.

C. ATLAS DCS Secondary panel

This is a second small panel, shown at the bottom left and provides information for the chosen workspace. This panel provides a navigation tool so one can use it to find supplementary information parallel to the one supplied from the main panel.

A main care of ATLAS DCS is to offer an effective way for the OI of the numerous subdetectors/subsystems of the ATLAS experiment. All the relevant DCS information is organized in a single screen window. This interface is equipped with a navigation tool that lets the user navigate through all the DCS data that come from these different subdetectors/subsystems and are displayed in panels as shown in Figure 6.

A. ATLAS DCS Navigation Buttons

In order to reach easily and quickly any part of the control hierarchy a navigation facility is been integrated within the OI. This navigation tool is shown at the top left of the screen. It consists of four self-explained buttons: "backwards", "forwards", "home" and "go up one level", that allow the navigation to the control node that one is interested to monitor or to take action.

B. ATLAS DCS Main Panel

This is the panel which provides the user with all the basic information concerning the workspace chosen previously with the navigation tool. From this panel the user can see the DCS data in various forms like: numbers, bar trends, tables, plots or geographical representations of the subdetector with the appropriate state connected DCS colors.

VII. OPERATION INTERFACE

The low and high-voltage Detector Control System of the ATLAS Monitored Drift Tubes is presented. Both voltage systems follow a common architecture. The developed system has been successfully used during the commissioning and integration phases of the muon spectrometer. It is ready for the LHC data taking.

REFERENCES

Noise Susceptibility Measurements of Front-End Electronics Systems

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Abstract

The conducted and radiated noise that is emitted by a power supply constrains the noise performance of the front-end electronics system that it powers. The characterization of the noise susceptibility of the front-end electronics allows setting proper requirements for the back-end power supply in order to achieve the expected system performance. A method to measure the common mode current susceptibility using current probes is presented. The compatibility between power supplies and various front-end systems is explored.

I. INTRODUCTION

The developments of new particle detectors for the LHC and the sLHC experiments are setting increasingly demanding requirements to the front end electronics that reads out and processes the physics data that they produce, with the aim to achieve high levels of performance in terms of resolution and accuracy. This performance is limited by the system intrinsic noise, but also by external sources of disturbances. The use of modern microelectronic technologies with lower operating voltage, with higher clock speeds and more dense input-output connectivity make the front-end electronics systems more sensitive to these disturbances. A more comprehensive and systematic approach of the electromagnetic compatibility issues that affect the front end systems becomes necessary so that the expected detector performance is achieved \cite{1}[2].

The power supplies have been identified, at many occasions during the commissioning phases of the LHC experiments, as a dominant source of disturbances that affect the resolution of the front-end systems \cite{3}. However, the compatibility between a power supply system and a front-end system is better addressed at the design stage, with the characterization of the susceptibility of the front end system to external noise \cite{4}, as part of a coherent development strategy \cite{1}. Knowing beforehand the noise susceptibility of a system allows implementing optimal corrective actions while the establishing the EMC requirements for a compatible power supply system.

The characterization of the conducted noise susceptibility of a system is achieved using well documented measurement techniques \cite{5}[6]. However, this measurement requires the use of particular instruments to allow the coupling of reference disturbances into the system. Also, physical constrains of the tested system often make the coupling difficult. Front-end power converters emit also near field radiated noise; a simplified method to explore the front-end susceptibility to radiated noise is proposed. The methods are applied to the front-end electronics of the absolute luminosity monitor for ATLAS (ALFA) and on the TOTEM detector front-end. Susceptibility curves are obtained and the dependencies between the noise and the system are interpreted. On the basis of the susceptibility figures, the noise properties of the power supplies can be set for each system.

II. NOISE COUPLING INTO FRONT-END SYSTEMS

The front-end systems are exposed to electrical disturbances of different kind, i.e. electrostatic discharges, overvoltage or undervoltage fast transients on all the input and output ports, conducted noise carried by all the cables, and radiated noise incident to the system (Figure 1). To achieve a robust and reliable system, its design has to take into account these disturbances, within a well defined electromagnetic compatibility plan that sets the limits that the system must be able to tolerate \cite{1}[2].

![Figure 1: Noise coupling paths.](image)

III. TESTING FOR CONDUCTED SUSCEPTIBILITY

A. Bulk Injection Method.

The front-end systems are exposed to common and differential mode noise voltages and currents on all their interconnection ports. They transfer each of these noise contributions into system noise through susceptibility transfer functions (in the frequency domain) associated to each disturbance for each port (Eq. 1).

\[
n(f) = I_{CM}(f) \cdot H_{CM}(f) \quad \text{[Eq. 1]}
\]

The common mode currents $I_{CM}$ have been identified at many occasions as being a dominant source of noise that degrades the performance of a front-end system \cite{2}[3]. These common mode currents often find their way into the system through the power ports.
They propagate deep inside the front-end circuitry, where they can become a significant source of disturbance when switched mode power supplies are used.

The measurement of the front-end susceptibility to conducted noise is carried out with the injection of known common mode or differential mode currents in the tested ports over a given frequency range using bulk injection probes and appropriate arrangement of the cables [2][6]. The disturbance is coupled inductively (Figure 2), and the magnitude of the injected current is a function of the circuit impedance. At low frequencies, the inductive coupling is weak, while at large frequencies the circuit inductance limits the injected current. Because of this, large voltages are often needed to drive the bulk injection probe in order to get the desired current, sometimes using specialized radiofrequency power amplifiers. Using a high purity RF generator and a suitable bulk probe, non distorted disturbances can be applied over a broad frequency range at constant amplitude. The injected current has to be monitored, typically with a second calibrated current probe.

![Figure 2: Injection of conducted noise.](image)

The ratio between the output system noise and the injected current sets the system susceptibility at the tested frequency. The full susceptibility figure is obtained in the frequency domain sweeping the test frequency from 100 kHz to 100 MHz at constant current.

**B. Susceptibility of the ALFA Prototype.**

The described measurement method was exercised to determine the common mode susceptibility of a front-end prototype of the absolute luminosity monitor for ATLAS (ALFA) [7]. This system is composed of a matrix of 5x5 front-end photomultiplier modules (PMF). The PMF incorporates a front-end ASIC (MAROC2) [8] that perform the pulse shaping, amplification and discrimination of 64 pixels according to configurable gain and threshold settings (Figure 3). The dynamic range of each MAROC preamplifier is set to 5 pC (30 p.e.) with a declared noise of 5 fC (ENC), that allows for single photoelectron resolution using a fast unipolar transimpedance shaper with a peaking time of 20 ns. The signals are acquired and transmitted to the motherboard by an FPGA embedded in the PMF. The motherboard packs and transmits the data through a GOL link (Figure 4).

Three electrical ports are found on the ALFA motherboard (Figure 4):

- 12VDC input power, feeding the motherboard auxiliary circuitry.
- 5VDC input power, feeding the FPGAs and the front-end ASIC in the PMF through linear regulators.
- CANbus interface for the ELMB, isolated with optocouplers.

The two power ports are fitted with common mode and differential mode filters with an insertion loss optimized between 10 MHz and 100 MHz.

The sensitivity of the PMF against noise is first determined by means of a threshold scan that delivers an S-curve of the front end ASIC (Figure 5). The sixty-four front-end pixels cross the noise threshold for a DAC setting comprised between 89 and 94. The susceptibility curves must be obtained for that range in order to observe the threshold effect on the susceptibility characteristic.

![Figure 5: ALFA front-end intrinsic noise versus threshold.](image)
A threshold is then set and common mode currents are injected (Figure 2) using an ETS-Lindgren-91256 probe, with amplitudes up to 10 mA and frequencies comprised between 150 kHz and 100 MHz, first on the 12V port, and after on the 5V port. The injected current was monitored with an ETS-Lindgren 91550-1L probe (Figure 2). The characterization is made at a nominal gain of the MAROC2 preamplifiers, set to 10 for different threshold settings.

The injection on the 12V power port did not reveal any susceptibility to common mode currents in the whole frequency range for the maximum amplitude of 10 mA. However, non negligible system noise was observed when injecting common mode currents on the 5V port that powers the front-end ASICs. The conducted noise develops the largest disturbance at the source of the detector signal, before its amplification, at the MAROC2 inputs.

The susceptibility characteristic is obtained at a constant current, sweeping the frequency from 150 kHz to 100 MHz. For each frequency, for each threshold setting, and for each pixel in the tested PMF the noise hits are counted for $10^4$ events. The resulting figure, obtained for a current of 10 mA and a threshold DAC of 89 allows putting in evidence a susceptibility peak at 25 MHz (Figure 6), in agreement with the frequency response of the transimpedance front-end preamplifiers that has a peaking time of about 20 ns. The measurements are repeated for different values of the injected common mode current.

Having identified the frequency at which the peak of susceptibility occurs, the dependency of the observed noise with respect to the injected current and to the threshold is estimated (Figure 7). The system is sensitive to common mode currents greater than 7 mA for thresholds settings greater than 88. The susceptibility at critical frequencies can be explored at nominal threshold and gain conditions, for different amplitudes of the noise current (Figure 8).

The physics requirements set the gain and threshold settings together with the maximum acceptable noise rate. With these parameters in hands, it is possible to extract the maximum common mode current that a power supply is allowed to emit into the system and select it (or filter it) accordingly, for instance with a limit of 7 mA between 10 MHz and 35 MHz in the ALFA front-end system.

IV. TESTING FOR RADIATED SUSCEPTIBILITY

The electric and magnetic fields radiated from devices in the vicinity of the front-end circuitry, located inside their shielding envelope, expose those to radiated near field couplings that degrade the system performance. The accurate measurement of radiated susceptibility requires the use of complex instrumentation that is often unavailable to the front-end designers. A simple method to qualitatively explore the front-end susceptibility to radiated near fields is presented. The methods are exercised on the production test setup of the TOTEM front-end.
A. The TOTEM Front-End.

The detector module used is part of the silicon strip TOTEM detector designed for luminosity monitoring. The front-end strips are coupled to four VFAT2 ASICs that shape, amplify and discriminate the strips signals. The discriminated signals are packed and transmitted by the hybrid board as LVDS signals. A test board [9] allows testing the hybrids prior to their installation. The test system is controlled by a dedicated software tool that configures the detector and analyzes the transmitted data.

The system has been exposed to electric and magnetic field sources with the aim to understand its compatibility with DC to DC converters located in the front-end area [10].

B. Susceptibility to Magnetic Field.

A major concern when embedding DC to DC converters is the magnetic field emitted by the coils at the switching and harmonic frequencies that can introduce noise in the preamplifier inputs. Electromagnetic simulations carried out with Ansoft Maxwell indicate that the magnetic field emitted along the axis of a coil decays very fast with the distance [11], being reduced by two orders of magnitude at 10 mm of the coil edge. To verify this, an air coil (Coilcraft 538 nH air core) was driven with a 0.5A, 1 MHz signal, pointing at different locations and angles around the front-end system (Figure 9). At these locations and angles, the S curves parameters were evaluated by the test platform for every channel. The dispersion of the slopes is used to estimate the susceptibility to the magnetic field at a nominal and fixed threshold.

When exposing the bondings of the VFAT chips, an alternating noise pattern is observed, that is correlated with the staggered arrangement of the bonding on the hybrid. When exposing the strips, the VFAT channels develop large noise along a pattern that is centred along the coil axis. In both cases (Figure 10), large noise amplitudes are observed for the channels exposed to the fields (VFAT#1).

The coupling between the coil and the strips decays fast with the distance, becoming negligible beyond 20 mm. Similarly and as in the case of conducted noise, the coupling between the coil and the front-end inputs is function of the frequency (Figure 11). However, the coupling is strongly reduced by the addition of a shield, either around the coil (Aluminium foil) or in the form of a copper plane between the coil and the sensitive area (Figure 12).

<table>
<thead>
<tr>
<th>VFAT#</th>
<th>Nominal Noise</th>
<th>Bondings</th>
<th>Sensor</th>
<th>Far distance [mm]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Oblique</td>
<td>Straight</td>
<td>Parallel</td>
<td>Straight</td>
</tr>
<tr>
<td>1</td>
<td>1.76</td>
<td>2.3</td>
<td>12.87*</td>
<td>10.05*</td>
</tr>
<tr>
<td>2</td>
<td>1.81</td>
<td>2.14</td>
<td>3.96</td>
<td>3.97</td>
</tr>
<tr>
<td>3</td>
<td>1.68</td>
<td>1.88</td>
<td>2.20</td>
<td>2.94</td>
</tr>
<tr>
<td>4</td>
<td>1.56</td>
<td>1.70</td>
<td>1.87</td>
<td>2.18</td>
</tr>
</tbody>
</table>

*not an S curve anymore

Figure 10: Magnetic coupling noise summary. The noise is expressed as the average slope dispersion of the S curves of all channels for each VFAT.

![Figure 9: Magnetic field coupling test setup.](image)

![Figure 11: Distance (top) and frequency (bottom) dependency of magnetic field susceptibility.](image)

![Figure 12: Shielding effectiveness of magnetic field coupling.](image)
The voltage developed between the coil pins is a noise source that radiates electric field towards the system: complementary tests to evaluate the susceptibility to electric field must complement the magnetic field susceptibility test described here.

C. Susceptibility to Electric Field.

A reference signal of 3.4V at 1 MHz was applied to different geometries to expose the front-end system to electric fields, through capacitive coupling (Figure 13). The applied signal is referred to the ground level of the front-end system. The use of a shield provides a significant but not complete reduction of the coupling (Figure 14).

D. Compatibility with a power converter.

The observations concerning the electric and magnetic field couplings made on the TOTEM front-end predict a low sensitivity to noise sources at distances greater than 20 mm. The same system has been exposed to the conducted and radiated noise emitted by a DC to DC converter (46 dBμA peak CM at 1 MHz) used to power the front-end hybrid (Figure 15).

The system was found to be insensitive to the combined emissions at three different locations in the close vicinity of the bondings and of the strips (X1, X2 and X3 on figure 15). An increase was only visible when the converter was placed straight on the top of the detector at about 15 mm, and only on the VFAT chip under the unshielded inductor.

V. CONCLUSIONS

The noise susceptibility of front-end systems is a key parameter that can be evaluated with accurate measurements. The characterization of the conducted susceptibility provides accurate results that can be used to set up appropriate filters and to specify a compatible power supply system. The radiated susceptibility can be evaluated with simple setups, allowing to qualitatively discriminate between electric and magnetic couplings and to set geometrical compatibility boundaries. The method allows exploring the effectiveness of shields.

VI. REFERENCES

Overview and Electronics Needs of ATLAS and CMS High Luminosity Upgrades

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Abstract

The LHC will begin collisions in Spring 2009, and build up to nominal luminosity \((1.0 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1})\) over the next few years. This will be followed by a continuous programme of improvements leading eventually to a ten-fold increase above nominal with the super-LHC (sLHC). Within a few years of operation, the LHC experiments should discover or rule out a Standard Model (SM) Higgs, and could find supersymmetric particles if they exist below about 1.5 TeV mass. Several other discoveries are possible. However detailed knowledge of any new particles will be needed to understand exactly what the physics behind them is. Large data sets will be needed for this; these will also allow the mass limits for discovery of new particles to be increased. Upgrades to the general purpose experiments ATLAS and CMS will be necessary to deliver these large data sets with good performance. This paper presents some of the physics goals of the upgrade, LHC machine plans, the schedule, and summarises the changes and challenges for the detectors at the sLHC.

I. INTRODUCTION

Most measurements at the LHC will benefit from larger data sets, though not all since some will be systematics limited. The LHC is expected to increase in performance, initially to sets, though not all since some will be systematics limited. Within a few years of operation, the LHC experiments should discover or rule out a Standard Model (SM) Higgs, and could find supersymmetric particles if they exist below about 1.5 TeV mass. Several other discoveries are possible. However detailed knowledge of any new particles will be needed to understand exactly what the physics behind them is. Large data sets will be needed for this; these will also allow the mass limits for discovery of new particles to be increased. Upgrades to the general purpose experiments ATLAS and CMS will be necessary to deliver these large data sets with good performance. This paper presents some of the physics goals of the upgrade, LHC machine plans, the schedule, and summarises the changes and challenges for the detectors at the sLHC.

II. PHYSICS MOTIVATION

Within a few years, the LHC should have delivered enough luminosity for discovery of the Standard Model (SM) Higgs if it exists in the mass range 100 to 1000 GeV; and if not seen, it will be ruled out at 95 \% confidence level. The lightest supersymmetric particle could be observed if its mass is below about 1.5 TeV. Several other discoveries are possible over the following years. However, much more data will be needed to really probe what has been discovered. The physics opened up at the sLHC will depend on just what is found, and has been reported in several places, for example [1] and [2].

If a Higgs is found, it will be important to see if it behaves as a SM Higgs. Higgs decay branching ratios are determined in the SM; any deviation would signal new physics. While some ratios will already be systematics-limited, many will improve significantly with more data. Improvements of up to a factor two are possible in the precision of measurements of ratios of decays to gauge bosons, with somewhat less in ratios of decays involving top quarks. Couplings among the gauge particles are characteristic of the electroweak theory. There are 5 extra coupling parameters possible in a general model of Triple Gauge Couplings. Measuring any deviation from the SM value would signal new physics. Table 1 shows the significant improvements achievable in the precision with sLHC statistics. The Higgs self-coupling is also important. The LHC will have very few events with two Higgs particles, limiting the precision; the sLHC can make a large improvement reducing the uncertainty in the deviation from SM coupling \((\lambda - \lambda_{SM})/\lambda_{SM}\) from 200 \% to about 10 \% for the most favorable mass Higgs.

Table 1: Precision of measurements of Triple Gauge Couplings with different integrated luminosities from [2]. In most cases, sLHC statistics give considerable improvement.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>100 fb(^{-1})</th>
<th>1000 fb(^{-1})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\lambda_z)</td>
<td>0.0014</td>
<td>0.0006</td>
</tr>
<tr>
<td>(\Delta\kappa_z)</td>
<td>0.0028</td>
<td>0.0018</td>
</tr>
<tr>
<td>(\Delta\kappa_{\gamma})</td>
<td>0.034</td>
<td>0.020</td>
</tr>
<tr>
<td>(\Delta\kappa_{\gamma_2})</td>
<td>0.040</td>
<td>0.034</td>
</tr>
<tr>
<td>(g_1)</td>
<td>0.0038</td>
<td>0.0024</td>
</tr>
</tbody>
</table>

If no Higgs is found, then something must happen before or around the TeV scale. Strong \(WW\) or \(ZZ\) scattering for example via a resonance at 1.5 TeV would only produce a few events at the LHC, but a clear discovery at the sLHC, with \(S/\sqrt{B}\) around 10.

Several models predict more than one Higgs, for example in MSSM models there are five. Searching for more than one Higgs is therefore important. The sLHC can extend the region in the \((m_A, \tan \beta)\) plane in which more than one Higgs will be seen.

Searches for supersymmetric partners will increase the dis-
covery region or push the limits further. Typically the reach can increase 40%, with the limit for the lightest $m_{1/2}$ rising from about 1 to 1.5 TeV. If supersymmetric particles are discovered at the LHC, then spectroscopy to measure heavier partners will require the larger data set of the SLHC.

Several new forces have been proposed, resulting in new heavy gauge bosons $W'$ and $Z'$. The mass range for discovery can be extended by around 20% at the SLHC. If already discovered at the LHC, the SLHC should provide precise measurements helping to distinguish between the models, for example on decay widths.

In a few years from now, much more will be known about physics at the TeV scale, and we can expect a rich variety of physics goals requiring the SLHC machine.

III. Evolution of the LHC Accelerator and Injectors

The LHC will start collisions in 2009 at low luminosity and ramp up to 40% of nominal luminosity in 2 to 3 years, limited by the absence of the full collimation scheme. The collimators will be completed in the 2010-11 shutdown, and allow further rises in luminosity up to nominal.

Upgrades to the LHC and its injectors will allow further improvements planned in stages known as Phase-I and Phase-II.

Phase-I will introduce two major changes in the 2012-13 shutdown: new focussing magnets with larger apertures allowing a $\beta^*$ reduction from 0.55 m to 0.25 m; and a new linac, called Linac4, allowing brighter beams to be fed through the injector chain and into the LHC. This will allow further increases in luminosity up to a maximum of about 3 times nominal.

Phase-II will introduce more new accelerators into the injector chain: a superconducting proton linac SPL to replace the PsBooster; and a new superconducting proton synchrotron, PS2, to replace the current PS. Superconducting magnets replacing the current SPS magnets are also envisioned later on. Each new component will allow brighter, more reliable operation, enabling the LHC current to go well beyond the so-called Ultimate level of $2.3 \times 10^{34}$ cm$^{-2}$s$^{-1}$ for which the LHC was designed.

The higher currents will be supplemented with other novel elements. Just which are best is being evaluated. The Large Piwinski Angle (LPA) scheme uses a high bunch charge ($4.9 \times 10^{11}$ protons compared to $1.15 \times 10^{11}$ at the LHC) in bunches 50 ns apart, and a large crossing angle to reduce the beam-beam effects. Wire correctors are needed with this scheme to further reduce the beam-beam effects. The Early Separation scheme avoids the geometric reduction in luminosity caused by the large crossing angle by allowing head on collisions and rapidly separating the beams with dipoles close to the interaction point. The placement of machine magnets deep inside the detectors is technically difficult, can cause increased backgrounds in the experiments, and reduce forward calorimetry performance. By using Crab cavities, which rotate the bunches away from their direction of motion, a crossing angle can remain while still minimising the geometrical loss. These can allow the dipoles to be further from the interaction point, or even be omitted all together. These Crab schemes can achieve the luminosity increase without increasing the machine current beyond ultimate, and run at 25 ns bunch spacing. Whichever scheme is adopted, the expectation is for the SLHC to achieve a luminosity of $10 \times 10^{34}$ cm$^{-2}$s$^{-1}$. Both schemes give very high pileup rates: the LPA scheme will give 400 pp scatterings (dissipative plus inelastic) per bunch crossing at the start of a spill; the Crab schemes will give 300.

Luminosity levelling schemes are also under investigation. These detune a parameter such as bunch-length, Crab rotation, or $\beta^*$ at the start of a spill to reduce the peak luminosity. As the bunch charge reduces, the parameter is tuned to maintain a constant luminosity. Levelling is attractive at the SLHC where the spill length can become shorter than the machine filling time: the integrated luminosity need not be much lower than the maximum. Furthermore, some of these schemes reduce the beam-beam interaction, allowing a higher machine fill: this allows luminosity levelling to actually increase the integrated luminosity at a much lower peak pile-up rate, and is clearly very interesting to the experiments.

Recent discussions between the LHC, ATLAS and CMS have led to an understanding of the most likely scenario for the evolution of the LHC luminosity. Whilst there are many uncertainties, this represents the best current estimate [3]. Figure 1 shows the peak luminosity evolution, and figure 2 shows the anticipated integrated luminosity assuming 60 fb$^{-1}$ per year of nominal luminosity running. This value takes into account the pp running time planned for the LHC, and typical fill times allowing for machine down-times.

The machine will require a longer shutdown than usual (8 compared to 5 months) for the installation of Phase-I equipment; the experiments will need a long shutdown at the end of 2016, consisting of a year’s running time plus two winter shutdowns (18 months total) in order to install major new detector elements. The experiments will work towards this schedule, adjusting their programmes as experience with the machine evolves.
IV. DETECTOR CHANGES

ATLAS and CMS detectors will have to cope with extremely demanding conditions at the sLHC: these are greatest for the B-layers. Depending on the final scheme, there could be up to 30 charged tracks per cm$^2$ per bunch crossing or 13,000 tracks. After 3000 fb$^{-1}$ data recorded the integrated ionising dose will be tens of MGray and the non-ionising dose will be over $10^{16}$ 1 MeV neutron-equivalent cm$^{-2}$. These doses tail off with distance, but remain much higher than the current detectors were designed for.

Some high-mass physics such as $W'$ and $Z'$ involve very high energy particles with little background, and can tolerate some reduction in detector performance. However, most channels of interest need the current resolution, efficiency and fake rates maintained or improved. For example, figure 3 shows a decay chain of supersymmetric particles involving many particles in the final state, which are relatively low in energy. These final state particles include neutralinos, $b$-quarks, electrons, muons, and jets. So missing transverse energy resolution, vertexing performance, electron identification and resolution, muon tracking and the trigger all need to be maintained. Studies of $WW'$ and $Z Z$ scattering need measurement of very forward jets ($\eta \approx 4.5$) and central jet vetoes, requiring calorimetry performance to be maintained even at the very forward regions.

Despite the much increased luminosity, most of the ATLAS and CMS detectors can stay and are expected to perform well throughout the life of the sLHC: all magnets, and most of the muon detectors and colorimeters will stay. Both will need completely new inner trackers: they will have reached their radiation limit, have too low a granularity for pattern recognition at $10 \times 10^{14}$ cm$^{-2}$s$^{-1}$, and have insufficient bandwidth to readout the data. Note that even in the absence of an sLHC programme, continuing ATLAS and CMS will require new inner trackers around 2017 due to radiation damage.

A. Phase-I Detector Upgrades

The Phase-I LHC upgrade will lead to instantaneous luminosities of $3 \times 10^{34}$ cm$^{-2}$s$^{-1}$ and a data set of about 700 fb$^{-1}$. The B-layers of both experiments will not survive this. Also they will lose hits because of limited bandwidth in the front-end readout chips: The CMS B-layer will be about 12% inefficient, and the ATLAS B-layer will be somewhat worse, on a very steeply rising inefficiency curve. Therefore both experiments plan new B-layers. The best opportunity to insert these is the 6 to 8 month shutdown foreseen for the Phase-I improvements in 2012-13. CMS is also considering more ambitious plans, with a range of options under study including replacing the whole pixel detector.

There are several other changes planned, such as adding some forward muon trigger chambers in CMS which were staged for financial reasons but become very important at higher luminosities. In both experiments, the triggers will develop continuously, taking advantage of cheaper processing power. New ideas such as topological triggers, which combine trigger items, are investigated; also at ATLAS a study is underway for a fast track trigger using associative memory to recognise hit patterns from tracks using data read-out at the level-1 trigger, and providing level-2 with high quality track parameters early on. CMS investigates the use of silicon photo-multipliers (SiPM, which are avalanche photo-diodes) to replace their tile-calorimeter hybrid photo-multipliers. These are very low noise reducing false triggers, large dynamic range allowing muons to be seen, and allowing more segmentation which can benefit calibration especially if radiation damage reduces light output of front scintillators more than others.

B. Phase-II Detector Upgrades

For Phase-II, both experiments will replace their entire inner trackers; also changes in the forward calorimeters and forward muon systems are under investigation. These changes need a long shutdown, and both experiments have agreed to do the changes in 18 months. This is challenging, and requires care-
ful design and planning early on.

1) Inner Trackers

The radiation damage at the inner-most region, the B-layer, will be much higher than for any LHC active sensor. This requires either new technology for the sensors to survive the full dose after 3000 fb⁻¹, or planar silicon can be used and replaced frequently. Several technologies are under investigation: diamond, 3D-edgeless sensors, thin-silicon, and Gossip (micropattern gas detectors).

There will be a very large number of tracks and a large number of primary vertices in each bunch crossing at the sLHC. To do pattern recognition and maintain good track-finding efficiency with low fake rate requires increasing the granularity of the inner trackers, ideally to the point where occupancies are much less than 1%, limited by cost and also the amount of material that has to be introduced.

Both experiments will add extra pixel layers at larger radii, replacing a region currently using silicon strip detectors. The pixel sizes will also be reduced; for example, the current ATLAS pixel size is 50 µm by 400 µm and will be reduced to 50 µm by 250 µm. This is possible by taking advantage of the availability of 130 nm read-out chip technology in place of the current 250 nm versions. It gives significant improvement in the z-vertexing, needed to separate the primary vertex from pile-up vertices.

In the regions just outside the pixels, either short-strip detectors (about 25 mm long in ATLAS case) or “strixels” – pixels ~ 2 mm long – will be used. At outer regions, long strips (about 100 mm long) will have low enough occupancy. The TRT straws of ATLAS will be removed and replaced with such long strips. The strip sensors about 400 mm from the beam need to cope with non-ionising doses up to 10¹⁵ n_{eq}/cm² (including a safety factor of 2). This requires very high bias voltage (600 V) for full depletion. Irradiated sensor prototypes for ATLAS have recently been shown to hold this.

Front end chips are under development for the strip detectors at both experiments. The goals here are high radiation hardness and single-event upset tolerance; and also low power, while still coping with the high data rate. Low power is important to save material bringing the power in and in cooling systems to remove it.

Powering remains a very important issue. There is no space for the present solution of one set of power cables per module; powering will have to be multiplexed, bringing in current at high voltage for low cable losses. Serial and DC-DC options are under study. System aspects – control, monitoring, and safety – are very important.

Data links also need developing, to find rad-hard optical communications at much higher rates (about 4 Gbit/s) than now (40 Mbit/s), and using multiplexing. High voltage and detector control systems also would benefit from more multiplexing.

2) Calorimeters

The barrel and most of the endcap calorimeters will perform well at the sLHC. Some re-optimisation of signal processing will be needed in view of the higher pile-up.

The electromagnetic calorimeter at CMS can suffer darkening of the crystals and vacuum photo triode light detectors; the effect depends strongly on pseudorapidity.

At ATLAS, the liquid argon (LAr) forward calorimeter FCAL will have increased heat-load, higher ionisation in the argon, and higher electrode currents; these could lead to boiling, signal deterioration, and voltage drop across the high-voltage resistors. The limits are being explored in a test-beam at Protvino. Two solutions are under investigation for use if necessary: to put a new, warm calorimeter in front of the current one; and to replace the FCAL altogether with a detector with more cooling and smaller gaps between electrodes. The latter requires careful development of tooling to be able to carry out the change in the time available, but engineering studies show it can be done. ATLAS considers reading out all data at 40 MHz from the detector, for both LAr and Tiles. High speed links to achieve this are being developed. Such a scheme can greatly simplify the front-end electronics and allow higher granularity giving increased flexibility in the trigger.

The detector sensitive elements and fibres of the hadronic tile calorimeters in both experiments will perform well at the sLHC. Light loss after 3000 fb⁻¹ will be significant, but the photon statistics are sufficient to maintain acceptable performance. The electronics however will probably need replacing - both power supplies and readout. The current versions are insufficiently radiation hard, and will be reaching their end-of-life, with spares hard to find.

3) Muon Systems

For both experiments most of the muon systems should perform well. CMS will install some new trigger chambers which were staged from the original design. At CMS, the iron for the magnetic return provides good shielding from background, and only some of the very forward cathode strip chambers will need replacing.

At ATLAS the air-core toroid has less shielding. The background rate estimates have large uncertainties. The chambers can handle five times the current background prediction at nominal LHC luminosity. If the backgrounds are as predicted, then at the sLHC only a small fraction will have to be replaced - the cathode strip chambers on the small wheels. But if backgrounds are five times higher than anticipated, far more chambers will need replacement, or solutions will have to be found that reduce the background. It is therefore very important for the backgrounds to be understood in early running at the LHC. Several radiation monitors are in place for this.

The current ATLAS muon chamber read-out architecture has some places with insufficient band-width for the sLHC. To minimise changes, a scheme where only chambers in regions with a level-1 muon trigger are read out is being developed.

New detector technologies under investigation include micromegas, drift-tubes with smaller diameter, and thin-gap chambers (TGC) for higher rates. Micromegas and TGCs can provide both trigger and precision measurement in one chamber. This can save space, allowing more shielding.
4) Triggers and Data Acquisition

Trigger processing power and network band-width will be expanded as it becomes cheaper and is needed. Additional ideas are under investigation. Increasing the level-1 trigger rate looks to be very difficult, but increasing the latency may be possible. This gives time to do more at level-1, reducing the burden on higher levels.

In addition, maintaining trigger rates will require raising thresholds. However at CMS the level-1 muon trigger rate becomes almost constant once the threshold rises above about 30 GeV. Higher trigger levels do give good reductions well above 30 GeV, by including inner tracker information. It is therefore interesting to develop track triggers at level-1. Read-out at 40 MHz is not possible. Instead several ideas are being investigated, including novel read-out chips looking at coincidences between pixels or strips at fixed azimuth in sensors separated radially by about 2 mm. Such coincidences can be communicated to the end of a stave, and further processing can look for pairs of such coincidences at the same azimuth but in different layers. This can give a sharp threshold to a high transverse-momentum trigger.

Other ideas are also under investigation, such as topological triggers - for example the combination of muon and calorimeter information to find isolated muons. ATLAS is investigating the use of a large associative memory to spy on the level-1 to level-2 data transfer, and provide level-2 early on with quality helix parameters for tracks.

5) Shielding

Clearly it would be good to improve shielding so that backgrounds do not rise in proportion to the luminosity. However, this is very difficult since both experiments already have highly optimised shielding. Some improvements are nevertheless possible. CMS can install borated polyethylene in their forward shielding, improving muon system backgrounds. The most important for ATLAS is to substitute the stainless steel beam-pipe sections which pass through the end-cap calorimeters and toroid magnets with beryllium. This reduces muon backgrounds a factor 2 or more. Also 50 mm of polythene moderator on the outside of the inner tracker volume will reduce neutrons in the tracker a factor 2. Other improvements could come if muon chambers can be made smaller, making more space for shielding.

V. Summary

A few years from now, there is likely to be a rich field of physics to study, that will benefit from a ten-fold luminosity increase. The sLHC will set demanding conditions for the detectors, requiring substantial upgrades. The timescale is challenging, particularly to install new inner trackers in 2017, needed even without the sLHC due to radiation damage of the present trackers. Several research and development projects are underway. Electronics developments are essential throughout the subdetectors, and are often on the critical path.

References


CO₂ cooling for HEP experiments

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Abstract

The new generation silicon detectors require more efficient cooling of the front-end electronics and the silicon sensors themselves. To minimize reverse annealing of the silicon sensors the cooling temperatures need to be reduced. Other important requirements of the new generation cooling systems are a reduced mass and a maintenance free operation of the hardware inside the detector.

Evaporative CO₂ cooling systems are ideal for this purpose as they need smaller tubes than conventional systems. The heat transfer capability of evaporative CO₂ is high.

CO₂ is used as cooling fluid for the LHCb-VELO and the AMS-Tracker cooling systems. A special method for the fluid circulation is developed at Nikhef to get a very stable temperature of both detectors without any active components like valves or heaters inside. This method is called 2-phase Accumulator Controlled Loop (2PACL) and is a good candidate technology for the design of the future cooling systems for the Atlas and CMS upgrades.

I. EVAPORATIVE CO₂ COOLING

In detector applications it is crucial to minimize the hardware needed for the cooling inside the detectors. It is known that two-phase cooling is more efficient than single phase cooling. Less flow is needed and a tube can become almost isothermal when the pressure drop remains low. The smallest diameter evaporator tubes can be achieved with fluids which are evaporating under high pressure. For these fluids, the created vapor can not expand to a large volume. Therefore the pipe volume hence the diameter can stay low. A smaller diameter pipe contains less fluid mass. A high pressure fluid needs a thicker tube wall, but since the pipe diameter is smaller, the increase in mass of the tube wall is compensated by the diameter decrease. Hence, the total mass (tube+fluid) is lower when using a high pressure fluid as compared to a low pressure fluid.

Another good feature of high pressure fluids is that larger pressure drops can be allowed. The influence of the pressure drop is related to the absolute pressure, and therefore less significant for high pressure fluids. This means that even smaller diameter tubes can be used.

Currently used radiation hard fluids are fluor-carbons and CO₂. Figure 1 shows the saturation pressure curves of some these fluids in the temperature range between +10 and -40°C. As can be seen, CO₂ is the best candidate of the three and C₃F₈ the least interesting candidate fluid. A calculation later in this paper will show the superiority of CO₂ compared to the two fluor-carbons.

A. Temperature distribution in an evaporative cooling tube.

The pressure along a cooling tube drops in the direction of the flow. This results for two-phase flow in a decrease in temperature due to the decrease of the saturation pressure. In contradictory for single phase flow the temperature increases along the tube due to the heat capacity. Figure 2 shows a typical temperature distribution over a cooling tube with CO₂ starting in single phase at the inlet and ending in gaseous phase at the outlet.

At the lower graph the temperature along a tube is shown, with the increasing temperature in the two single phase regions and a decreasing temperature profile in the two-phase...
region. The black line is the fluid temperature, while the red line is the tube wall temperature. The difference between them is caused by the heat transfer resistance. In the region where the evaporation starts, the heat transfer resistance and hence the temperature difference is low. At a certain vapor quality the heat transfer can get suddenly worse causing a rapidly increasing wall temperature. (Vapor quality is the mass fraction of vapour to liquid in a two-phase flow). The wall temperature increase is due to the fact that the remaining liquid is no longer touching the tube wall resulting in a poor heat transfer resistance. This phenomenon is called dry-out.

During a cooling cycle two main parameters change: energy is added or released in the form of enthalpy and pressure is lowered by expansion or increased by pumping or compression. Due to the change of these 2 properties the other important features like the temperature are derived. Setting a temperature directly is not possible; it is achieved by setting the right enthalpy and pressure to achieve the desired temperature. For this reason cooling systems are designed in the pressure-enthalpy diagram of the corresponding fluid. In the top panel of Figure 2 a CO₂ pressure enthalpy diagram shown. The temperature distribution over the tube and the fluid state in the lower panel can be read from this diagram.

B. Pressure drop and heat transfer

Two-phase pressure drop as well as two-phase heat transfer is hard to predict accurately as the liquid/vapor flow pattern are very non-uniform. The existing prediction methods are all based on empirical correlations of data fitting in certain operational areas. A lot of research is done on low-pressure fluids in macro tubes, while our applications use high pressure and mini channels. Only a few research results are available for each of these subjects and results on the combination of the two are even harder to find. The calculations in the example in this paper are based on research from several years ago. Although more recent and hence more accurate models have become available in the mean time, it does not influence the comparison of different cooling fluids.

Petterson et al [1] used the Friedel correlation for pressure drop and the Kandlikar correlation for heat transfer during their research of CO₂ in micro channel tubes for automotive air-conditioning in 2000. In both correlations the two-phase formula is the single phase formula multiplied by a correlation factor. An overview of all the relevant equations and parameters are given in chapter VII and VIII. The two-phase pressure drop can be calculated with equation 1:

$$\Delta P_{TP} = \phi_{LO}^2 \Delta P_{LO}$$ (1)

$\Delta P_{LO}$ is the pressure drop of single phase liquid with the same mass flux. For simplicity the Blasius equation (15,16) can be used. The two-phase pressure drop multiplier can be calculated according to the Friedel correlation:

$$\phi_{LO}^2 = \frac{E + 3.24 * F * H}{F_{Fr} 0.45 * W_{E_{Tp}} 0.035}$$ (2)

The two-phase heat transfer coefficient can be calculated according to the Kandlikar correlation.

$$\alpha_{TP} = \alpha_{LO}^*(C_1*CO_2^2*(25+F_{Fr})^5+C_3*B_0^4*F_{Fr})$$ (6)

$\alpha_{LO}$ is the heat transfer of the of single phase liquid with the same mass flux. For simplicity the Dittus-Boelter equation (7) can be used.

With the above mentioned formulas a possible cooling pipe solution for the upgrade of the Atlas staves (see next section for details) was analysed to give an estimate of achievable tube diameters. An indication of the temperature distribution over the tube for the estimated tube diameter is also given.

C. Example cooling tube of an Atlas upgrade stave.

To demonstrate the superior properties of CO₂ with respect to C₃F₈ and C₂F₆, the cooling of a possible Atlas upgrade stave is analysed for all three fluids. The stave is constructed of two layers of silicon, each layer existing of 20 wafers with a spacing of 10cm. Each wafer assembly dissipates 17 watt. The four meter long cooling tube runs along all wafers and has to absorb a total power of 680 Watt.

![Figure 3: Schematic example of an upgrade Atlas stave](image)

The estimated cooling fluid temperature for this calculation is -35°C and the outlet vapor quality is fixed at 75%. First the pressure drop as a function of the tube diameter is calculated using the pressure drop formula of equation 1. Figure 4 show the pressure drop dependency as a function of the diameter for the three fluids. Figure 5 shows the temperature drop along the tube as a function of diameter. This temperature drop is a result of the changing saturation pressure (temperature drop phenomena explained in figure 2).

![Figure 4: Pressure drop of CO₂, C₃F₈ and C₂F₆ as a function of tube diameter](image)
For a given diameter, the pressure drop of CO₂ is the lowest of the 3, this is due to the high latent heat of CO₂ (less flow=less pressure drop), the low viscosity and the low vapor speed. Table 1 shows the calculated mass flows for the three fluids at -35°C, 75% exit vapor quality, and 680 Watt. If we assume a maximum temperature gradient over the tube of 2°C we can extract the necessary tube diameters from figure 5. Table 1 shows the tube diameter selection and the corresponding mass flux.

Table 1: Required mass flows, fluxes and diameter

<table>
<thead>
<tr>
<th>Fluid</th>
<th>Mass flow (g/s)</th>
<th>Tube diameter (mm)</th>
<th>Mass flux (kg/m²s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CO₂</td>
<td>2.9</td>
<td>2.7</td>
<td>506</td>
</tr>
<tr>
<td>C₂F₆</td>
<td>9.6</td>
<td>4.3</td>
<td>186</td>
</tr>
<tr>
<td>C₇F₆</td>
<td>8.7</td>
<td>7.7</td>
<td>661</td>
</tr>
</tbody>
</table>

After selecting the necessary tube diameter the heat transfer to the tube can be calculated. For comparison the heat transfer is calculated over a length of 75mm and 25mm respectively. The heat transfer coefficient is calculated using the Kandlikar correlation as given in equation 3. The fluid dependent parameter F_d is set to 1 for all three fluids assuming stainless steel pipes, as suggested by Kandlikar [2].

Figure 6 shows the calculated heat transfer coefficients. Figure 7 shows the temperature distribution over the cooling tube and the tube wall for both heat exchange lengths. The presented calculation clearly shows the superior behaviour of CO₂ as evaporative cooling fluid for detector applications. A CO₂ evaporator needs the smallest diameter tube and has the best heat transfer coefficients of the three fluids.

D. Cooling cycle

After defining a proper two-phase flow in the evaporator tube it is important to select a method to get this two-phase condition in there. In general there are two methods to achieve this. One is a liquid pumped system with an external cold source; the second method is to use the evaporator tube directly in a refrigeration cycle. Both methods have been used at CERN for the LHC experiments. The Atlas inner detector uses a vapor compression system with C₃F₆ as refrigerant [3]. The LHCb-VELO Thermal Control System (VTCS) [4,5] uses a liquid pumped system using the two-phase Accumulator Controlled Loop (2PACL) method [6] with CO₂ as working fluid.

![Figure 5: Temperature drop of CO₂, C₂F₆ and C₇F₆ as a function of tube diameter](image)

![Figure 6: Heat transfer coefficients.](image)

![Figure 7: Cooling tube temperature distribution.](image)

![Figure 8: Two-phase cooling system principles used at CERN.](image)

The advantage of the Atlas system is that one can use warm transport lines; a pumped system has cold transfer lines and needs proper insulation. The insulation layer gives extra space requirements, however the tubes are smaller so the mass involved is most likely lower. The disadvantages of the Atlas system are the existence of heaters in the detector to boil-off the remaining liquid, an oil-free compressor is needed as well which is in general harder to find as an oil-free pump. The main advantage of the VTCS-2PACL method is a complete passive evaporator section inside the detector. Neither actuators, nor crucial sensors are needed in the inaccessible detector area.
II. THE 2PACL METHOD

So far two CO₂ cooling systems have been developed for particle physics applications. CO₂ was proposed as alternative cooling fluid for the LHCb-VELO in 1998 [7]. The positive results of the feasibility tests for the LHCb-VELO with CO₂ has inspired the design of Tracker Thermal Control System (TTCS) [8] of the Alpha Magnetic Spectrometer (AMS) for the International Space Station (ISS) [9] to use CO₂ as well. The AMS-TTCS is a mechanically pumped two-phase loop system where the CO₂ vapor is condensed to a cold radiator plate. The evaporator pressure is controlled by a two-phase accumulator which is the regular way of controlling the pressure in a capillary pumped loop. The capillary pumped loop is an evaporative heat transport system where the flow is achieved by capillary pumping. Capillary pumped loops are applied in satellite cooling [10]. The development of a two-phase accumulator in combination with a mechanical pump in the AMS-TTCS, has inspired the design of the LHCb-VELO cooling system. The use of a two-phase accumulator as loop pressure control was named 2PACL method, which stands for two-phase Accumulator Controlled Loop.

The 2PACL cycle is shown in figure 10. The accumulator vessel is mounted in parallel to the system and contains by design always a mixture of liquid and vapor. This guaranteed presence of a saturated mixture makes the loop pressure to be a function of the accumulator temperature. The 2PACL method works as long as the chillier is able to keep the CO₂ outlet of the condenser colder than the accumulator saturation temperature. In this way the pump is fed with sub-cooled liquid and can run free of cavitation. The internal heat exchanger is heating the sub-cooling, so that the evaporator is always evaporating at the saturation temperature set in the accumulator.

Between node 2 and 3 heat is applied via the internal heat exchanger to reduce sub-cooling. Liquid expansion takes place between node 3 and 4, ending up with saturated liquid at the evaporator inlet. The evaporator is taking up heat from node 4 to 5, where the vapor quality increases due to evaporation. The evaporator outlet (node 5) can still be partly liquid, not all the liquid need to be evaporated as the pump is providing an overflow.

The heat exchanged from node 5 to 6 is equal to the heat applied to node 2 to 3. In the fact of insufficient heat absorption in the evaporator or from the environment, node 6 can be sub-cooled. In this case there is still evaporation in the evaporator but only sub-cooled liquid is present in the condenser. Only at extreme unbalance between the sub-cooling temperature and the evaporator saturation temperature, there is sub-cooled liquid in the evaporator. The 2PACL is now out of its working range. The condenser is the section from node 6 to 1, with sub-cooled liquid supplied back to the pump again at node 1. Nodes 4, 5, 6 and 1 all have the same pressure as the accumulator, neglecting the small pressure drop in the system.

III. THE LHCb VELO DETECTOR

The LHCb-VELO [10] is the sub-detector closest to the collision point in LHCb. It consists of 21 double and 2 single silicon sensor layers which are positioned at about 1 cm distance from the LHC proton beams. The VELO is split into two halves both covering half of the active silicon sensor area. The silicon wafers are mounted on a module containing the read out electronics and mechanical support. The silicon modules are situated in a vacuum volume which is separated by a 0.3mm aluminium foil from the LHC beam vacuum volume. The maximum allowed pressure difference between the 2 vacuum volumes is 5 mbar, which is controlled by a complex system for pumping down and filling the vacuum volumes simultaneously [12]. The reason for a secondary vacuum is the out gassing of the silicon modules, and the possibility of installing detector hardware without exposing the LHC beam vacuum volume to the air. The 0.3 mm aluminium foil around the silicon modules acts also as a Faraday cage protecting the silicon and electronics from the electromagnetic interference of the proton beams.

Figure 9: The 2PACL principle

Figure 10: The 2PACL cycle in the Pressure-enthalpy diagram

Figure 11: The LHCb-VELO detector with a quarter of the silicon modules visible.
depletion voltage. Permanent cooling of the sensors is needed to avoid further degradation of the silicon sensors. A silicon temperature less than -7°C is sufficient to minimize the effects of radiation damage.

A. VELO module design.

The VELO modules consist of a carbon fiber TPG laminate where on both sides an electronics hybrid with a silicon sensor is glued. At the bottom of this laminate the CO$_2$ cooling evaporator is mounted on one side and the carbon fiber support paddle on the other side. The paddles are mounted on a stiff aluminium base frame. Figure 13 shows a picture of an assembled VELO half with the discussed items clearly visible. The Beetle read-out chips are located on the hybrid at the edge of the silicon and can generate up to 28 watts of heat per module which needs to be taken away by the CO$_2$ cooling system. The aluminium base is the positional reference of the modules and must stay at room temperature. This is achieved by heaters since the thermal connection via the paddles to the CO$_2$ evaporators will otherwise cause the base to cool down.

B. CO$_2$ evaporator design.

Each silicon module is connected to a dedicated parallel evaporator branch. Each branch consists of a 1 meter long stainless steel capillary of 1.5x0.25mm, which is embedded in an aluminium cooling block which is attached to the carbon fiber/TPG laminate. The aluminium cooling block is obtained with a casting procedure specially developed at Nikhef. The Aluminium is melted around the tube in a vacuum oven, so that the Al joins the stainless steel in a chemical way. The casting will give a lot of freedom in pipe geometry inside the aluminium and a perfect thermal contact between the pipe and the cooling block. Each evaporator branch has a 1.3 meter restriction capillary of 1x0.2 mm at the inlet to obtain a good flow distribution over all the evaporator branches. The presence of the evaporator in a vacuum system gives high constraints to the leak tightness. Therefore the complete evaporator assembly (figure 14) is made of stainless steel tubes all joined together with vacuum brazing or orbital welding. No connectors are present inside the vacuum system. The inlet manifold connected to the inlet capillaries is outside the vacuum vessel and is accessible. This way it is possible to connect cooling to individual channels, a feature which is used by module commissioning using a small scale test cooling system.

IV. THE VELO THERMAL CONTROL SYSTEM (VTCS).

The VTCS is a cascade of three hydraulic systems. A Freon chiller condenses the CO$_2$ vapor and rejects the waste heat to the cold water system of CERN. This chiller has a gas compressor, water condenser, evaporators and expansion valves. The water system is called the primary cooling system, the chiller the secondary and the CO$_2$ loop the tertiary cooling system. Figure 15 shows a schematic diagram of the cascade systems, with the main heat flows and the system temperature distribution.

The VTCS also has an air-cooled chiller with lower capacity. This back-up can only cool the CO$_2$ loops to -10°C and has no capacity left over to absorb detector power. It is only for maintaining the unpowered detector cold to avoid radiation damage in case of a problem or during maintenance.
The VELO detector

The evaporator inlet flow to be saturated.

The concentric construction acts return tube (16mm x 1mm). The liquid feed transfer tube (1/4”x0.035”) is situated inside the vapor system operation.

only for monitoring and are not important for the cooling Sensors (pressure and temperature) in the radiation zone are passive devices such as restrictors and one-way valves. Sensors (pressure and temperature) in the radiation zone are only for monitoring and are not important for the cooling system operation.

The CO₂ evaporators in the detector are connected to the VTCS via 55 meter long concentric transfer lines. The liquid feed transfer tube (1/4”x0.035”) is situated inside the vapor return tube (16mm x 1mm). The concentric construction acts as a long counter flow heat exchanger needed for conditioning the evaporator inlet flow to be saturated.

The cooling plant of the VTCS is placed 55 m away from the VELO detector behind a thick concrete shielding wall (See figure 16). This wall shields the system from the radiation of the LHC. The VTCS is designed such that all active hardware is located in this safe zone. The cooling hardware in the experimental area consists only of tubes and active hardware is located in this safe zone. The cooling radiation of the LHC. The VTCS is designed such that all (See figure 16). This wall shields the system from the waste heat of the experiment. The main control task in the CO₂ loops is to regulate the pressure by either evaporating liquid or by condensing vapor in the accumulator. Stabilisation is achieved by PID loops. For the freon chillers the most important tasks are the control of the expansion valves for the CO₂-freon heat exchangers and the frequency of the compressor.

Figure 16: VTCS set-up in the LHCb cavern

The flow in the evaporator must be of low vapor quality to achieve a stable liquid expansion in the flow distribution capillaries. The needed evaporator temperature to achieve the silicon temperature requirement is between -25°C and -30°C [13]. This temperature can be set in the system by controlling the accumulator pressure and hence saturation temperature. This temperature setting of the accumulator is called the VTCS set-point. For commissioning the set-point can be set higher, as the silicon sensors are not yet irradiated. Under vacuum the cooling temperature for commissioning is -5°C, for commissioning under Neon atmosphere the cooling temperature is +10°C. Operating the cooling at +10°C is achieved by using the back-up air-cooled chiller, as the water cooled chiller is too powerful for operation at higher temperatures than -5°C.

Figure 17: The VTCS cooling plant in the LHCb-cavern

The cooling system is controlled by a Siemens S7-400 series Programmable Logic Controller (PLC). It controls the two independent CO₂ loops and also the water cooled main chiller and air cooled backup chiller. Moreover, the PLC handles all the VTCS safety alarms and it interlocks to other subsystems of the VELO like low voltage, bias voltage and vacuum system. In total the cooling system contains about 20 pressure sensors, more than 150 temperature sensors and over 20 actuators such as pumps, valves, compressors and heaters. Note that only a fraction of these sensors are crucial for the operation of the cooling system. The other sensors allow us to study the behaviour of the system in great detail. This is important as the VTCS is the first CO₂ based cooling system in use at a HEP experiment. The main control task in the CO₂ loops is to regulate the pressure by either evaporating liquid or by condensing vapor in the accumulator. Stabilisation is achieved by PID loops.

Figure 15: Block diagram and heat balance representation of the VTCS

![Diagram of VTCS](image)

![Diagram of VTCS](image)
Figure 18: Unpowered detector cooling tests under vacuum in March 2008.

V. COMMISSIONING RESULTS OF THE VTCS.

The VTCS was installed in 2007 and commissioning was started early 2008. The full detector was not operational until May 2008. Prior to detector availability, dummy heaters were installed near the VELO to replace the detector heat load. The flow through the detector was by-passed, as it was not allowed to cool the detector below 10°C under Neon vented condition of the vacuum volumes. The VTCS was tested using the dummy heaters under several heat loads up to 800 Watt per loop.

In March 2008 the detector was for the first time cooled under vacuum conditions at several operational temperatures ranging from 0°C to -30°C (See figure 18). There was no power dissipated neither in the detector nor in the dummy heaters. The detector electronics were not yet cabled.

In May the detector was powered on module by module under Neon atmosphere with the back-up chiller at 10°C cooling only one detector half. After the successful detector powering tests, the detector was evacuated to vacuum at the end of June for upcoming LHC commissioning. Following the evacuation the full detector was commissioned with its designed cooling temperature of -25°C and all the electronics switched on.

The start-up of the left VTCS is shown in figure 19. Around 13.4 clock time the accumulator started heating (7,red) to increase the pressure (7,gold) to 27°C saturation temperature. As the loop saturation temperature is higher than the environment temperature, the loop is filled with liquid and consequently the accumulator liquid level is dropping (7,blue). Around 13.6 hour the pump was started as can be seen by the increase of the pump head pressure (2). The chiller is started right after this cooling down the liquid flow to the pump (1). After pumping cold liquid for a while, the accumulator is cooled to bring the pressure down to the desired set-point pressure and hence temperature. The accumulator cooling is the negative signal from the combined heating/cooling control (7, red). Due to the accumulator cooling, the accumulator is filling as can be seen by the increasing liquid level (7,blue). Around 14.7 hour the set-point has been reached and the temperatures and pressures stay constant. The accumulator remains to be cooled to compensate the environmental heat leak from the environment. The VTCS is now ready for detector power.

Figure 19: Start-up of the left-VTCS 2PACL.

Figure 20 shows the powering-up of the left detector with the cooling set-point to be -25°C. Around 15 minutes the detector is switched on. The purple line is the individual heat load of one module, the blue line the total heat load of the left detector. As a result the module temperature (black line) and the silicon temperature (green line) are increasing. The silicon is stabilizing around -7°C, this is according to the design requirements. The applied heat in the evaporator increases the...
amount of vapour in the system which causes the pressure and hence the evaporator temperature to rise a bit. The accumulator control is reacting to this pressure offset by cooling the accumulator (cyan line). As a result is the liquid level (red line) increases because the generated amount of vapor is accumulated in the accumulator. After a small deviation the evaporator temperature is maintained.

VI. CONCLUSIONS AND OUTLOOK.

This paper has demonstrated that CO₂ as evaporative coolant is very promising. It has multiple advantages for detector applications as CO₂ seems to add less mass to the detector compared to evaporative cooling with fluor-carbons. The possibility of using smaller tubing is not only beneficial for the mass budget, but gives also more flexibility in the design as the pipes are more flexible. Flexible tubing gives less structural impact on the detector mechanics, such as thermal expansion.

The 2PACL method was presented in this paper. The VTCS was built according to this principle and the VTCS works as expected. The requirements are met, as the silicon was operating at -7°C at the designed cooling temperature of -25°C. The evaporator temperature turned out to be very stable; fluctuations of less than 0.05 °C were measured over time. The VTCS set-point range was determined to be between -5°C and -30°C.

The construction of the VTCS is not yet finished. The VTCS commissioning has learned us that an accumulator connection at the inlet of the condenser is working better than the location after the condenser were it is now. The accumulator heating was sometimes giving saturated liquid to the pump, causing the pump to cavitate. The accumulator connection swap will solve this problem. One 2PACL side (right system) was temporarily modified, and results were promising. It was decided to implement this modification on both 2PACLS. These modifications will be done early 2009. Other ongoing works are the implementation of the automatic back-up procedures, the chiller expansion valve tuning and the integration of the system in the PVSS-finite state machine.

VII. NOMENCLATURE

ΔP = Pressure drop (Bar)
φ = two-phase pressure drop multiplier
E, F, H = Friedel correlation constants
α = Heat transfer coefficient (W/m²K)
Fr = Froude number
We = Weber number
Re = Reynolds number
Pr = Prandtl number
Co = Convection number
Bo = Boiling number
Nu = Nusselt number
h = Enthalpy (J/kg)
λ = Thermal conductivity (W/mK)
ρ = Density (kg/m³)
η = Dynamic viscosity (Pa*s)
σ = Surface tension (N/m)
Cp = Heat capacity (J/kg*K)
x = Vapor quality
g = Specific gravity (m³/kg)
f = Friction factor
m' = Mass flux (kg/m²s)
q' = Heat flux (W/m²)
D = Hydraulic diameter (m)
C₁ = Kandlikar´s nucleate boiling constant: 0.6683
C₂ = Kandlikar´s nucleate boiling constant: -0.2
C₃ = Kandlikar´s nucleate boiling constant: 1058
C₄ = Kandlikar´s constant: 0.7
C₅ = Kandlikar´s constant: 0 (Fr₅<0.04), 0.3 (Fr₅<0.04).
F₄ = Fluid surface parameter: 1 for stainless steel tubes

Indices:
TP = Two Phase
LO = Liquid only
L = Liquid
G = Vapor
VIII. EQUATIONS:

1. \[ \Delta P_{TP} = \Phi_{LO}^{2} \cdot \Delta P_{LO} \]

2. \[ \Phi_{LO}^{2} = \frac{E + 3.24 \cdot F \cdot H}{F_{LO} - 0.045 \cdot \Phi_{LO}^{2} - 0.035} \]

3. \[ E = (1-x)^{2} + x^{2} \left( \frac{\Phi_{L}}{\Phi_{G}} \right) \]

4. \[ F = 0.78 \cdot (1-x) \cdot 0.24 \]

5. \[ H = \left( \frac{\Phi_{L}}{\Phi_{G}} \right)^{0.91} \left( \frac{\Phi_{G}}{\Phi_{L}} \right)^{0.19} \left( \frac{\Phi_{G}}{\Phi_{L}} \right)^{0.7} \]

6. \[ \alpha_{TP} = \alpha_{LO} \cdot (C_{G} \cdot C_{G} \cdot C_{G}^{2} + (25 \cdot F_{LO} / C_{L}) \cdot C_{G} + C_{G} \cdot C_{G} + C_{G}) \]

7. \[ \alpha_{L} = \frac{\alpha_{LO}^{2}}{D} \]

8. \[ F = \frac{m}{g \cdot D \cdot \rho^{2}} \]

9. \[ \alpha_{TP} = \frac{m \cdot D}{\rho \cdot P} \]

10. \[ \alpha_{L} = \frac{m \cdot D}{\eta} \]

11. \[ \alpha_{TP} = \frac{\eta_{G}^{2} \cdot C_{G}}{\eta_{L}} \]

12. \[ \alpha_{L} = \frac{\alpha_{LO}^{2} \cdot \Phi_{L}}{D \cdot \Phi_{L}} \]

13. \[ \alpha_{TP} = \frac{m^{2} \cdot \Phi_{L}}{D \cdot \Phi_{L}} \]

14. \[ \alpha_{L} = \frac{m^{2} \cdot \Phi_{L}}{D \cdot \Phi_{L}} \]

15. \[ \alpha_{TP} = \frac{m^{2} \cdot \Phi_{L}}{D \cdot \Phi_{L}} \]

16. \[ \alpha_{L} = \frac{\alpha_{LO}^{2} \cdot \Phi_{L}}{D \cdot \Phi_{L}} \]

IX. REFERENCES


THURSDAY 18 SEPTEMBER 2008

TOPICAL 1

LHC UPGRDES
Abstract

The ATLAS Pixel Detector is an 80 million channels silicon tracking system designed to detect charged tracks and secondary vertices with high precision. An upgrade of the ATLAS Pixel detector is presently being considered. The Large Hadron Collider (LHC) will be upgraded to provide a ten fold increased luminosity leading to increased radiation doses and significantly higher occupancy in the region of the ATLAS Inner Detector and especially in the Pixel Detector.

The extreme radiation levels at planed Super Large Hadron Collider (SLHC) lead to a number of specific design challenges for read-out integrated circuits, silicon sensors and optical signal transmission. Options considered for a new detector are discussed, as well as some important R&D activities, such as investigations towards novel detector geometries and novel processes.

I. INTRODUCTION

The ATLAS detector is one of the largest and one of the most complex detectors at LHC. It is general purpose detector for the study of p-p interaction. In the heart of ATLAS, inside the solenoid magnet is the Inner detector. The Inner detector consists of Transition Radiation Tracker, Silicon Central Tracker and in the innermost region the Pixel Detector.

The Pixel detector provides critical tracking information for pattern recognition near the interaction point and very significantly contributes to overall capability of the Inner detector to find and reconstruct secondary vertices. In addition it provides very good spatial resolution for reconstruction of primary vertices coming from p-p collision point. The design of the Pixel detector is done in a way to get at least three space points on a charged track coming from the interaction point of ATLAS. There are three barrel layers approximately at radii of 5, 9 and 12cm with respect to the interaction point and six disks, three at each side of the detector. The actual layout of the Inner detector is illustrated in Fig.1.

The pixel detector is built with 1744 modules identical for both barrel and disk parts. The module consists of silicon sensor containing 2880 planar diodes of 50x400μm connected to sixteen Front - End (FE) chips. The electrical connection of the sensor and FE chips is done via bump-bonding interconnection technology using solder or indium bumps of about 12μm in diameter. The total number of channels is about 80 million and the total active silicon area is about 1,7m² [1].

II. THE LHC MACHINE UPGRADE

The LHC at CERN is recently ready to start operation and first data coming from proton-proton collision are expected soon. The exact upgrade scenario of LHC to SLHC is not yet defined in details but most likely it will occur in a number of phases.

An relatively modest increase above nominal luminosity \(10^{34} \text{cm}^{-2}\text{s}^{-1}\) is expected in the first 4-5 years of LHC running and should be achieved through higher beam currents. This first upgrade phase would also involve major hardware upgrade, in particular the installation of new inner triplet focussing magnets allowing larger aperture. The changes just mentioned should allow a ramp-up close to 3 times nominal luminosity. The integrated luminosity that time should reach about 700fb⁻¹ and about 70 events are expected per collision.

The second phase of upgrading to SLHC will require rather larger time counting in order of months. Several ideas are recently investigated to reach the target value \(10^{35} \text{cm}^{-2}\text{s}^{-1}\) in 2017. The hardware changes will certainly include major improvement of injector and likely other new machine elements will have to be installed. More details can be found in [2].

The running at such high luminosity as \(10^{35} \text{cm}^{-2}\text{s}^{-1}\) will bring up pile-up of about 400 p-p interaction per collision and the annual integrated luminosity will be around 300fb⁻¹. In total, the integrated luminosity delivered in course of LHC and SLHC running should reach a value about 3000fb⁻¹.
The scenario recently considered and here described is shown in Fig 2.

III. SLHC GOALS AND PHYSICS MOTIVATION

In general, the SLHC luminosity upgrade to $10^{35} \text{cm}^{-2}\text{s}^{-1}$ allows extension of the LHC discovery mass/scale range by 25–30% and improves the sensitivity for precision measurements, for example, the couplings between the electro-weak bosons or of the couplings of the Higgs boson to various other particles. Operation of LHC will certainly provide a deep view of the physics at energy of TeV scale. Nevertheless, the physics program at LHC still does not guarantee whole understanding of all fundamental questions in particle physics. It is rather difficult to predict these days, at the beginning of LHC operation what would be the best next machine after LHC. Obviously it will become clearer when the first LHC data will be available. The upgrade to luminosity of $10^{35} \text{cm}^{-2}\text{s}^{-1}$ seems to be reasonable compromise between the cost and physics achievements. SLHC is natural extension of the LHC program for further decade of years requiring rather modest investment compared to the LHC overall cost in an efficient way. It maximally exploits the existing tunnel, the machine and also the experiments.

However, to fully exploit a factor 10 increase in the luminosity, the tracking performance of ATLAS during SLHC operation must be maintained at a level comparable to its performance during LHC operation.

IV. IMPACT TO TRACKER DETECTORS AND RADIATION LEVELS

It is evident that upgrading to SLHC will pose a significant challenge to experiments especially to ATLAS and CMS. The entire tracking system of both main LHC experiments has to be completely replaced and major upgrades are also being considered for the forward calorimeters, trigger system and beam-pipe. The start-up of LHC operation will help with focusing the main effort to right direction. In light of these upgrade issues a number of R&D’s have already started in order to be ready to take SLHC data in the second half of next decade. For the detector upgrades, the overall design, production and installation schedule is already very aggressive goal based on the LHC experience.

The expected high radiation levels as well as the large increase in the occupancy impose very strict requirements to inner tracking systems of ATLAS and CMS experiments. In order to cope with the increased occupancy, the LHC trackers will have to be replaced by ones with higher granularity. In reality it means about a factor of 2-3 more channels. The increased channel number imposes stringent constraints also for the power consumptions as well for the material budget. Therefore new powering schemes for trackers are considered. In addition, very radiation-hard techniques will be needed in the hottest region within 20cm apart from the beam pipe. Such environment is demanding fundamental R&D for new detector materials and concepts. At larger radii, evolutions of the present pixel and strip technologies should be still adequate.

Fig. 3 shows simulated radiation level inside the Inner detector region of ATLAS. The innermost part where the Pixel detector is installed will be exposed up to a fluence close to $10^{16} \text{n}_{eq}/\text{cm}^2$ and to radiation dose of 5MGy in FE electronics corresponding to the total integrated luminosity of 3000fb$^{-1}$ delivered by LHC/SLHC. The simulation of radiation levels is shown in Fig.3.

V. PIXEL DETECTOR B-LAYER REPLACEMENT

With expected luminosity increase we assume the performance of the innermost pixel B-layer will start to
degrade due to radiation damage after 3-4 years of LHC operation. This will happen when LHC integrated luminosity will reach about 300fb⁻¹ corresponding to a fluence of about 10^{19}\text{ n}_{eq}/\text{cm}² in this innermost Pixel detector region where the B-layer is installed. As the after effects of such very harsh radiation environment influence one can expect to observe reduced efficiency and worsening of point resolution of the B-layer. Also, the present B-layer is not designed for luminosities above 2 x 10^{13}\text{ cm}²/\text{s}. Due to granularity issue, the read-out chain does not allow to read all hit pixels and the deteriorating of efficiency would be starting.

The performance of the B-layer has significant impact on Atlas physics especially on B-tagging. Therefore it is suggested to replace the recent B-layer with new one or even to insert the new B-layer built with reduced diameter whilst keeping the old one inside the detector.

The second option, the insertion of the new B-layer it will happen most likely considering access issues at ATLAS after few years of LHC operation and rather short shutdown periods allowing access to the detector cavern.

VI. DEVELOPMENT OF SENSORS FOR SLHC

As already mentioned, the ATLAS Pixel detector will have to operate in very harsh radiation environment resulting fluence up to 10^{19}\text{ n}_{eq}/\text{cm}². The current Pixel detector sensors are based on planar n-in-n technology (n-type bulk) and are proved to be sufficiently radiation hard up to a fluence order of magnitude lower, it means around 10^{15}\text{ n}_{eq}/\text{cm}². Recently there are several R&D’s running in parallel searching for new sensor design concepts and technologies. Obviously overall production cost of new sensors will play dominant role especially at larger radii where the detector area is not negligible.

Recently used n-in-n sensors are not radiation resistant enough to be seriously considered for the innermost Pixel detector layers at SLHC. Choosing p-bulk material seems to bring several advantages. Firstly, it requires only single side wafer processing what would lead to higher production yield and consequently to significantly reduced production cost when compared to double sided n-in-n technology. Also, the p-bulk material does not invert and the pixel connection is always at junction side. P-bulk sensors show less charge trapping when highly irradiated.

Developments of both, n-in-n and n-in-p planar sensors are aimed to rise breakdown voltage values allowing increase of maximal applicable bias voltage, probably to values close to 1000\text{V} whilst reducing the inactive area at detector edges. Obviously the cutting quality has significant influence to detector properties and therefore new “safer” methods and technologies are also searched.

The “thin sensors”, ~75-150\text{µm} thick silicon planar sensors benefiting much lower voltage needed to reach full depletion state, shorter collection time, reduced reverse current and shot noise contribution. There is not significant difference when comparing amount of collected charge after fluence 10^{16}\text{ n}_{eq}/\text{cm}² at “thin” sensors with standard ~280\text{µm} sensors. However, such sensors are yielding lower signal since the beginning of operation and are demanding low threshold operation of FE electronics (Th < 4000e⁻). “Thin” sensors use usually connected to thinned FE electronics vertically using very challenging Inter Chip Vias (ICV) or Through Silicon Vias (TSV) interconnection method both offering an alternative to the bump-bonding process.

The 3D sensors, sensors where tiny highly doped p+ and n+ electrodes are processed inside the detector bulk instead of being implanted on the wafer’s surface, have progressed pretty well since time when firstly introduced. The technology developed and adopted originally at Stanford Nanofabrication Facility is being successfully transferred to the industry. Several companies (e.g. SINTEF Norway, IRST Italy, CNM Spain) already adopted key technological operations including critical steps as deep reactive ion etching or poly-silicon filling into tiny electrode holes of few microns in diameter. The 3D detectors perform quite well even after high irradiation dose (Fig.4).

VII. DEMANDS ON FRONT-END ELECTRONICS

The increase of the luminosity by order of magnitude brings significant challenge to electronics of trackers. Firstly, the detectors need a sufficiently fine granularity and high resolution to resolve hit ambiguities when performing the pattern recognition. The pile-up of about 400 events per beam crossing at SLHC is expected yielding about 30 tracks per cm² per bunch crossing. It requires to reduce the pixel size from current 50 x 400\text{µm} to 50 x 250\text{µm} or even further to 50 x 200\text{µm}. The pixel pitch of 50\text{µm} will be most likely kept to allow “safe” and relatively less costly bump-bonding processing and to provide more freedom for selection of final sensor design (inter-pixel insulation, 3D implementation, etc).

The IBM 0.25\text{µm} process used for the recent FE electronics is becoming obsolete and newer IBM 0.13\text{µm} CMOS8RF process featuring with enhancements for analog design seems to be the most appropriate technology for B-layer replacement or even for SLHC FE electronics. The use of 0.13\text{µm} CMOS process should allow further scaling of design. The digital part should scale by at least 4 in going from 0.25\text{µm} to 0.13\text{µm}, due to presence of greater interconnection ability as well as device scaling. However, newer CMOS technologies can usually reduce only the size of digital circuitry, but the size and power required for the transistors in the analog
circuitry are set by the required noise and threshold matching. Newer submicron CMOS technologies would not reduce the power required for the desired noise levels, but would improve digital power efficiency.

The 0.13μm CMOS process is naturally more radiation resistant due to further reduction of thin oxide. Present pixel FE-I3 chips (0.25μm process) suffer from Vt shift at large doses affecting threshold dispersion and time over threshold (TOT) measurements. However, it does not look to be a serious issue for 0.13μm process. The 0.13μm process should allow simplification of rather complex in cell built tuning circuitry and also dropping guard rings around NMOS devices. The radiation dose seems to be mainly serious sensor issue resulting decrease of charge collection efficiency. Therefore the analog pixel electronics must cope with lower charge of irradiated sensors (8-10ke or even less), with relatively high sensor capacitance and high input current.

The goal for development of new FE electronics is to reduce inactive area (the area not covered by sensitive part of the sensor) as much as possible and also significantly enlarge the size of the FE chip. Recently used FE-I3 chips have size of 7,6 x 10,8mm (74% active area), proposed new FE-I4 pixel chip should have the size of 20,2 x 18,8mm (89% active area). Larger FE chips will reduce the assembly cost (flip chip process) and also the cost of sensors due to smaller module size considering 2x2 chips on the module or even only single chip modules for inner Pixel detector layers.

The digital readout architecture of recent FE-I3 chips is not appropriate for high SLHC luminosity and the hit inefficiency would rise steeply with high hit rate. The bottleneck is mainly data transfer through column pair bus clocked at 20MHz (shift register). All hits are transferred to the end of column buffer (64 deep) where waiting trigger, but only ~1% hits are actually triggered. The idea for new readout architecture is based on buffers placed locally close to a group of pixels and the transfer of information to the periphery would happen only when getting really triggered (Fig 5).

Figure 5: New FE Read-Out architecture [5]

VIII. PIXEL DETECTOR MODULE AND STAVE CONCEPT

General trend is to have the pixel module quite simple what would lead to higher production yield reducing overall cost. Recently is proposed to have modules with 4 FE chips for outer layers and perhaps only single chip modules for inner layers. Proposed size of the outer layer module is about 36 x 42,5mm accommodating 2x2 FE chips. The module controller chip is not considered anymore and will be substituted by stave controller chip, probably with simplified functionality placed at the “end of stave card”.

There are many challenging discussions and proposals concerning Pixel detector layout a local support structures. Local supports provide the mechanical support and integrated cooling for pixel modules. The aim is to reduce material budget and simplify production. The low density, thermally conductive foam with very thin carbon fibre facings appear to be very convenient material for either single layer stave support or monolithic structures [7]. The highlights of the foam material are low mass, low distortion from cool-down, easy machining, good mechanical and thermal conductivity properties and low radiation length. Such features give very promising presumption to consider this material as good candidate for future support structures of Pixel layers.

IX. POWERING ISSUES

The number of electronic channels will be dramatically increased for SLHC trackers. The total silicon area of upgraded Pixel detector will be approximately tripled. A constraint is that existing cable plant in the tracker most likely will not be replaced. The design of new tracker electronics must consider the use of existing cabling to power also additionally channels.

Presently used power scheme with separated power lines on level of the module can not be considered anymore. Such approach providing independent powering for each module is luxury way how to operate modules however, considering the cable material budget it is unacceptable furthermore. Also, the goal is to minimize the current flowing through the supply lines and to reduce cable power losses. Therefore options as DC-DC convertors with 2-3 times the target voltage placed close to the module or serial powering scheme with shunt or
linear regulators allowing supplying several FE electronic in series through one single power line are recently investigated.

X. SUMMARY

There are three main issues to be taken into account when upgrading LHC tracking detectors: detector performance, detector lifetime and the overall cost. The lifetime of resent silicon sensors for SLHC seems to be really serious issue and there is not available appropriate sensor working at high fluence as $10^{16} \text{ n}_{eq}/\text{cm}^2$ without significant degradation of initial parameters. However, there are recently many R&D’s focused on new technologies like 3D sensors, thin sensors or CVD diamond sensors. The planar sensors, as proved and relatively not expensive technology seem to be appropriate solution only for outer layers of the Pixel detector. The design of FE electronics partly depends on available technologies at given time. Obviously, the pixel size has to be further reduced the column readout architecture changed and the bandwidth of output links increased allowing higher data output rate. The timescale, either for B-layer replacement or full Pixel detector upgrade at SLHC is relatively short, so understanding of details, very good coordination and right decisions on time is substantial for successful development and installation at the ATLAS experiment.

XI. ACKNOWLEDGEMENTS

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Design Studies of a Low Power Serial Data Link for a possible Upgrade of the CMS Pixel Detector

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Abstract
The material budget inside the sensitive tracking volume is highly dependent on the dissipated power for data transmission. It is therefore important to have a very low power serial data link, which allows transmission of digital data over short distances within the tracking volume. This low power ohmic data transmission through micro-twisted transmission lines aims for a transmission speed of 160/320 MHz and allows concentration of the tracker data to multi gigabit optical data hubs. For such a future link we need low swing differential drivers and receivers with PLLs for frequency multipliers and clock recovery. We have implemented in radiation hard layout all the necessary components on a recently submitted 250nm CMOS test chip. After reporting on the experience gained with low power data transmission in the current CMS pixel detector, we present the design considerations and first results for this new 160/320 MHz serial link that may work with differential signal levels as low as 10mV.

I. INTRODUCTION

The communication from the detector modules to outside the tracking volume needs special data link configurations. It is not possible to take a few (optical) high speed data links because the information should be collected from many different similar detector components at different locations. For the case of the CMS pixel detector, the distances of 1 to 2 meters are relatively short. We need many data links of some 100 MBit/s. Due to the material budget and power constraints, it is not reasonable to do this with optical links. Copper wires are preferred. For the cabling, we have to optimize the following properties:

- To minimize the material budget, we take thin twisted pair wires without a shield.
- To minimize the power consumption we should have a low voltage swing. This needs differential signals.
- To minimize the wiring effort we need a serial data link at a multiple of the 40 MHz clock frequency. We need 160 or better 320 Mbit/s if it is possible.

We need to know what works if we go to thin wires, low signals, and higher speed at the same time. A possible approach will be shown for an upgrade for the CMS pixel detector.

II. THE CMS PIXEL DETECTOR

A. Signal Cabling

The CMS pixel detector consists of 768 modules on a support structure where the cooling pipes are also integrated. All the power and signal cables from the modules are routed to flanges at the two ends of the detector structure (Figure 1). There, the cables are connected to 64 PCBs. The signal cables are flat band cable with 21 traces.

![Figure 1: Signal and power connections from the modules.](image1)

From each of these PCBs, we have two wide flat band cables to the supply tube as shown in Figure 2. From there we have optical links. There are a total of 1664 connectors for power and signals on both flanges.

![Figure 2: Cabling at one of the ending PCBs. The module cable comes from the bottom left and is connected to a PCB on each side of the flange.](image2)
B. A possible new Concept

Figure 3 shows a schematic view of the signal path. From the supply tube we have clock, trigger, and control data. The signals are sent over a flat band cable to one of the 64 endring PCB’s. From there, we go to one of the 768 modules. From the module, we have control and detector data which are sent through separate lines over the same path.

As shown in Figure 4, for the new concept we would completely remove the PCB’s on the endflange with all the connectors. We would replace the flat band cables with one or two micro twisted pair cables which go directly from the module to the supply tube. At each endpoint is a controller for the serial protocol and the cable drivers and receivers. This logic can be integrated in existing chips.

The data format for the existing link is a 7 level signal and analog level for the pulse height information. The new link is fully digital. No analog pulse height signals can be transmitted. For this reason we have to add an ADC to digitize the pulse height signals.

III. MICRO TWISTED PAIR CABLE

A. Choice of a Cable

A first choice for a cable we have tested is a micro twisted pair cable. It consists of two copper clad aluminium (CCA) selfbonding wires as shown in Figure 5 from Elektrisola (http://www.elektrisola.ch).

This seems to be a good compromise between electrical resistance and breaking strength. Such a wire is easier to handle because you can bend it in each direction compared with the flat band cable that you can only bend in one direction.

One or two of these cables are bundled together with the power cables to build a module cable.

B. Electrical Characteristics

We have calculated the impedance with the software ATLC [1]. The resulting differential impedance is 48±2 Ù/m. The impedance decreases with increasing wire distance with 2.3 Ù/m per µm. We have verified the impedance calculation by a measurement with the cable. The measurement signal velocity is 2/3 c. The impedance is very low because of the thin isolation and the consequential small distance between the wires. The return path consists of the power and ground wires. Because the geometry of this wire is not defined, the common mode impedance is not well defined. The calculated capacitance is C=100pF/m and L=250nH/m.

Thin wires also mean that we have a high series resistance and resultant loss. The DC-resistance of this cable is R_DC = 2.3 Ù/m. We have also taken into account the skin effect. The skin depth is [2]

\[
\delta = \frac{2}{\sqrt{\alpha \cdot \sigma}}
\]

where \( \omega \) is the frequency and \( \sigma \) is the conductivity. For our wire, \( \delta = 8.5 \mu m \) @ 100 MHz. The resistance due to the skin effect is

\[
R_{AC}(\omega) = \frac{1}{2 \pi d \delta}
\]

where \( d \) is the wire diameter. This is an approximation for \( \delta \ll d/2 \). A good approximation [2] for the total frequency dependent resistance is

\[
R(\omega) = R_{DC}^2 + R_{AC}(\omega)^2
\]

We get 8.8 Ù/m @ 100 MHz for this. Possibly the resistance can be increased by the proximity effect.

From the telegrapher equation we get the complex line impedance of a lossy line

\[
Z(\omega) = \sqrt{j \omega L + R(\omega)}
\]

and the propagation coefficient

\[
\lambda(\omega) = \sqrt{j \omega C \left( j \omega L + R(\omega) \right)}
\]

Here, L is the inductance per meter and C the capacitance per meter. The real part of \( \lambda \) is the damping factor in Neper. From our calculations and measurements we get a power loss of about 50% for a wire of 2 m length.

IV. ELECTRICAL TRANSMITTER AND RECEIVER

A. Transmitter/Receiver

Figure 6 shows a unidirectional data link consisting of a transmitter, a receiver and the twisted pair cable. Typically at the receiver end is a differential termination of 24 Ù to ground at each end of the differential pairs. This type of data link is used in the existing CMS pixel detector to send clock, trigger and control signals to the module.
The transmitter is a current driver. The current \(I_{DC}\) from the constant current source is switched to one of the outputs \(V^{+}\) or \(V^{-}\). In this way the common mode current has the constant value of \(I_{DC}\). This is important because there is no well defined common mode impedance. The DC path between transmitter and receiver is closed by the power/ground lines. To test at different signal levels, the current \(I_{DC}\) is adjustable in the first test version.

The differential receiver has high impedance inputs. For the measurements, the termination resistors are not implemented on the chip and must be placed outside on the test board.

**B. Bidirectional Transmission**

We combine two driver and receiver pairs into a transceiver as shown in Figure 7. Here, we get a bidirectional link (half-duplex) with one physical line. At any time one driver is in a so called high impedance state. In order to let the common mode current stay constant, the current in this state is \(I_{DC}/2\) on each output so that the sum is exactly \(I_{DC}\). Typically, this link has a termination on both sides. The data direction is given by the protocol.

**V. Test Setup**

**A. ASIC Design**

To make the following measurements, I have designed a test chip as a member of the newly founded Chip Design Core Team at PSI with a size of 2 by 2 mm with the following test structures:

- Driver, receiver and transceiver as described above. The \(I_{DC}\) of the driver/transceiver is adjustable from 0 to 2 mA (LINK).
- A four bit serializer and deserializer shift register connected to the transmitter, receiver, and transceiver.
- Two types of voltage controlled oscillators (VCO), and two types of frequency phase detectors (FPD). With these blocks we can build a PLL for the clock multiplier from 40 MHz to 160 or 320 MHz which also can be used for clock recovery.
- A 4 bit SAR ADC to digitize the analog data signals. For the real data we need 8 bits but this block is for a low priority design study.
- A switched capacitor voltage divider for the analog voltage power supply. This block is not discussed here.

The Chip, whose layout is shown in Figure 8, is fabricated in a 0.25 \(\mu\)m technology from IBM the same as the CMS readout chip.

**B. Test System**

To make the measurements, we have built a test system consisting of a chip adapter and a test board (see Figure 9). The main component of this board is a Cyclone II FPGA from Altera. To control the board by a PC, there is a NIOS II soft core CPU in the FPGA and an USB adapter.

![Figure 8: Layout of the 2 by 2 mm chip with the different Components. It consists of four different test structures. The most space is used for the pads.](image1)

![Figure 9: Test system consisting of the Test board (left) and the chip adapter (middle). On the right side are bundles of cables which can be connected to different drivers or receivers](image2)
VI. DATA LINK TESTS

A. Lossy Line Effects

Figure 10 shows a signal at the end of a 2 m data link at 160 Mbit/s. A typical effect of line loss is seen at the signal edges. This consists of a fast and a slow component. For low frequency, we see an RC-line and for high frequency, it is an LC-line. This can also be shown with a spice simulation with a simple lossy line model.

The single ended signals at V+ and V- on the top of Figure 10 show common mode noise. Most of this comes from digital signal noise from the testboard, but it is highly suppressed in the differential signal.

B. Bit Error Rate Measurements

To find a lower limit for the signal amplitude we made a bit error rate test (BERT) for a unidirectional link (Figure 11). At 80 Mbit/s, the bit error rate was below $10^{-11}$. Because of a design error in the receiver output, it is not able to go below 30 mV at 160 Mbit/s. At this rate we get the same limit in the bit error rate.

C. Crosstalk Measurements

Another important measurement is the crosstalk between parallel lines. The problem is that we have no shield and want to bundle the cable. For the measurement we repeated a BERT but sent a differential signal with a six times higher amplitude as an aggressor to a parallel line over a length of 2 m. We could not see any difference in BER with and without the disturbing signal as shown in Figure 12. A reason for that can be the high capacitance of the cable. Field simulations have shown that the energy flows mainly in the small gap of the wire pair.

D. Bidirectional Link

Important for the bidirectional link is the dead time after switching the direction, especially if we plan to work with small packets. For this test I have sent a data packet (Figure 13) and then switched the transmitter into a high impedance state.

The signal on the line is stable before two signal line delays. This is the earliest time when the data arrives from the transmitter on the other side.
E. Power Budget

If we assume that we can run with a signal level of $V_{\text{diff}} = 20 \text{ mV}$ then we need a total driver current of 0.4 mA. The receiver has a current consumption of 0.2 mA. If we assume a supply voltage of 2 V we get a total power of a link of 1.2 mW. The energy per bit at 160 Mbit/s is then 7.5 pJ/bit.

The power for the data transfer to and from a module in the existing CMS pixel detector is approximately 30 mW at 2V. With the new concept we were able to replace the old link with a bidirectional link for one or two lines with a total power of 2.4 mW. In this calculation the power consumption of the PLL is not included.

VII. Data Protocol

A. Overview of a possible System

On the test chip, all front end components to build a complete communication link are available except the protocol implementation. We are able to implement this in the FPGA on the testboard. It is a full digital design that we can later transfer to an ASIC. Figure 14 shows such a system. The left side is the master on the supply tube at the interface to the optical links. The two wires could also be replaced by a single bidirectional wire. The problem with this configuration is that most data are sent back from the module. During the data transfer it is not possible to synchronize the clock for the detector. To increase the amount of data, it is also possible to run with two bidirectional wires or more than two wires.

The LHC clock is multiplied by 4 or 8 to generate the 160 or 320 MHz serial data clock. The Protocol logic combines the incoming trigger and control signals in packets and vice versa for the data signals. The protocol logic runs at 40 MHz and sends and receives 4 bit (at 160MHz) or 8 bit (at 320MHz) from/to the SER-DES.

On the module side is a clock recovery PLL to regenerate the 160 or 320 MHz clock from the data signal. The protocol controller works similar to the other one but in the other direction.

Figure 14: Overview of a possible communication link configuration between the supply tube to a detector module

VIII. Conclusions

The measurements show that we can build a communication link with less than 10 pJ per bit. 160 Mbit/s is possible with these micro twisted pair cables. 320 Mbit/s should still be tested. Crosstalk is not a problem if we bundle the cables.

IX. Acknowledgements

The following students who were supported by an NSF PIRE grant helped with this project: Tony Kelly (UNL), David Migas and Nick Spizzirri (UIC), Sandra Oliveros (UPRM), and Irakli Chakaberia (KSU).

X. References


Abstract

The basic concept of the Inner Detector in the Atlas Detector upgraded for the Super-LHC is being elaborated and proposed. The readout electronics of this new detector is based on a hierarchical architecture involving front-end chips (FEIC), Module Controller chips (MC) and Stave Controller chips (SC) and a few high speed readout links.

The design is still in a very early phase and a lot needs more detailed studies, however, some architectural issues can already be described. This article will briefly describe the proposed detector layout and its environmental conditions, the proposed readout architecture and the main parameters associated to it (mainly for the strip detector), the different options for the detector control system and the powering of the readout electronics.

I. INTRODUCTION

The basic concept of the Inner Detector in the Atlas Detector upgraded for the Super-LHC is being elaborated and proposed. It is assumed that the small radius layers will be built using pixel detector technology while the mid and large radius layers will be built using silicon strip technology. Furthermore, it is assumed that strips of different lengths will be used in the middle and in the outer layers in order to keep the strip occupancy and the detector leakage current and charge trapping due to radiation damage at acceptable levels.

The readout electronics of this new detector is based on a hierarchical system involving front-end chips (FEIC), Module Controller chips (MC) and Stave Controller chips (SC).

This document will first present the proposed detector layout and its environmental conditions, followed by the readout requirements and some system considerations.

The design study of the detector still in progress and very likely subject to change, some of the information given in this article might become obsolete and inaccurate.

II. UPGRADED DETECTOR

This section gives a short overview of the organisation of the detector for both strips and pixels as well as some of the environmental conditions. Some details concerning the barrel strips detector are also given.

The current straw-man layout [1] is given in Figure 1.

A. Pixel layers

There is not yet a design concept for the pixel detector, however, it is assumed that the most inner layer (B-layer) is made with FEICs 4 times bigger than the current one and that the pixel size is ½ the current one [2]. One FEIC would then handle about 20,000 channels. The outer layers, having lower pixel occupancy, will use a slightly larger pixel size, 250 µm x 50 µm, but still smaller than the current one.

B. Strip layers

Two types of strips are considered: the short strips (2.5-cm length, 80-µm pitch) in the inner most layers and the long strips (10-cm length, 80-µm pitch) in the outer layers. They are all based on detector modules of 10x10-cm²; a long strips module will have 1280 channels while a short strips module will have 4x1280 channels.

The detector will be mounted in double-sided staves (Figure 2) which can be as long as 4-m for the long strips.
Table 1 details the barrel strips detector in number of staves, modules, 128-channel FEIC and number of channels. For comparison, the current silicon strips detector contains 4088 modules, about 50,000 FEIC and 6,000,000 channels.

Table 1: Number of elements in the barrel strips detector.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Type</th>
<th>Radius [cm]</th>
<th>Phi segment.</th>
<th>Modules per half single sided stave</th>
<th>128-ch FEIC per half single sided stave</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Short</td>
<td>38</td>
<td>28</td>
<td>10</td>
<td>400</td>
</tr>
<tr>
<td>1</td>
<td>Short</td>
<td>49</td>
<td>36</td>
<td>10</td>
<td>400</td>
</tr>
<tr>
<td>2</td>
<td>Short</td>
<td>60</td>
<td>44</td>
<td>10</td>
<td>400</td>
</tr>
<tr>
<td>3</td>
<td>Long</td>
<td>75</td>
<td>56</td>
<td>19</td>
<td>190</td>
</tr>
<tr>
<td>4</td>
<td>Long</td>
<td>95</td>
<td>72</td>
<td>19</td>
<td>190</td>
</tr>
</tbody>
</table>

Total number of staves: 236
Total number of modules: 14,336
Total number of 128-ch FEIC: 270,080
Total number of channels: 34 10^6

C. Temperature and magnetic field

The detector will have to be maintained at low temperature (-30°C) and the magnetic field in the tracker volume will be 2T.

D. Radiation level

The upgraded detector will run until a 3000 fb⁻¹ integrated luminosity will be obtained. The detector and its electronics have to be designed for twice as much, i.e. 6000 fb⁻¹.

The total ionising dose (TID) will be about a factor 10 higher than for the current detector and is given in Table 2.

Figure 3 gives the fluence expected in the tracker volume. At the level of the pixel detector, more than 10¹⁵ n.cm⁻² are expected while for the strip detector it is in the range 10¹⁴ - 10¹⁵ n.cm⁻². Note that these numbers take into account the introduction of moderators which are necessary in order to reduce the amount of high energetic neutrons which are very damaging for the sensors.

Table 2: Total ionising dose in kGy for 3000 fb⁻¹ integrated luminosity at different radii.

<table>
<thead>
<tr>
<th>Radius in cm</th>
<th>Dose in kGy</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.05</td>
<td>15800</td>
</tr>
<tr>
<td>12.25</td>
<td>2540</td>
</tr>
<tr>
<td>29.9</td>
<td>760</td>
</tr>
<tr>
<td>51.4</td>
<td>450</td>
</tr>
<tr>
<td>43.9</td>
<td>300</td>
</tr>
<tr>
<td>108</td>
<td>70</td>
</tr>
</tbody>
</table>

III. READOUT ARCHITECTURE

The readout of the current strips detector is organised around the modules: each of the 4088 modules is an autonomous readout entity, meaning that there are 4088 power supply channels and 4088 sets of readout and TTC optical links. Although this architecture has shown to be working, it is not usable for the upgraded tracker because of the large amount of services that it would imply.

Both the pixels and strips architecture must be changed to reduce services per readout channel. The following describes the concepts of the generic architecture for pixels and strips with specific examples for strips and some information for pixels where available.

A. Generic architecture

The architecture will be based on a hierarchical model and the readout electronics system will divided in three main blocks:

- The FEIC handling a number of channels (typically 128 for the strips and up to ~20,000 for the pixel detector);
- The Module Controller (MC) that distributes timing and control to the front-end ASICs of a module and receives data from them;
- The Stave Controller (SC) that distributes timing and control to the modules receives data from them and after concatenation ships the data through a Gbit link to the off-detector electronics.

The MC and SC should also contain the necessary electronics to handle the slow control of the detector, either directly (i.e. including ADCs, DACs, temperature sensors) or interfacing to a separate DCS chip.
Figure 4 shows a schematic view of this generic architecture as described in [1].

![Generic view of the readout electronics.](image)

**Figure 4:** Generic view of the readout electronics.

**B. Readout unit**

The detector is organised in staves regrouping either 10 (short strips) or 19 (long strips) modules. Each stave is made of two layers in order to have a double-sided detector. These two layers will be treated separately from the readout point of view. The data of a single-sided stave will be collected at the level of a stave controller (SC). Each module on the stave has either one (long strips) or two (short strips) readout hybrids. In both cases, the readout unit is the hybrid. The hybrid will host n FEICs (n=20 in the case of the short strips and n=10 in the case of the long strips) and a so-called module controller (MC) which will gather the data of the hybrid FEICs and transmit them to the SC.

Figure 5 is a sketch of a single-sided stave of short strips.

![Sketch of a single-sided stave of short strips.](image)

**Figure 5:** Sketch of a single-sided stave of short strips. 10 modules are readout by 2 hybrids of 20 FEICs each. A stave controller gathers the data from all module hybrids and interfaces to the off-detector electronics. Each hybrid houses a module controller which interfaces the FEICs to the SC. The DCS data can either be sent together with the readout data or be sent on a dedicated link.

**C. Working assumptions**

It is assumed that the current ATLAS binary readout will be used and that the interface to the ATLAS TDAQ system will remain the same although an increase of the level-1 latency is anticipated.

In the current system, the L1A rate does not exceed 100kHz. An increase of this rate would have a dramatic effect on the readout system. For instance doubling this rate would mean either to double the amount of data to be extracted or to perform a selective readout.

However, when defining the needed bandwidth at different places (on modules, from modules to end of staves and from staves to off-detector electronics) some safety margin should be taken. This will allow a bit of flexibility on the L1A rate (and also on the maximum luminosity the machine can reach).

The amount of energetic hadrons (more than 20MeV) susceptible of generating SEU will be very high and hence SEUs will appear everywhere. The following policy will be adopted:

- The static registers holding thresholds, masks, etc. will be implemented with triple redundant logic;
- The “physics data” themselves will not be protected, as a SEU acts as a small excess of noise and because the data do not stay for a long time in the FEICs;
- Level-1 identifier (L1ID) and Bunch Crossing identifier (BCID) will not be protected as they stay a very short time in the front-end. In addition an error is very easily detected in the off-detector electronics and the policy of periodic resets will be maintained (there is a Bunch counter reset every 90 µs and an Event counter reset at a relatively high frequency [order of Hz] which can be used to reconfigure the front-end);
- Special care will have to be taken for the transmission to the front-end of the trigger and control (TTC) as the receiving PIN diodes are very sensitive to SEU;
- Complex logic in the front-end, very likely sensitive to SEUs, will be avoided as much as possible.

There are several different possibilities to organise the readout of the tracker elements and definitely not a unique solution. Each time choices between different options are to be considered, the following criterions will be applied to select one:

- The readout architecture should be as identical as possible for the strips and the pixels so that one can avoid extra design diversity and share as much as possible design efforts and costs. This common approach is to be applied from the front-end electronics up the off-detector electronics. In particular the Readout Drivers (ROD) for the strip and pixel detectors are assumed to be identical (as they are in the current design);
- The material budget is a key element for the upgraded tracker and hence the solutions which minimise the amount of material are always preferred;
- The radiation environment of the front-end electronics will be extremely harsh. In particular a high level of single event upsets can be expected. The readout architecture should be kept as simple as possible and in particular complex tasks such as partial event building, data integrity check, etc. requiring extra buffers in the front-end should be avoided;
- The amount of services connected to the tracker should be kept as low as possible, not only to maintain an overall low material budget (the services located at large radius are less damaging to the calorimeter resolution) but also because the available volume for services routing is severely limited. This will also ease the installation process.

**D. Quantity of data**

Simulations of the strips barrel part [3], based on worst SLHC scenario (50 ns BC period, 400 pile-up events per BC), worst part of the detector (short strips) and a 1.2 to 1.35 safety
factor on the number of hits, have been made. The current readout data format has been used.

Figure 6 shows the distribution of a short strips module event size. The mean number of bits for 40 FEICs is 1554, i.e. 777 for a readout hybrid. A 100kHz L1A would lead to a mean readout speed of 77.7Mbits/s.

Figure 6: Event size for a short strips module (40 128-channel FEICs). The coding scheme is the same as the one used in the current ATLAS SCT detector. The luminosity is $10^{35}$ cm$^{-2}$ and the beam crossing period is 50ns (worst case). A safety factor of 1.35 on the occupancy is applied, however, in the case a DC balanced code is needed, this safety factor is only 1.2.

An 80Mbits/s link between the 20 FEICs of a readout hybrid and the MC would be acceptable as long as sufficiently large derandomising buffers are available in the FEICs. However, as already mentioned, the safety factor used for the simulation is not very large and some uncertainties remain concerning the actual L1A rate which can be obtained and also about the ultimate machine luminosity. In addition, it is anticipated that the pixel detector will require higher bandwidth and hence it is deemed reasonable to implement a 160Mbits/s readout speed per readout hybrid (i.e. for 20 FEICs).

The MC-to-SC links will also have to run at 160Mbits/s and as up to 10 modules (i.e. 20 readout hybrids and hence 20 MC) can be connected to a SC, the output bandwidth of the SC must be at least 3.2Gbits/s. Figure 7 shows the bandwidth requirements in different places.

Figure 7: Bandwidth requirements on the readout hybrids, the stave service bus and the optolinks.

E. Trigger, timing and control (TTC)

The TTC links are used to transmit to the front-end a clock synchronised with the beam (either the LHC clock or a multiple of it), the L1A, fast commands such as the bunch counter reset (BCR) or the event counter reset (ECR), control data to be stored in the FEICs, MCs and SCs (e.g. threshold, masks, ...) and slow commands allowing reading the contents of registers in the different ICs. In order to limit the amount of material, these links will be unidirectional: when reading a register, the command is transmitted on this link but the data will be transmitted on the readout data link. The necessary TTC links bandwidth is dictated by a number of parameters, such as the clock frequency to be transmitted, the need for transmitting simultaneously the L1A and other commands (e.g. Bunch Counter Reset [BCR]), the necessity for transmitting some information with the L1A (e.g. a trigger type), the need for DC balanced codes, etc. The bandwidth of these links should be greater than or equal to 80 Mbits/s.

F. Links

All the links on the staves and hybrids will be electrical. Some studies are on-going in order to assess what is achievable in different places. It is in particular important to select the proper protocols (single high speed data-clock encoded links versus multiple low speed links for instance) and to know whether multi-drop links can be safely used.

The optical links connecting the staves to the off-detector electronics have to run at a reasonable speed but are to be very radiation hard. The project relies heavily on the on-going development of the Versatile Link [4].

G. Data format

The data format used in the current detector is highly optimised in size. The drawback of this optimisation is that the front-end chips have to analyse the transmitted data “on the fly” in order to decide what to do. This might be a problem when large amounts of SEU are expected as complex state machines can be disturbed anytime. It could be better to consider the system as a network and to push packets of data from the FEIC up to off-detector electronics and let the off detector electronics make the necessary work to separate the different types of data (physics data, control data, register contents,...) and to assemble sub-parts of an event. That would simplify the on-detector electronics (very likely at the expense of higher bandwidth for the data transmission) and use efficiently the high power of FPGA in the off-detector electronics.

H. Redundancy

Redundancy can have a large impact on the readout architecture as it could add some complexity and increase the number of devices to be installed (e.g. doubling all the opto-electronics devices if one wants to be fully protected against an optical link failure). Some work is still necessary to evaluate the impact of losing a FEIC, a readout hybrid or a half single sided stave. After that step and based on the expected failure rate of the different components of the system, the need for redundancy can be assessed.

IV. POWER

The power consumption of the FEIC is still unknown but it is deemed very reasonable to assume it will not be higher
than 1 – 1.5mW per channel. Based on this assumption and assuming a (pessimistic) 1.3V Vdd, 100 – 150mA per 128-channel FEIC is needed. The total current for the barrel and end-caps strips detector would then be in the range 33 – 48.5kA. The current ATLAS SCT and TRT detectors (occupying the volume of the future strips detector) are fed with about 12kA. If we take this amount of injected current as an upper limit, a powering scheme allowing a 5 – 6 saving factor on the current one has to be used.

There are on-going developments on serial powering [5] and DC-DC conversion [6]. Both schemes can easily reduce the current to be supplied by the required factor.

At the system level, DC-DC converters offer some very interesting flexibility as they allow easy switching on and off of different elements (e.g. stave controller, readout hybrids) as well as a full separation of analogue and digital supplies leading to some potential saving in overall power. However, there is not yet a viable device today. A serial powering scheme is capable of potentially large saving in current (powering 10 to 20 devices in series is feasible) but some system issues have still to be addressed. Both options must be kept opened for the time being and the readout system must be able to accommodate both.

V. ON-GOING DEVELOPMENTS AND NEXT STEPS

A working document on the readout architecture [7] is available since about a year. It has been reviewed and presented to the collaboration and is going to be updated. Two working groups (one for the pixels and one for the strips) are in place to try and define more precisely the specifications of the different components. These specifications will be used for the design of the different components but also as an input to the “common projects” teams (e.g. for the Giga Bit Transceiver [GBT] project [8]).

Common solutions with other experiments are mandatory for some of the components. The proposed readout architecture involves (for the strips) about 350,000 FEIC but only about 20,000 MC and 5,000 SC. A production of only 5,000 parts in a very high speed technology is absolutely not economically viable.

A full 0.25 μm CMOS readout chip (ABCn [9]) has been developed to be used as a test vehicle for sensor and different power and readout scheme studies. Preliminary study of the front-end part (preamplifier-shaper-discriminator) in 0.13 μm CMOS technology have shown very good power performances (<200μW per channel).

The schedule for the detector and its readout electronics developments is not yet fully understood but looks already very tight: in order to be ready for a full replacement in the year 2017 (to start data taking in 2018) one has to start the staves assembly in the year 2013 with all the final components available...

VI. CONCLUSION

The readout architecture of the ATLAS upgraded tracker has to be different from the current one. The detector will be organised in staves and a hierarchical readout scheme will follow this segmentation. One consequence will be the use of fewer but higher speed readout links.

Some elements of the readout electronics are not to be produced in very large quantity. This points towards common solutions with other experiments.

The power distribution requires special efforts to maintain a reasonable amount of current to be supplied to the detector and consequently a manageable volume of services. A saving factor of the current in the range 5 - 10 has to be achieved.

VII. ACKNOWLEDGEMENTS

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CMS Microstrip Tracker Readout at the SLHC

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Abstract

The increased luminosity at the SLHC and associated increases in occupancy and radiation levels present severe challenges for the CMS tracker, which will require complete replacement. Inner pixellated regions will expand to higher radii and the outer tracker region will most likely be instrumented with short strip silicon sensors. It is also necessary for the tracker to provide information to the level 1 trigger if the overall CMS trigger rate is to remain at 100 kHz.

Power consumption is one of the main challenges for the tracker readout system, because of the higher granularity necessary. The current status of architectures for a short strip outer tracker readout chip is presented, with projections for performance and power consumption.

I. INTRODUCTION

A major challenge for tracker readout systems at the SLHC is power consumption (and provision). Higher luminosity and hence granularity means more sensor channels and front end chips, and the CMS material budget at the LHC is already dominated by electronics power consumption related material (cabling and cooling).

Another major challenge for the CMS tracker at SLHC is the need to provide trigger information, since without this it is not possible to maintain the average level 1 accept (L1) rate at 100 kHz (the LHC value) [1] unless changes are made in the CMS trigger strategy.

Higher granularity and triggering requirements mean that a complete replacement of the CMS tracker is required. It is hoped that power consumption can be controlled by making use of advances in electronics technology, but savings depend on any additional front end functionality required for the SLHC. Advances in high-speed digital optical link technology may help to reduce the resources required to implement off-detector links (using commercial developments).

II. CMS STRIP READOUT AT THE LHC

The current CMS silicon strip tracker readout system at the LHC is illustrated in figure 1. Analogue readout was chosen, with no sparsification (zero suppression) on-detector, utilising 0.25 μm CMOS technology throughout. The APV25 front end chip [2] instruments the AC coupled silicon sensors and the output data from two APV25 chips (figure 2) are combined onto one optical fibre, by the APVMUX chip, at 40 Ms/s. Opto-electrical conversion is performed in the off-detector CMS FED readout boards [3], where digitization, pedestal and common-mode noise subtraction, followed by zero suppression, are performed.

![Figure 1: CMS silicon strip readout system at the LHC](image)

Because of no zero suppression on-detector all front end chips operate synchronously. Taking advantage of this, the state of the front end chips is emulated externally, at the L1 trigger control system level, by the APVE VME module [4]. One function of the APVE is to predict the address of the pipeline location in the APV25 which will be triggered, which is then sent to the FED readout boards. This address is compared with the value subsequently transmitted by all APV25 chips in the system, in the output frame digital header information (figure 2), giving a strong check on the correct functioning of all front end chips.

![Figure 2: APV25 output data frame format](image)

There are other advantages of a synchronous, non-sparsified, system. Since an L1 trigger sent down will result in the return of a data frame from every front end chip, and the L1 latency is fixed, there is no need to timestamp data on-detector. The data volume per trigger is also occupancy independent which greatly simplifies the functionality required to combine data from more than one front end chip onto off-detector links. Transmitting the raw data off-detector allows the functionality of pedestal and common-mode noise subtraction, and zero-suppression to be performed where the associated power consumption is less critical. The raw data are also available to help set up, diagnose any suspected faults with, and monitor the performance of the front end system.

The analogue, non-sparsified approach provides a relatively simple and robust readout system for the CMS strip tracker at the LHC.
III. SOME POSSIBLE SLHC CHIP ARCHITECTURES

Figure 3 shows a functional representation of the 128 channel APV25 chip used for strip readout at the LHC. The APV25 [2] uses a relatively slow front end amplifier which produces a 50 ns CR-RC shape pulse, sampled into the pipeline at the 40 MHz bunch crossing frequency. The pipeline is implemented by gate capacitance, which gives the highest capacitance per chip area possible in the process.

![Functional block diagram of the APV25 readout chip](image)

In response to an L1 trigger, the analogue samples stored in the pipeline can be read out in either peak or deconvolution modes [2], where deconvolution mode provides single bunch crossing resolution for signals.

The analogue approach of the APV25 allows pulse height information to be retained and transmitted, but is clearly incompatible with digital off-detector transmission envisaged for the SLHC. If pulse height information is to be retained it becomes necessary to consider where to introduce the digitization step in the analogue chain.

Digitization early in the signal processing chain, before the pipeline, allows analogue functionality to be confined to the front edge of the chip, and a digital pipeline is possible, which should lead to a minimal area requirement for this circuit. This requires an ADC on every channel and table 1 gives power estimates for 6 or 8 bit ADCs running at 20 MHz (one of the proposed bunch crossing frequencies for the SLHC) in 130 and 65 nm technologies. The numbers in the table are based on International Technology Roadmap for Semiconductors (ITRS) 2003 predictions [5].

Table 1: Power estimate, in mW, for a 20 MHz CMOS ADC based on the ITRS roadmap 2003 [5]

<table>
<thead>
<tr>
<th>Technology</th>
<th>130 nm</th>
<th>65 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 bits</td>
<td>6.4</td>
<td>2.5</td>
</tr>
<tr>
<td>6 bits</td>
<td>1.6</td>
<td>0.6</td>
</tr>
</tbody>
</table>

The power consumption per channel for the present APV25 based readout is 2.7 mW, and a significant reduction in this value is required for SLHC. From table 1 it is clear that an ADC on every channel is not a viable option, even at 20 MHz, and it is also possible that the bunch crossing frequency at SLHC may remain at the LHC value of 40 MHz.

Retaining pulse height information without an ADC on every channel means that the required digitization must be performed at a point where the channel information has been brought together, and an obvious option is then to digitize after the multiplexing stage. Figure 4 illustrates this, where the ADC power is shared between all channels. For example, 6.4 mW shared between 128 channels results in a power consumption per channel of only 50 µW.

Digitization after the multiplexing stage requires that the analogue pipeline and multiplexing stage present in the APV25 is retained, and the slow shaping (plus deconvolution) feature could also be retained. Implementing the pipeline using gate capacitance may not be an option as the gate oxide thickness reduces with feature size, and significant leakage results. It may still be possible in 0.13 µm technology, but not for finer feature processes, which would have implications for overall chip size as other capacitor implementations tend not to be so area efficient.

![Functional block diagram of an APV-like chip with on-chip ADC](image)

Figure 4 includes a further block between the ADC and output data serializer stage, where additional functionality could be implemented, such as the pedestal and common-mode noise subtraction currently implemented off-detector in the LHC system. It will be shown in section IV that digital data volumes and associated transmission power at SLHC will dictate that sparsification is necessary if pulse height information is retained.

Comparing the existing APV25 and “digital APV” architectures in figures 3 and 4, it is clear that the digital APV contains all the complexity of the APV25, plus additional complexities of digitization and on-chip sparsification, which will not help to keep power consumption low. On chip sparsification will also add complexity to the overall front end system, losing some of the attractive features of the present system already discussed in section II. The opposite extreme to a digitized analogue, sparsified readout system in terms of complexity is binary, non-sparsified readout.

Figure 5 shows a binary non-sparsified architecture. For binary readout a fast front-end amplifier and comparator are required. The front-end amplifier speed must be sufficient to enable the hit to be registered in the correct bunch crossing.

![Functional block diagram of a binary, non-sparsified front end chip architecture](image)
Although the architecture in figure 5 does not look greatly different to that in figure 3, the implementation of the functional blocks would be substantially simplified. The pipeline is only one bit per channel and the area it would occupy would be small. The readout would just require the retrieval of a 128 bit digital word from the pipeline and a simple 128:1 digital multiplexer operation, the resulting data stream being transferred directly off-chip.

It seems likely that the digital power associated with an architecture like that in figure 5 would be low. Front end power cannot be as low as for slow shaping, because of the speed requirement and additional comparator functionality.

IV. SLHC CHIP POWER ESTIMATES

A. Front end amplifier simulations

The APV25 was designed for long strips with sensor capacitances, $C_{\text{SENSOR}}$, in the range 15 – 25 pF. The noise performance and rise-time of a charge sensitive preamplifier depends on $C_{\text{SENSOR}}$ and $g_m$, the transconductance of the input FET, according to the formulae:

$$\text{noise} \sim C_{\text{SENSOR}} / \sqrt{g_m}, \quad \text{rise-time} \sim C_{\text{SENSOR}} / g_m$$

For short strips at SLHC, $C_{\text{SENSOR}}$ is reduced, so lower values of $g_m$ are possible. $g_m$ depends on drain-source current, and supply voltages are halved when moving from 0.25 µm to 0.13 µm technology so significant savings in input device power are possible.

![Figure 6: 0.13 µm preamp/shaper circuit for simulations](image)

Figure 6 shows the transistor level schematic of a simple preamplifier/shaper circuit used to evaluate the performance achievable in 0.13 µm CMOS. A simple two supply rail circuit is chosen with a PMOS input device. The bias currents to the preamplifier and shaper input devices, IPRE and ISHA, together with the shaper feedback resistor Rs, were varied to achieve the two different CR-RC pulse shapes in figure 7. The 50 ns pulse shape might be suitable for a digital APV type architecture like that in figure 4, whereas the 20 ns pulse shape would be more suitable for a binary front end. A sensor capacitance of 5 pF was chosen, which would correspond to strip lengths of ~ few cm.

Table 2 shows the values of bias currents chosen to achieve the pulse shapes in figure 7, together with the corresponding power and simulated noise performances. It can be seen that for a 0.13 µm front end for short strips a good noise performance is achievable for substantially less than the ~1 mW required for the APV25 preamp/shaper.

<table>
<thead>
<tr>
<th>Sub-circuit</th>
<th>Power [µW]</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preamp/shaper</td>
<td>120</td>
<td>Simulated 50 ns CR-RC shaping, $C_{\text{SENSOR}} = 5$ pF</td>
</tr>
<tr>
<td>Pipe readout</td>
<td>50</td>
<td>APV25 / 4 (guess)</td>
</tr>
<tr>
<td>ADC</td>
<td>50</td>
<td>Estimate from [ITRS]</td>
</tr>
<tr>
<td>digital</td>
<td>120</td>
<td>(APV25/10) x 3 - see text</td>
</tr>
<tr>
<td>Fast serial O/P</td>
<td>230</td>
<td>30 mW / 128 (based on estimate for fast LVDS)</td>
</tr>
<tr>
<td>Total</td>
<td>570</td>
<td></td>
</tr>
</tbody>
</table>

![Figure 7: Simulated pulse shapes for the circuit of figure 6, for $C_{\text{SENSOR}} = 5$ pF and with the bias currents in table 2.](image)

B. Overall SLHC chip power estimates

Table 3 shows the power breakdown by functional sub-circuit of the existing APV25 chip. Tables 4 and 5 show estimated power consumptions, in similar format, for digital APV and binary non-sparsified architectures respectively, in 0.13 µm technology. Justifications for the numbers are indicated in the tables, but it should be emphasised that there are considerable uncertainties where estimates are provided for digital functionalities. Nevertheless a target power consumption of close to 0.5 mW per sensor channel seems appropriate for a 0.13 µm chip for short strip readout.

![Table 3: 0.25 µm APV25 power breakdown](image)

<table>
<thead>
<tr>
<th>Sub-circuit</th>
<th>Power [µW]</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preamp/shaper</td>
<td>120</td>
<td>Simulated 50 ns CR-RC shaping, $C_{\text{SENSOR}} = 5$ pF</td>
</tr>
<tr>
<td>Pipe readout</td>
<td>50</td>
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</tr>
<tr>
<td>ADC</td>
<td>50</td>
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</tr>
<tr>
<td>digital</td>
<td>120</td>
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</tr>
<tr>
<td>Fast serial O/P</td>
<td>230</td>
<td>30 mW / 128 (based on estimate for fast LVDS)</td>
</tr>
<tr>
<td>Total</td>
<td>570</td>
<td></td>
</tr>
</tbody>
</table>

![Table 4: Estimated 0.13 µm digital APV power / channel](image)

<table>
<thead>
<tr>
<th>Sub-circuit</th>
<th>Power [µW]</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preamp/ shaper</td>
<td>180</td>
<td>Simulated 20 ns CR-RC shaping, $C_{\text{SENSOR}} = 5$ pF</td>
</tr>
<tr>
<td>comparator</td>
<td>20</td>
<td>Simulated</td>
</tr>
<tr>
<td>digital</td>
<td>60</td>
<td>Simpler than digital APV</td>
</tr>
<tr>
<td>Fast serial O/P</td>
<td>230</td>
<td>Same as digital APV</td>
</tr>
<tr>
<td>Total</td>
<td>490</td>
<td></td>
</tr>
</tbody>
</table>
C. Estimated link power contribution

Overall system and front end chip architectures are inter-dependent. Data from front end chips must be merged to make efficient use of off-detector link bandwidth, and data volumes depend on whether or not pulse height information is retained, ADC resolution, and whether sparsification is employed.

Table 6: Estimated link power contributions for different front end chip (128 channels) architectures

<table>
<thead>
<tr>
<th></th>
<th>Link speed Gb/s</th>
<th>No.of chips / link</th>
<th>Power/ link</th>
<th>Link power/ sensor chan.</th>
</tr>
</thead>
<tbody>
<tr>
<td>APV25 non-sparsified analogue</td>
<td>0.36 (eff.)</td>
<td>2 / fibre</td>
<td>60 mW</td>
<td>230 µW</td>
</tr>
<tr>
<td>Digital APV non-sparsified</td>
<td>2.5</td>
<td>32/ GBT</td>
<td>~2 W</td>
<td>490 µW</td>
</tr>
<tr>
<td>Digital APV sparsified</td>
<td>2.5</td>
<td>256/ GBT</td>
<td>~2 W</td>
<td>60 µW</td>
</tr>
<tr>
<td>Binary non-sparsified</td>
<td>2.5</td>
<td>128/ GBT</td>
<td>~2 W</td>
<td>120 µW</td>
</tr>
</tbody>
</table>

Table 6 shows estimated link power contributions for the different choices of front end chip architectures discussed in section III. For the APV25 LHC non-sparsified analogue case, the data from 2 APV25 chips are transmitted at 40 Ms/s on one fibre. Analogue samples are digitized off-detector with an effective resolution of 9 bits, giving an effective link data rate of 0.36 Gb/s. The link power contribution / sensor channel is less than 10% of the overall front end channel power budget at the LHC (table 3).

The remaining three rows in table 6 deal with candidate front end chip architectures for SLHC, where it is assumed that the off-detector link will be implemented by the GigaBit Transceiver (GBT) currently under development [6]. The GBT available data bandwidth is taken to be 2.56 Gb/s, with a power consumption of 2 W, organized as 32 x 80 Mb/s lanes.

For the non-sparsified digital APV (128 channels) a 6 bit ADC is assumed, giving 77 Mb/s to transmit for a L1 trigger rate of 100 kHz. This theoretically allows 32 chips per GBT. The power/sensor channel of 490 µW is too large, being approximately the same as the target power consumption of the front end chip itself (at the SLHC). The ratio of 77 Mb/s data rate to 80 Mb/s available link rate leads to a link bandwidth use efficiency factor (ratio of transmitted data rate to maximum available digital data bandwidth) of 96% which would be unfeasible to implement in practice.

For the digital APV with sparsification case a 6-bit ADC and an occupancy of 4% is assumed, leading to 5 hits per 128 channel chip on average. For each hit 13 bits are required (7 bits address + 6 bits pulse height), and a 20 bit header is added to incorporate timestamp (12 bits) and chip identity. This gives an overall average data packet of 85 bits and so a data rate of 8.5 Mb/s at 100 kHz L1 rate. Combining data from 8 chips on an 80 Mb/s GBT lane gives a combined data rate of 68 Mb/s, with a link bandwidth use efficiency of 85%.

For the binary non-sparsified case only 1 bit per hit is transmitted and data volume is occupancy independent. An extra 16 bits per trigger are added to allow for the transmission of header information, including the address of the triggered pipeline location as is done in the digital header for the present system (figure 2). This leads to a data volume per L1 trigger of 144 bits and a data rate of 14.4 Mb/s at 100 kHz L1 rate. 128 chips per GBT are possible with a comfortable link bandwidth use efficiency of 72%.

While the sparsified digital APV architecture gives the least link power contribution per sensor channel, the added power and system complexity associated with merging fluctuating trigger-to-trigger data volumes must be taken into account.

V. Triggering

The overall L1 trigger rate at SLHC cannot be maintained at 100 kHz without transverse momentum (P_T) information from the tracker [1], assuming the same trigger strategy is used as that planned for LHC luminosity. Ideas presented here are based on the assumption that there will probably be one or more P_T layers, dedicated to providing information for the L1 trigger decision.

Some concepts which have been previously presented include the stacked tracking approach [7], where P_T discrimination is achieved by correlating hits in closely spaced layers, and cluster width discrimination [8], where high P_T tracks in a single sensor layer can be identified by their narrow cluster width. The concepts are clear, but issues associated with practical implementations (construction details, power consumption, cost) need further understanding.

Figure 8 shows a possible implementation of the stacked tracking approach, for an inner layer at 25 cm radius, which could extend over the full pseudo-rapidity range of the existing tracker. A P_T module with dimensions 25.6 mm x 80 mm is constructed from 2 silicon sensor layers, each tiled with 32 readout chips, each chip instrumenting 256 pixels (2 x 128 columns) with a pitch of 100 µm and 2.5 mm long. The readout chips could be wire-bonded to the sensor. A correlator chip receives signals from both layers.

![Figure 8: A possible PT module for a 25 cm radius layer.](image-url)
The $P_T$ module contains 8192 pixels (per layer) with a predicted occupancy of 0.5% at 40 MHz and $10^{35}$ cm$^{-2}$s$^{-1}$ luminosity. The correlation operation is expected to reduce the hit rate by a factor ~20, giving a “high $P_T$ occupancy” of 0.025% (0.5%/20). Thus the number of positive correlation results per $P_T$ module per bunch crossing should be only two (0.025% x 8192). It is necessary to transmit all the positive correlation results every bunch crossing, and 64 bits are available every 25 ns, for a 2.56 Gb/s off-detector link, so one link can handle data from 2 $P_T$ modules.

Approximately 3000 $P_T$ modules would be required to tile the surface of a 3m cylindrical layer at 25 cm radius (allowing for modules overlapping) so 1500 off-detector links would be required, consuming 3 kW in total for 2 W per link. Extrapolating the readout power for the current pixel system to 50 $\mu$W/pixel for the $P_T$ layer pixels gives 8192 pixels/layer x 2 layers/$P_T$ module x 3000 modules x 50 $\mu$W = 2.4 kW. This does not include any extra power for the other digital functionality (correlation operation and short distance digital transmission), so it can be seen that a $P_T$ layer implemented in this way would be a high power layer.

![Figure 9: A possible PT module for an outer layer [9].](image)

Figure 9 shows another possible idea for implementing a stacked tracking $P_T$ layer module [9], this time for an outer tracker layer. For the lower outer layer occupancy, the module could be implemented using relatively long strips with readout chips wire-bonded at the end. The novel idea in this case is to bond neighbouring chip channels alternately to strips in the upper and lower sensor planes, such that correlations between planes can be made on the same readout chip, between neighbouring channels, and no extra correlator chip is required. It is likely that this would save power and material, and costs could be minimised if DC coupled sensors could be used. The correlation operation, which also uses cluster width discrimination so that the correlation between planes is only performed for high $P_T$ tracks, can be implemented with relatively simple logic.

The two triggering layer ideas presented, figures 8 and 9, are included to show recent progress in this area. More work is needed to understand details of performance and practical implementation, and alternative ideas may be preferred or develop in the future.

**VI. SUMMARY**

The CMS silicon strip readout architecture for SLHC is not yet defined, and major challenges of power consumption and provision of information to the first level trigger decision must be confronted. The pros and cons of different front end chip architectures are under consideration, involving compromises between power consumption, front end chip and system complexity, system robustness and performance.

A readout chip development programme will begin soon, beginning with front end test structures matched to different sensor options (polarity, strip length, DC coupling), progressing to a full chip prototype in the second year, when decisions will be needed on system issues (e.g. binary/sparsified analogue architecture, powering scheme (serial/parallel), and sensor choices).

It seems likely that a binary, non-sparsified architecture could lead to minimum front end chip power consumption, while also retaining some of the valuable features of the existing LHC system, but the disadvantages of abandoning the pulse height information must also be considered.

A simpler strip readout chip and system architecture would require less resources to develop, and resources will be needed to confront the triggering issues, where ideas are still evolving. It is clear that there will be dedicated chip developments required in this area.

**VII. ACKNOWLEDGEMENTS**

We would like to thank the UK Science and Technology Facilities Council for supporting this work. Thanks also to R.Horisberger and W.Erdmann for permission to show their outer layer $P_T$ module design (figure 9).

**VIII. REFERENCES**

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Upgrade of the Readout Electronics of the ATLAS MDT Detector for SLHC

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Abstract

Simulation predicts a high level of ionizing radiation in the ATLAS experimental hall during LHC operation. This radiation will act as a source of background signals to the four subsystems of the ATLAS muon detector. We present the performance of the Monitored Drift Tube detector (MDT) under these background conditions and discuss the consequences for the much higher background rates at SLHC with respect to tracking efficiency, resolution and readout bandwidth. For rates beyond the expected LHC levels, we discuss options to improve the performance of detector and electronics.

I. INTRODUCTION

The MDT chambers form the outermost part of the ATLAS experiment and are designed to measure the position of tracks with a precision of about 80 μm. MDT chambers are arranged in layers, in such a way as to measure the coordinates of each track at three locations along its trajectory, allowing to determine its momentum from the curvature in the magnetic field. The MDT chamber layers form three concentric cylinders around the beam axis in the central part of the detector and three wheel-like structures in the forward and backward part. A detailed presentation of the muon system and of the MDT readout electronics is given in [1] and [2], respectively.

As the calorimeters in the central part absorb most hadrons, electrons and γ’s, only muons will penetrate into the outer region and only an average of about 1.5 muons above 6 GeV are expected in any triggered event. Thus, only a small number of chambers (out of 1200) contains tracking information in any given event.

Most of the MDT chambers are matched by a corresponding trigger chamber. These chambers use the RPC and TGC technology in the barrel and end-cap region, respectively. Compared to the MDT, trigger chambers are less precise in measuring the track position, but have much better time resolution (10–15 ns), which allows tagging of the beam crossing. Pairs of trigger chambers are used to define track slopes with respect to the direction towards the interaction point, from which the track’s curvature, i.e. momentum is derived for use in the LVL1 trigger decision. The track slopes are also used as search roads for muon localisation in subsequent levels of triggering and in the offline analysis. The search roads for muon tracking are called ”Regions of Interest” (RoI). The precise determination of the muon momentum at LVL2 and in the Event Filter (EF) is entirely based on tracks flagged by the RoIs. At low luminosity where the track pattern in the tubes is little obscured by background hits, the offline analysis may find additional tracks, not flagged by trigger chambers, adding so called ”soft RoIs”. A detailed description of the ATLAS triggering system is given in [3] and [4].

At LHC the large majority of hits in the MDT detector is not caused by charged tracks but by converted γ’s which are generated by slow neutrons, leaking from calorimeters and shielding material. These ”background hits” from converted γ’s are the limiting factor for the rate capability of the MDT. Hit rates and ionization created in the tube gas by the γ-background affect the main performance parameters of the MDT, like tracking efficiency, position resolution and readout bandwidth. The SLHC will deliver much higher luminosity and background rates than the LHC. Hence, for an upgrade of the MDT, solutions have to be found to overcome the limitations of the MDT with respect to the high background rates.

II. SIMULATED γ FLUX IN THE EXPERIMENTAL HALL

The background hit rate in the MDT detectors depends on the γ-flux in the experimental hall. Figure 1 shows the simulated γ-flux as given in [5].

Figure 1: Gamma flux in the ATLAS experimental hall. The area colored in blue depicts the region of relatively low γ-flux, where the MDTs of the barrel (BI, BM and BO) and
those of the outer parts of the middle and outer wheels (EM and EO) are located. In contrast, the inner parts of the inner and middle wheels (EI and EM), in the areas coloured in yellow, receive about a factor of ten more $\gamma$-flux. Reference [5] explains the high flux in the forward part from the fact that elastically scattered protons from the interaction point hit the beam pipe about 10 m downstream, creating an intense source of secondary particles. Because of the limited space between beam pipe and inner bore of the end-cap toroidal magnet, shielding in this region is not as effective as around the interaction point, where the calorimeters provide tight shielding.

The uncertainties of the simulated flux are estimated to be composed of a factor of 1.5, due to uncertainties of the cross section at the primary vertex and by a factor of 2.4 for the error on the particle transport across the shielding material. For the hit rates in the MDT chambers there is an additional uncertainty of 1.4 due to the absorption of the $\gamma$’s in the material of the tube (aluminum wall and gas). The compounded error on the predicted background hit rates in the MDT tubes results in $1.5 \times 2.4 \times 1.4 \approx 5$. Assuming that actual hit rates may exceed the simulated ones by this large factor, all rate estimations in this paper are applying the “safety factor” of 5.

For the extrapolation of hit rates from LHC to SLHC, a factor of 10 is applied, corresponding to the anticipated luminosity increase. A reduction of this factor of 10 may occur if the currently used stainless steel beam pipe was replaced by a beryllium pipe, which might reduce rates in the forward direction by a factor 2–3. If, in contrast, the SLHC upgrade leads to a displacement of the final focus magnets in direction to the interaction point, part of the space presently used for shielding may have to be given up, which may raise the background and partly or fully compensate the improvements due to the beryllium pipe.

The error range on expected rates will be reduced as soon as the LHC will operate under close-to-nominal conditions. For the purpose of the discussion in this article we assume that background rates in the MDT detector will be 5 times and at the SLHC 50 times the ones simulated.

### III. Expected Tube Hit Rates Due to $\gamma$-Flux and Consequences for the MDT

The $\gamma$-flux in the experimental hall translates into hit rates in the tubes of the MDT system as shown in figure 2. At the inner tip of the EI and EM wheel the rates are 10–15 times higher than in the BI layer of the barrel. The variation is partly due to the $\gamma$-flux and partly due to the tube lengths in the different chamber types.

The background rates from the $\gamma$-flux lead to inefficiencies of the tube in recording $\mu$-tracks, as a $\gamma$-hit preceding the passage of a track may mask the signal produced by the track. Missing tube hits along the trajectory of the track may reduce the reconstruction probability of this track, leading to a possible misidentification or loss of a physics event. Therefore, if a luminosity increase leads to a reduction of reconstruction efficiency beyond a certain point, the benefit of higher event rates may be
outweighed by a loss in the significance of the physics signal. Thus, a careful analysis of the rate capabilities of the MDT is a mandatory step in the preparation of a luminosity upgrade as planned for the SLHC.

The rate capabilities of the MDT have been tested at the Gamma Irradiation Facility (GIF) at CERN where high momentum muon tracks were crossing a MDT chamber in the presence of an adjustable high intensity γ-source, [6, 7]. The position of the muon tracks was known with an accuracy of about 20 μm due to the presence of silicon strip detectors. Figure 3 shows the hit efficiency of a single tube versus background count rate, while figure 4 gives the reconstruction efficiency for the corresponding tracks. At 5 × nominal the track reconstruction efficiency is between 88 and 95%, depending on the reconstruction algorithm.  

![Figure 5: Position resolution as a function of γ-flux.](image)

Figure 5 shows the position resolution of a given tube versus the impact radius of the track at five different levels of γ-flux. The degradation of position resolution with increasing background rates comes from space charge accumulated in the drift volume due to positive ions, an effect which grows with the length of the drift of the primary electrons, as can be seen in the figure. The average position resolution per tube degrades from about 80 μm at zero background to about 120 μm at 5 × nominal LHC rates. This is considered still acceptable for most of the physics channels under consideration.

Another consequence of the background rates is the data volume to be transferred to the rear end electronics. Figure 6 shows the level of saturation (%) of the optical readout links of a typical large and average chamber vs. the hit rate of the individual tubes. At a hit rate of 125 kHz a data rate of about 300 Mbit/s is transferred to the Readout Driver (ROD) for an average chamber of 288 tubes, corresponding to about 20 % of the available bandwidth of the link (about 1.4 Gbit/s for user data), while at 360 kHz, which corresponds to rates in the end-cap, about 50% of the available bandwidth are used. For a large chamber with 432 tubes, the same background conditions lead to 33% and 66% saturation, respectively. For comparison: a BI chamber in the barrel with 240 tubes and 25 kHz rate per tube, only uses about 8% of the available bandwidth.

These numbers demonstrate that link saturation at LHC is below a value of about 2/3, even in the hottest regions. For operation at SLHC, however, the presently available bandwidth is largely insufficient.

![Figure 6: Level of saturation of the optical links for two chamber types versus tube hit rate.](image)

Figure 6: Level of saturation of the optical links for two chamber types versus tube hit rate. The maximum bandwidth on the link, available for user data is 1.4 Gbit/s. The overhead produced by the TDCs (two 32-bit words per trigger) creates an occupancy of the link of 8–12% (depending on the number of tubes), even if no hits are present. All numbers refer to a LVL1 trigger rate of 100 kHz.

A diagram of the readout scheme of the MDT is shown in figure 7. The number of 325 kHits per tube is for a chamber in the “hot” region, which leads to an average occupancy per triggered event of about 50%. With 288 tubes (an avg. chamber), 700 Mbit/s are transferred over the optical link to the ROD. The ROD, receiving data from up to six chambers, achieves a significant reduction of the data volume by discarding control data (empty data frames, synchronisation words etc.). The output is sent via a S-link to the ROB, where data are stored for analysis by the LVL2 trigger and the Event Filter (EF) and, eventually, permanent storage. The ROD is thus condensing up to six input data streams from the MDT into one output data stream to the

1The reconstruction efficiency of an algorithm is, in general, complementary to the fake track rate, so the selection of the optimum algorithm is quite difficult.

2There is an overhead of data frames and control words which leads to a “base” data volume of about 110–160 Mbit/s at 100 kHz LVL1 trigger rate, even if no hits are present in the chamber. Most of this overhead is discarded in the next processing stage, the ROD.
ROB. Even with the data reduction in the MDT, this is only possible because most MDTs at LHC operate at data rates far below saturation. Care is taken to balance the data loads for each ROD by combining high rate with lower rate chambers. Details of this "load balancing" in the ROD are given in [8] and [2].

Consequently, at the much higher rates of the SLHC, the present architecture would not allow the RODs to service up to six CSMs, if backward pressure from the ROBs (i.e., data loss and/or additional dead time) is to be avoided. If only the available bandwidth for data readout was the limiting factor, a single ROD could be used for each CSM, while the bandwidth of the optical links between CSM and ROD and between ROD and ROB would have to be increased. A requirement of, e.g., 2.5 Gbit/s could be put into reality using new optical links like the GBT (see this conference). As for the RODs and ROBs, the processor speed and architecture would have to be reviewed for handling the increased data rates. However, as discussed above, the present MDT chambers would become unacceptably inefficient at such high hit rates and would have to be replaced by chambers of a different type. The present MDT technology could only be maintained in regions where the hit rate does not exceed 400 kHz per tube.

IV. UPGRADE STRATEGIES FOR THE MDT IN A SLHC ENVIRONMENT

As a consequence of the previous section, the present MDT detectors, characterized by their diameter of 30 mm, can only operate up to a tube hit rate of about 400 kHz if an efficiency for track hits of ≥ 70% is to be maintained. In the forward regions of the MDT these limits will most likely be exceeded by factors of 5–10 and alternative concepts for tracking chambers must be found.

We present two options for an upgrade with tube-based detectors. Alternative chamber types with pixel-like structure (e.g., GEMs, Micromegas) may also be considered candidates for an upgrade but are not discussed in this paper.

A. Small tubes

A drastic improvement of the rate capabilities of the MDT tube detectors could be achieved by a reduction of the tube diameter from 30 mm to e.g., 15 mm. This will reduce the drift time, and with it the sensitive time for background hits, by a factor of 3.5 due to the non-linear characteristics of the space-to-drift time relation in the ArCO$_2$ gas, see figure 8. A further reduction of the background hit probability comes from the shorter track segment crossing the tube, which leads to shorter pulses and hence to a reduced probability for converted γ’s to mask subsequent track hits. Another reduction comes from the two times smaller area exposed to γ’s. Compounding these figures, a total hit rate reduction of 7 is expected, while the probability for an inefficiency due to hit masking is reduced by a factor of about 20 due to the additional effect of shorter signal length.

The small tubes also allow more tube layers to be installed in the available space, leading to improved position resolution and robust tracking in the presence of tube inefficiencies.

B. Field shaped tubes

An alternative way to reduce the active volume in drift tubes has been proposed by J. Chapman et al. (University of Michigan)
gan). Figure 10 shows a 30 mm tube, where two plates have been added, roughly at half-distance between wire and wall. The potential of the two plates is close to the potential of the wire, deforming the drift field in such a way that only a small region of about 4 mm thickness has field lines ending at the wire. Only primary ionisation originating from this region drifts to the wire and undergoes gas amplification, while ionisation from other regions drifts to the field plates where little or no amplification takes place. This way, only a short fraction of the track contributes to the observed signal, leading to a short pulse and a small probability of masking. The hit rate is also strongly reduced, as the ionisation of many converted $\gamma$'s does not reach the central wire.

For optimal position resolution, tracks should cross the drift field at right angle. Therefore, all tubes in a chamber should be turned towards the interaction point ("clocking").

A set of tubes to be tested at the GIF facility is currently in preparation.

![Figure 10: Reduction of the active volume in a tube with field shaping plates. Primary ionisation created outside a 4 mm wide drift layer does not drift to the amplifying central wire but is collected by field plates, where no significant amplification takes place. Field lines not ending on the central wire are not shown.](image)

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**C. Upgrade of electronics**

The large increase of occupancy at the MDTs calls for a corresponding upgrade of the readout bandwidth and storage capacity of the on- and off-chamber storage elements (TDC, CSM, ROD, ROB) as discussed in section III. However, as mentioned in section I., the large majority of the transferred data will not correspond to a RoI, i.e. contain a charged track, and the majority of the other MDTs, which only contain background hits. The data of the latter could be deleted already at the level of the CSM and would thus cease to contribute an unnecessary load to the readout system.

Data not marked by a RoI can be safely discarded, because

- the LVL2 and the EF, guided uniquely by the RoI, would not consider them for the trigger decisions,
- at high background the offline tracking algorithms would not be able to identify additional tracks (not labelled by a RoI), because track recognition from tube hit patterns is not possible, the background of fake tracks being far to large.

Figure 11 shows a possible readout scheme for selective readout. The role of the "Readout Selector" is to derive, for each RoI supplied by the MuCTPI, a list of chambers which may contain segments of the corresponding track. If a RoI was flagged, e.g. by a track segment in the middle layer of the barrel, all three barrel chambers along the track (i.e. a full barrel "tower") would have to be read out, see figure 12. Based on this list, the Readout Selector sends a YES or NO to the corresponding CSMs.

As most chambers do not have a track (hence no RoI), this readout scheme would lead to a reduction of the transferred data volume by a large factor, reducing the required bandwidth on

![Figure 11: Schematic diagram of the muon trigger system and a possible implementation of selective readout.](image)

Figure 11: Schematic diagram of the muon trigger system and a possible implementation of selective readout.

Obviously, the information prepared for the LVL2 could also be used to discriminate between those MDTs which correspond to a RoI, i.e. contain a charged track, and the majority of the other MDTs, which only contain background hits. The data of the latter could be deleted already at the level of the CSM and would thus cease to contribute an unnecessary load to the readout system.

Data not marked by a RoI can be safely discarded, because

- the LVL2 and the EF, guided uniquely by the RoI, would not consider them for the trigger decisions.
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As most chambers do not have a track (hence no RoI), this readout scheme would lead to a reduction of the transferred data volume by a large factor, reducing the required bandwidth on
the optical links and the storage capacities of the ROD and ROB processors. Based on the muon rates predicted for LHC and SLHC, a reduction factor of 10–50 can be expected. Even if only a factor of 10, the bandwidth of the present LHC links would be sufficient for SLHC.

The data transfer between TDCs and CSM would, of course, not profit from this data reduction scheme. All hits recorded by the TDC would have to be transferred to the CSM, which would mean an increase in storage capacity in the TDC and of the transfer rate to the CSM, cf. figure 7.

Due to the tenfold higher level of ionizing radiation at SLHC a total ionizing dose (TID) of up to 500 krad would have to be expected in ten years of operation. For newly designed ASICs this should not be a problem, as technologies with much higher tolerance are available.

Figure 12: Cross section through a “tower” of three barrel chambers, showing MDT as well as RPC trigger chambers. RoIs are generated by coincidences between hits in RPC layers which allows to find tracks in the MDT, even at high occupancy. Track segments found in the outer and middle MDT are extrapolated to the inner layer which is not equipped with RPCs. In selective readout mode a whole tower of MDTs would be read out if there is any RoI in it. If the track is flagged to be in the overlap region, i.e. the track is close to a tower boundary and might, due to its curvature, migrate to the adjacent tower, the adjacent tower is also read out.

As for the FPGAs in the CSM processors, the currently used XILINX Virtex-II devices started to fail in tests at about 50 krad TID and would, therefore, not be suitable for SLHC applications in the experimental hall. The radiation performance of more recent FPGA families seems not yet to be demonstrated. Therefore, it seems uncertain whether Field Programmability at the frontend can be maintained for the SLHC.

V. SUMMARY

The muon detector in its present form would be able to support a moderate luminosity upgrade by about a factor of 2, if background rates in the hall were reduced e.g. by the installation of a Beryllium beam pipe, and if the present shielding structure was maintained (i.e. no loss of shielding due to modified beam optics). To make the MDT system usable for 10 times higher rates, as foreseen for the SLHC, a number of chambers in the forward direction of the end-cap would have to be replaced by chambers with reduced acceptance for γ−conversions, using new drift tube technologies.

For the chambers in the barrel and in the outer end-cap region, a replacement of the on-chamber electronics may be sufficient to improve readout bandwidth and radiation tolerance. Optical readout links and off-chamber processors could be maintained if a new readout concept was implemented which only transfers relevant tracking data, using the guidance of the RoIs, as provided by the trigger chambers.

A number of R&D projects are prepared to address the relevant questions.

REFERENCES

THURSDAY 18 SEPTEMBER 2008

TOPICAL 2

LESSONS FROM LHC
Some Lessons from the LHC Projects

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The LHC Experiments have been Successfully Commissioned
It is now Useful to Reflect on the Progress we have made over the Construction and Commissioning of these Complex Projects and to Ask how Best to Prepare for the SLHC?

This Presentation will Review:
- Access to Microelectronics Technology
- Microelectronics and Tracking Detectors
- Opto-electronics Systems
- Power Systems, Grounding and Shielding
- Off-Detector Systems

In the Beginning (1)
- In the Mid 1980s the European Electrical Engineering Communities were beginning to teach the design of Microelectronics for MSc Courses
- This required access to Design Tools, Lithography, Fabrication and Circuit Evaluation (~ 5μ Technology)
- Facilities to support the need for an increased number of trained Engineers were established throughout Europe
- One such Facility was an EU project called ‘Euro-Chip’

In the Beginning (2)
- In the Mid 1980s Bernard Hyams and Terry Walker had demonstrated the readout of a Silicon Strip Detector using an NMOS Integrated Circuit. Good Performance, but Large Power Dissipation.
- The Solution was to use the emerging CMOS Technologies
- So Particle Physics began to use Microelectronics
- The Big Question was how could this be Done and What Facilities would be Required?

In the Beginning (3)
- A Review of the Requirements for Electronics Facilities at CERN (Chaired by Chris Fabjan) recognized the growing Importance of Microelectronics to the Future of Particle Physics and Recommended the Establishment of a Properly Resourced Microelectronics Group at CERN
- Properly Resourced included having a Critical Mass of Trained Engineers, the Correct Balance of Design Tools, Technician Support, and Testing Facilities
- The CERN Group should act as a Centre for Particle Physics

In the Beginning (4)
- Which Design Tools should the Particle Physics Community invest in?
- At RAL we had bought one License for one of a New Generation of Design Tools from ‘SDA’ (Later ‘Cadence’)
- It was very good, but was very Expensive even with an Educational Discount (for the MSc Courses).
- RAL and CERN evaluated the software and agreed that we should use it for future Particle Physics Designs
- How could we obtain Affordable Access to the Design Tools?
In the Beginning (5)

• The Mandate of ‘Euro-Chip’ was to Train Electronics Engineers in Microelectronics.
• The EU Commission accepted that most of the Training would take place in University Departments, but also accepted that ‘Not for Profit’ Research Institutes had an important role in this Training Process.
• Hence it became possible for all European Universities and Particle Physics Institutions to gain access to the best available Design Tools through ‘Euro-Chip’ & Europractice.

In the Beginning (6)

• Today RAL supports the access to the best Microelectronics Tools to ~ 650 European Universities and ~ 100 Research Institutions within the Europractice Programme.
• In October 1990, at the Aachen Workshop to discuss the design of Future LHC Experiments there were two significant additional meetings:
  • The First Meeting of the Recently Establish DRDC
  • A Meeting to Establish the ‘Microelectronics User Group’

In the Beginning (7)

• The Microelectronics User Group became the Forum to discuss the best Design Techniques, the ‘State of the Art’ in Microelectronics Technologies and Testing Techniques.
• The use of Common Design Tools was important in the Transfer of Experiences and in Collaborative designs.
• Once Design had Started it was Important to Establish an Annual Workshop to Coordinate the Work of the Community and Encourage the Use of Common Solutions.
• Hence the LHC Electronics Workshops and TWEPP Started.

Lesson One from the LHC

• LHC Experiments would not have been possible without Access to Microelectronics Technology.
• Obtaining Affordable Access to the Technology and Tools Requires Continued Coordination and Collaboration.
• Future Particle Physics Experiments will Continue to Require Access to these Technologies and this will Require Continued Investment in both Engineers, Tools and Facilities.
• Without these Investments there will be No Future Particle Physics Experiments.

Microelectronics and Silicon Detectors (1)

• At the LEP Experiments, all Silicon Micro-Vertex Detectors used CMOS Technology which provided the required performance with the required Radiation Tolerance.
• The Initial Concerns in the Instrumentation of Silicon Detectors for LHC were the hostile Radiation Environment and the Minimization of the Power Dissipation.
• Fortunately, access to Radiation Tolerant Technology was becoming available from a number of Specialist Vendors.

Microelectronics and Silicon Detectors (2)

• It was clear that the Priority given to the Development of Radiation Tolerant Technologies would decrease with time.
• The LHC Electronics Board (LEB) encouraged an Investigation (PARAM) into the use of ‘Deep Sub-Micron’ (0.25μ or 250nm) CMOS Processes for LHC Applications. The LEB Recommended to the LHC that this Project be Approved.
• The LHC Experiments gained access to 0.25μ CMOS Technology with sufficient Radiation Tolerance and the Very Good Yield expected of a Modern High Volume Technology.
Microelectronics and Silicon Detectors (3)

• The Scale of LHC Silicon Tracking Detectors was larger than the LEP Detectors.
• This Required Much Larger Numbers of Chips (Factor ~100) and the Consequent increase in Quality Assurance (QA)
• Microelectronics had always required a Professional Engineering Approach to Ensure Success, This was now Mandatory, with Careful Reviews at Each Stage.
• With the Best Tools and Discipline the Particle Physics Community proved that it could Reach the Highest Standard

Scale of the CMS Tracker Project

• ~ 66,000,000 Pixels and 10,000,000 Silicon Strips
• ~ 16,000 Modules
• ~ 100,000 APV Chips, ~ 20,000 ROC Chips (250nm IBM CMOS)
• ~ 40,000 Optical Fibres
• ~ 500 FEDs (Front End Drivers (Off-Detector Data Receivers))
• ~ 2500 Power Supplies, ~ 2500 Power Cables
• ~ 450 Cooling Loops (Capable of Cooling Tracker to -30°C)
• ~ 540 Physicists and Engineers (54 Institutes in 10 Countries)

Time Scales Involved in the CMS Tracker Project

• Approval to Completion of Integration – 7 Years
• First Production Modules to Commissioned Tracker – 3 Years
• Strip Tracker Transport and Installation – 2 Days
• Strip Tracker Connection to Services – 3 Months
• Strip Tracker Commissioning to ~ 99% - 3 Months
• Pixel Tracker Transport and Installation – 1 Week
• Pixel Tracker Connection to Services – 1 Week
• Pixel Tracker Commissioning to ~ 99% - 3 Months

Microelectronics and Silicon Detectors (4)

• It was only Possible to use Reasonably Advanced Microelectronics Technology at the LHC because there was a Very Effective Infrastructure in Existence to provide Access to Design Tools, Design Kits and Libraries, and the CERN Managed MPW scheme that provided Affordable Access to Engineering Prototypes and a Single Interface to Industry
• The Partnership with IBM proved Absolutely Invaluable in Understanding the Solutions to the Complex Problems that always arise in Large and Complex Detector Systems.
Why go to more Advanced Microelectronics Technologies?
- The Drive for smaller feature size Microelectronics comes from the Commercial Requirements to obtain Greater Functionality at less Power for Large Volume Applications
- These are also the requirements of SLHC Applications
- Use ADCs to Compare Power Dissipation per Conversion
- Atlas Calorimeter 200K Channels, 16 bits at 40MHz
  - In 250 nm Technology 262 KW 1pJ/Conv
  - In 65 nm Technology 13 KW 50fJ/Conv

Microelectronics and Silicon Detectors (5)
- Fifteen Years Ago, Technologies were > 1μm and Wafers ≤ 6"
- In Future Technologies will be << 1μm and Wafers > 8"
- Hence the NRE costs will be much higher!!
- How do we maintain the same cost / chip as we have now?
- Limited Number of Design Iterations and > 100,000 Chips
- This will inevitably involve a small number of tightly coupled Design Centres with University Groups involved in both the Specification and Evaluation Phases

Lesson Two from the LHC
- The Engineering of Large and Complex Systems Requires a Very Disciplined and Professional Approach.
- Adoption of Formal QA Methods has enabled the Particle Physics Community to Achieve the Highest Standards in both System Performance and Number of Iterations.
- When Considering the Challenges of the SLHC, We should Consider whether we need to Further Improve our Techniques and Organization

Opto-Electronics Systems (1)
- There are a number of reasons for using Opto-electronics systems to Transport Data from the Detectors to the “Off-Detector” Electronic Systems
  - Electrical Isolation of the Detector from Counting Room
  - Potential for High Speed Data Transmission
  - Potential for both Digital and Analogue Data Transmission
- In the Beginning there was very little Experience in the Particle Physics Community and although there were Commercial Links there was still much R&D Activity

Opto-Electronics Systems (2)
- There was a DRDC R&D Project to evaluate the Options available and to provide a Focus for the Community
- It was Clear from the Outset that Power would be an Issue
- It was Clear from the Outset that Cost would be an Issue
- The CMS Tracker chose to use Analogue Links to provide more Diagnostic Information in Commissioning the System
- The Atlas Tracker chose a Binary Link System
- Both Detectors used Links for both Data and Control
Opto-Electronics Systems (3)

• Initially it was thought that the Cost would be Different
• The Final Costs were:
  - CMS: 42,800 Links Production Cost 294 CHF / Link
  - Atlas: 12,264 Links Production Cost 284 CHF / Link
• Considering that almost every aspect of these Systems were different this is an interesting Conclusion
• To Engineer Large Complex Systems it is Crucial to Establish a Excellent QA at every Stage of the Project

Opto-Electronics Systems (4)

• It is Crucial to Test at every Stage of Procurement, Assembly and System Commissioning
• It is Crucial to do Complete System Tests before the starting Production Procurement. Details Compromise Quality
• CMS Tracker: 0.04% Dead Links, 0.38% Problematic Links
• Atlas Tracker: 0.8% Dead Links, 0.6% Problematic Links
• The CMS Analogue Links required more QA from the Outset and this probably resulted in the Different Yields

Opto-Electronics Systems (5)

Lessons from the CMS Tracker Experience
• Avoid fibre pig-tails.
• Do not allow excessive fibre-slack without corresponding management scheme.
• Use Ruggedized ribbon/fibre only.
• Avoid simplified and/or compact connectors which are difficult to dismount and clean.
• Develop and distribute fibre-test tools which allow on-line testing, providing immediate channel quality feedback during construction.

Opto-Electronics Systems (6)

Lessons from the Atlas Tracker Experience
• Better ESD precaution
• More longer term testing of the VCSELs at an earlier stage in the assembly to weed out any damaged devices.
• Avoid all use of fragile single fibres on the detector.
• Always used balanced codes.
• Ensure that QA is performed for identical conditions to the final system.

Lesson Three from the LHC

• All of the Experience in Constructing and Commissioning and the Quality Assurance of the Opto-Electronics Systems for LHC must be Preserved
• Most of the ‘Know-how’ is stored in the Groups that have Successfully Engineered these Systems
• It is Crucial to Maintain a Critical Mass of Engineers with the Facilities and Equipment to ensure that the Present Systems Maintain their Performance and that the Engineering of Future Systems is Built on the Experience from the LHC Projects

Power Systems, Grounding and Shielding (1)

• Initially there was Concern that it would not be possible to Install the Power Systems in the LHC Caverns because of both the Radiation and the Magnetic Field Environments
• These are not Problems that Commercial Systems commonly encounter and Hence there were No Commercial Solutions
• The Alternative was to Place the Power Systems Outside the Caverns with the Additional Cost of Cables and the Increase in the Power Dissipation
Power Systems, Grounding and Shielding (2)

- There had also been a contraction in the Number of Companies providing Electronics for Particle Physics Applications.
- Development Projects were started with Two Companies (CAEN and Wiener) to Provide both Radiation and Magnetic Field Tolerant Power Systems.
- Both Projects were Successful and Provided the Range of Systems to meet the Requirements of the LHC Projects.
- However Most Power was Transmitted at Low Voltage (<3V) and Hence the Transmission Power Losses were Very Large.

Power Systems, Grounding and Shielding (3)

- Initially Compact Radiation Tolerant Voltage Regulators were Not Available. Hence the CMS Tracker did not have ‘On-Detector’ Voltage Regulation.
- A Very Successful Partnership with CAEN developed a Power System (including a Low Inductance Cable) that delivered both Low Voltage Power and the Bias for the Silicon Sensors without Introducing Transients at the Silicon Modules that could have damaged the Chips.
- An Extension of this System Development became a Standard Commercial Product Range.

Power Systems, Grounding and Shielding (4)

- It is Crucial to design a Complete System, which involves Power Supplies, Cables, Control and Safety Systems, and Grounding and Shielding Systems.
- In General this did Not Take Place at LHC.
- Initially a lot of Effort was absorbed in Engineering the Front-End Chips and Electronics Coordinators worked hard to bring Power, Grounding and Shielding Issues into Focus.
- On Occasion Schedule Pressure prevented the attention to the detail that would have improved noise immunity by orders of magnitude.

Power Systems, Grounding and Shielding (5)

- Fortunately, Good Engineering at the Integration Stage Reduced the Grounding & Shielding Issues to a Manageable Level and so far there have been no Show Stoppers.
- In General the Particle Physics Community is not well Equipped to Diagnose and Solve Grounding and Shielding Problems.
- Since the Power Systems are in the Experimental Caverns, System Reliability is an Important Issue. It has been important to ‘Burn In’ the Power Systems before Installation in the Experiments, and to Log and Follow up all Problems.

Lesson Four from the LHC

- It is Important to Design Complete Power Systems From the Start, which involves Power Supplies, Cables, Control and Safety Systems, and Grounding and Shielding Systems.
- Solving Problems is always Easier, and Usually Cheaper at an Earlier Stage of the Project.
- It is Crucial to Maintain a Critical Mass of Engineers with the Facilities and Equipment to ensure that the Present Systems Maintain their Performance and that the Engineering of Future Systems is Built on the Experience from the LHC Projects.

Off-Detector Electronics Systems (1)

- The Engineering of the ‘Off-Detector’ Electronics Systems has been dominated by the Development of FPGA Technology.
- Early Developments of some Systems fixed the Technology before FPGA Technology was Available, Other Systems Adapted to the New Technologies.
- Large Systems with many FPGAs Need Very Careful Engineering to Delivery High Yield, Highly Reliable Systems.
Off-Detector Electronics Systems (2)

• The Issues with FPGAs is that Many People can write the Firmware required to programme an FPGA, but Not Many People can Engineer a Reliable System that is Easy to Commission and Maintain.
• Other Issues are Obsolescence of both Hardware and Software and the Version Control of the Firmware
• Again QA and Attention to Detail in the layout of Large Multi-Layer Circuit Boards are Essential

Off-Detector Electronics Systems (3)

• A Example of Good Practice is the Front-End Driver System for the CMS Tracker.
• It involves 500 9U Boards (See next Slide)
• The Fabrication Company was Chosen with Care
• 99% of the Boards worked on Receipt from the Fabrication Company, who were also responsible for Board Fabrication & Board Testing, with Test Equipment supplied by the User
• The System was Easy to Commission and has proved to be Very Reliable

Off-Detector Electronics Systems (4)

• The Issues are by now Very Familiar:
  • Careful Systems Design
  • Careful Tuning and Reviews of the Specifications
  • Professional Design Teams for Hardware, Firmware and Software, Commissioning and Maintenance Systems
  • Careful Preparation of Commissioning and Performance Evaluation
  • A QA System that promotes Continuous Improvements

Lesson Five from the LHC

• Large Complex Systems Can only be Efficiently Commissioned and Maintained if Best Engineering Practice has been followed throughout the Design of the System
• Too Often Gifted Individuals become Single Point Failures
• LHC Systems have to be Maintained for ~ 10 years well beyond the Commitment of Individuals
• Hence it is the Institutions that must Underwrite the Commitment to Maintain the Systems for the Life of LHC
• It is the Institutions that must maintain the Engineering Infrastructure that Guarantees the Long Term Commitment

Summary (1)

• The Problems faced in the Engineering of the Electronics Systems have been Significantly Larger and More Complex than any Previous Particle Physics Projects
• Success has only been Possible by Merging Many Gifted Individuals with an Engineering Structure that has Provided the Environment in which the most Creative Ideas could be Transformed into Reliable and Maintainable Systems
• Summary (2)
  • It is Important that we recognize what has worked well and what is required to Maintain the Improvement
  • Coordination, Collaboration and the Search for Common Solutions to avoid Duplication have been Very Important
  • We should Continuously Review our Organization and Adapt to Changes in both Requirements and Technologies
  • We must Maintain a Critical Mass of Engineers with the Facilities and Equipment to Build on the Experience of LHC

• Summary (3)
  • In General our Approach to System Design could be Improved. It is Very Difficult to Control the System Design without having Control of the Budget. Hence the Method of Funding LHC Projects has made this more Difficult
  • Formal QA Systems need to be Adapted to the Particle Physics Environment. In Many Projects, more in-depth Reviews would have found Problems much Earlier and Hence saved both Time and Money

Conclusions
• The LHC Electronics Systems have been Very Successful and the Community should Reflect with Pride at this Massive Achievement
• Many of the Organizations Establish at the Beginning of the Projects Worked Well. New Working Groups Work Well
• We need to Build on these Experiences and Ensure that we have a Strong Community to take on the Challenges of SLHC

Electronics at SLHC

An Optimistic Plan for LHC Luminosity
Some of the Issues for Electronics at SLHC

- Which Microelectronics Technology Should we Use?
- Do we have the right Organization in Place to Obtain Cost Effective Access to Advanced Technologies?
- Which Interconnection Technologies Should we Use?
- Will we have Access to Cost Effective Optical Links?
- Can we Transmit Power to the Detector at High Voltage and obtain Efficient Conversion to Low Voltage at the Detector?
- How will Future Off-Detector Systems Evolve?
- How do we Establish Effective Partnerships with Industry?

Thank You
THURSDAY 18 SEPTEMBER 2008

POSTERS SESSION
Implementation of the Control and supervision of ALICE ZDC positioning Systems-
TWEEP-08

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Abstract

The ALICE Zero Degree Calorimeters (ZDC) have been installed to either side of the LHC IP2 in the machine tunnel next to the dipole magnet D2. The calorimeter modules are mounted on a special table equipped with a mechanism to lower the modules away from the beam orbit during injection and acceleration. During stable operation the modules can be raised individually to be aligned with the beam orbit. The horizontal clearance between ZDC modules and beam pipe will be only about 3 mm. Anti-collision switches are therefore installed to protect the beam pipes against accidental damage. The movement of the calorimeter modules and the protection switches are remote controlled by the ALICE ZDC positioning system.

I. INTRODUCTION

The ALICE Zero Degree Calorimeters (ZDC) are installed to either side of the LHC IP2 in the machine tunnel next to the dipole magnet D2 \cite{1}. The calorimeter modules are mounted on a special table equipped with a mechanism to lower the modules away from the beam orbit during injection and acceleration (Figure 1) \cite{2}.

During stable operation each calorimeter module can be raised individually and centered position. The horizontal clearance between ZDC modules and beam pipe will be only about 3 mm (Figure 1).

Anti-collision switches are therefore installed to protect the beam pipes against accidental damage.

The movement of the calorimeter modules and the protection switches are remote controlled by the ALICE ZDC positioning system. The architecture of the control system is based on a Programmable Logic Controller (PLC) which connects to the local servo-controllers via a field bus. Two application interfaces have been created; one using Labview\textsuperscript{®} for the development and maintenance and the 2\textsuperscript{nd} in the SCADA \cite{3} framework for the detector control system. The layout and the implemented controls algorithms are explained.

II. ACRONYMS

ALICE A Large Ion Collider Experiment
DCS Detector Control System
DSS Detector Safety System
IP2 Intersection Point 2
JCOP Joint Controls Project
LHC Large Hadron Collider at CERN
LVDT Linear Voltage Direct Transformer
MMI Man Machine Interface
PLC Programmable Logic Controller
SCADA Supervisory Control and Data Acquisition
ZDC Zero Degree Calorimeter

III. OVERVIEW OF THE SYSTEM

The general concept of the controls system follows a 3 layer architecture (Figure 3). The hardwired sensor and actuator level is connected to the device control and data acquisition layer which includes servo-controllers and PLC. The SCADA level communicates with the PLC through industrial Ethernet.

Signal flow and interlock chain are shown in the diagram (Figure 4) for one calorimeter. The acquisition of the value of the LVDT is done directly via an analog input channel of the servo-controller. All interlock switches are also cabled to the servo-controller.
IV. POSITIONING SYSTEMS CONTROL

The vertical movement to approach or retract each of the ZDC with respect to the recombination beam pipes is controlled by one dedicated PLC which acts on a servo-controller for each of the four calorimeter modules.

The control functions can be separated in process control functions and supervisory control functions. They later run in the PLC and partially in the Detector Control System (DCS) of the ALICE experiment [4] which also provides the standard MMI for the operation of the positioning system. The process control functions are shared between PLC and the servocontrollers.

A. Process Control

The PLC monitors the position of the calorimeters and controls the movement of the servo-motors which is hard limited by a number of the interlock switches.

The main actions and status of the system are:

- on/off: PLC active or disabled
- stop: interrupt any active command and halt servo-motor
- garage position: when normally all calorimeters are retracted
- hold: calorimeter in position outside garage position
- run: calorimeter changes position
- limit detection (calorimeter at end stop, limit switch or anti-collision switch)

The PLC monitors and registers the complete installation: physical parameters (position, speed, direction, etc.) and status (operation mode, on-off, warnings, alarms, etc.).

B. Movement control

The vertical position of each calorimeter is permanently monitored by an LVDT. This value is received by the dedicated servo-controller which converts the value to internal coordinates by applying a transfer function of format:

$$V_{pos}(Zxy) = V_{request}(Zxy) + V_{LVDT}(Zxy)$$

The result is converted by the PLC into physical coordinates.

In order to change the position of a calorimeter the supervisory system needs to send first the new set point value to the PLC and then the go command. This causes an activation of the corresponding servo-drive until one of the following conditions becomes true:

- $$V_{pos}(Zxy) = V_{request}(Zxy)$$ or
- Alarm (Zxy); i.e. an exception condition has been detected or
- PLC receives a new command which supersedes the previous command.

In order to avoid any hysteresis due to mechanical tolerances of the drive gear the control algorithm is constructed such as to reach the requested position always by a movement against gravity.

C. Movement limits and LHC interlocks

The movement of each of the calorimeters is constraint by limit switches and mechanical stops. The limit switches act directly on the servo-controllers and stop the motors. The mechanical stops act as an ultimate emergency device preventing any further motion and eventually causing a power interruption by a motor protection function in the servo-controller.

It is not foreseen to provide programmable range limits in the PLC. These thresholds can be better integrated in the supervisory system where they can easily be changed on the fly.

The ZDC station which is located just downstream of the beam injection area for beam 1 of the LHC is directly exposed to miss-injected beam. The position of the calorimeter modules of this station is therefore interlocked with the LHC Beam Interlock System (BIS) during injection. A current loop output of the servo-controllers is used to generate the “beam permit flag” signal as long as the calorimeter modules are in the out position which is detected by an end switch. Outside injection periods the flag has no effect. During injection mode the absence of the flag will prevent through the hardware beam injection inhibit system any injection of beam 1 into the LHC ring. The request for two independent signal sources for this flag has been implemented by feeding the output from each calorimeter to a different channel. Consequently, the injection permit will only be true if both calorimeters are in the garage position.
D. Recovery

Each of the described exception conditions aborts the received movement command and the calorimeter stops immediately. However, a command to move in the reverse direction will still be accepted by the controls system.

In case of a hardware failure a remote reset will not be possible.

E. Movement calibration

The absolute position of each of the calorimeters can be calibrated during an initialization run. The device needs to be moved previously into a defined position; i.e. the lower mechanical stop. The measured value from the LVDT is then stored in the servo-controller as permanent offset.

V. LOCAL SUPERVISION

A local/remote switch mounted at the electronics rack in the LHC tunnel allows switching to local control of the ZDC positioning system. In this mode the PLC will accept commands for the servo-controllers concerned only and ignore other sources like the supervisory system of the DCS. The access to all the control functions of the graphical interface are password protected.

VI. NETWORK CONNECTIONS

The ALICE ZDC position system is controlled from one single PLC Siemens S7-300, CPU 315T-2 DP located in one of the ALICE counting rooms in the PX24 shaft. The concentrator PLC is connected to the internal ALICE network (industrial Ethernet) available in the experimental and service cavern.

A direct connection with the Detector Safety System (DSS) is not implemented. All interlock switches act directly on the servo-controllers which are located in the electronic racks in the LHC service tunnel close to the detector stations.

VII. DATA TRANSMISSION

Communication with the ALICE DCS is implemented following the standards of the JCOP framework [5]. This PLC communicates with the ALICE DCS system over TCP/IP. The PLC can be accessed through the dedicated OPC server or using the native driver in the PVSSII supervisory system running on Windows OS or Linux OS.

Data exchange between PLC and the front-end instrumentation has been implemented over Profibus using the Profinet protocol suite. The integration of the servo-controllers required the use of the “technology function blocks” which are tailored for these instruments. This, however, limits the optimization of the FSM and the robustness of the transmission since the use of the preconfigured function blocks does not allow to adapt the transfer function between position measurement from an external instrument (LVDT) and the response of the servo-controller. Therefore, the integrated resolver of the servomotor had to be used for the real-time feedback to the servo-controller. In a second step the measured position is compared to the set point followed by a new iteration loop in case of a difference.

The use of the technology functions restricts the communication over the Profibus to synchronous transmission mode which implies short latency for the data exchange between master and slave stations and therefore relatively high transmission speeds of 6 MB/s in our case. This reduces, however, the acceptable bus segment length dramatically. In order to cover the required distance of about 500 m between stations specific Profibus RS 485 repeaters have been added at each station.

VIII. CONTROLS OPERATOR INTERFACE

A. Experiment Control Room ECR

In normal operation the ECR authorised operators can position each calorimeter individually within a preset range. The validity of the command is checked inside DCS with respect to the LHC operation mode. Only requests to change which have been validated by the DCS are transmitted to the ZDC control PLC.

The PLC application executes the command if no exception condition exists either in the PLC itself or in the front-end instrumentation.

On reception of an operator request the PLC application returns an acknowledgement. If an exception condition is detected an alarm status is returned. In this case the detailed status is returned to the supervisory system on request.

B. Local/Remote

This feature allows a direct intervention on the device and shall prevent any accidental remote activation. In local mode the positioning system will not accept any commands from the ALICE DCS but exclusively from a dedicated computer with the native Siemens software and the Labview interface.

The full controls functionality is also made available in local mode. The hardware interlocks remain active under all conditions.

IX. PARAMETERS AND VARIABLES

The following table shows the parameters and variables which are available at the interface between PLC and DCS.
### Table 1: ZDC positioning system parameters and variables

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Source</th>
<th>Dest.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Go</td>
<td>Start movement to set point</td>
<td>Scada</td>
<td>PLC</td>
</tr>
<tr>
<td>Stop</td>
<td>Stop movement immediately</td>
<td>Scada</td>
<td>PLC</td>
</tr>
<tr>
<td>Setpoint</td>
<td>Requested position (absolute physical coordinate)</td>
<td>Scada</td>
<td>PLC</td>
</tr>
<tr>
<td>Measurement</td>
<td>Actual value of the position of the calorimeter (absolute physical coordinate)</td>
<td>PLC</td>
<td>Scada</td>
</tr>
<tr>
<td>StationActive</td>
<td>Status of drive electronics</td>
<td>PLC</td>
<td>Scada</td>
</tr>
<tr>
<td>Error</td>
<td>Fault condition</td>
<td>PLC</td>
<td>Scada</td>
</tr>
<tr>
<td>InPosition</td>
<td>Actual position is equal to set point</td>
<td>PLC</td>
<td>Scada</td>
</tr>
<tr>
<td>IGP</td>
<td>Actual position is equal to garage position</td>
<td>PLC</td>
<td>Scada</td>
</tr>
<tr>
<td>ABI</td>
<td>LHC hardware injection permit raised</td>
<td>PLC</td>
<td>Scada</td>
</tr>
<tr>
<td>LOC</td>
<td>Remote / local status indication</td>
<td>PLC</td>
<td>Scada</td>
</tr>
<tr>
<td>CIL</td>
<td>Protection cover open</td>
<td>PLC</td>
<td>Scada</td>
</tr>
<tr>
<td>HES</td>
<td>Upper end switch reached</td>
<td>PLC</td>
<td>Scada</td>
</tr>
<tr>
<td>LPC</td>
<td>Lower end switch reached</td>
<td>PLC</td>
<td>Scada</td>
</tr>
</tbody>
</table>

### X. COMMISSIONING

The commissioning of the system has been performed in two stages. In a 1st period the complete ZDC system was assembled and tested in a surface hall. A full implementation of the control system was developed in parallel. Tests included the remote control of the movement, end switch interlock, remote and local command functions. A stand alone application was developed with Labview in order to have a comfortable tool to test the entire functionality and as debugging tool. This application will also be used later during operation and maintenance in local mode. At the same time the implementation of the SCADA application with the final MMI was also developed and tested.

After installation of the complete detector including support structure in the final position in the tunnel a full test sequence has been performed with the remote control application and in local mode. This included the test of all safety and limit switches as well as the injection inhibit interlock.

### XI. REFERENCES

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High-Resolution Time-to-Digital Converter in Field Programmable Gate Array

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Abstract

Two high-resolution time-interval measuring systems implemented in a SRAM-based FPGA device are presented. The two methods ought to be used for time interpolation within the system clock cycle. We designed and built a PCB hosting a Virtex-5 Xilinx FPGA. We exploited high stability oscillators to test the two different architectures. In the first method, dedicated carry lines are used to perform fine time measurement, while in the second one a differential tapped delay line is used. In this paper we compare the two architectures and show their performance in terms of stability and resolution.

I. INTRODUCTION

High-resolution Time-to-Digital Converters are often required in many applications in high-energy and nuclear physics. Furthermore, they are widely used in many scientific equipments such as Time-Of-Flight (TOF) spectrometers and distance measurements. Different configurations of tapped delay lines are widely used to measure sub-nanosecond time intervals both in ASIC and FPGA devices. However, the design process of an ASIC device can be expensive, especially if produced in small quantities, while FPGAs lower the development cost and offer more design flexibility. In 1997, Kalisz et al. [1] proposed an FPGA-based approach: their design used a variation of conventional delay line and offered a time resolution of 200 ps. In 2000 [2], rapid progress in electronics technology allowed them to achieve a time resolution of 100 ps. Resolution values between 50 ps and 500 ps have been achieved with this technology [3]. Two different digital delay line circuits have been designed and tested by the authors thus far [4].

II. PRINCIPAL OF OPERATION

We have designed two types of TDC architectures in the newest available Xilinx Virtex-5 FPGA [5]. Both approaches use the classic Nutt method [6] based on the two stage interpolation. The timing acquisition process consists of three phases shown in Fig.1. First, the time interval $\Delta t_1$ between the rising edges of the START signal and the subsequent reference clock edge is measured. Then, a coarse counter measures the time interval $\Delta t_{12}$ between the two rising edges of the reference clock immediately following the START and the STOP signals. The same procedure is exploited to measure the time interval $\Delta t_2$ between the rising edges of the STOP signal and the subsequent reference clock. The time interval between the START and STOP signals, $\Delta t$, is: $\Delta t = \Delta t_1 + \Delta t_{12} - \Delta t_2$. The fine conversion dynamic ranges $\Delta t_1$ and $\Delta t_2$ are limited to only one reference clock cycle. The simplified circuit block diagram of the TDC architecture is shown in Fig.2. The external clock frequency we used was 550 MHz. The Virtex-5 Digital Clock Managers (DCMs) provide a wide range of clock management features and allow phase shifting. We used one DCM that gives four copies of the same clock signal shifted by 0°, 90°, 180° and 270°. In our work, the coarse TDC is designed around a free running 550 MHz synchronous counter. The coarse counter does not allow us to measure $\Delta t_1$ and $\Delta t_2$ as shown in Fig. 1. Their measurement has been obtained using the same fine time converter for both $\Delta t_1$ and $\Delta t_2$. We designed two different fine time converters. The first one consists of tapped delay lines, while the second one uses Vernier delay lines. In order to test the two different TDC architectures, we designed and built a PCB hosting a Virtex-5 FPGA from Xilinx, which is shown in Fig.3. Two high stability oscillators from Valpey-Fisher have been installed in order to compare their performance side by side. Test points for high-bandwidth active probes are used to perform the Virtex-5 clock signal characterization. They are placed just near the FPGA, making the shortest distance for the device output signals. SMA connectors are used to send the START and STOP signals to the board. They may adopt differential lines or single ended signaling schemes.

![Figure 1: Measurement of time interval T with the Nutt method](image-url)
A. Time counter

The coarse time measurement is realized by the coarse TDC. The building blocks of the coarse TDC are the 550 MHz synchronous counter and the finite state machine. The counter has a 16 bit data width and is used in free-running mode. When the START signal transition occurs the current state of the counter is sampled by the START register, and the same operation occurs also when the STOP signal is delivered to the TDC.

The difference between the STOP and START register is the coarse measurement of the time interval. The state machine is needed to achieve a better resolution of the time interval measurement. It samples the start and stop signals and detects the phase difference between the start and stop rising edges. The least significant bit corresponds to a quarter clock period. The full clock period is recovered by the 2 bit counter \( N_{c[1:0]} \) which labels the phase value.
The output binary value $N_c[1:0]$ increases the data out width of the coarse TDC, $N_c$ which is a 18 bit wide word. Therefore the state machine allows us to obtain a coarse resolution of quarter of the CLK0 period (454 ps). Furthermore, it is useful to the delay line selection of the fine TDC performed in the carry chain delay line architecture. The sel0/1 output bits, shown in Fig. 2, follow the phase difference between the START/STOP and the CLK0 signal. This value is 0 if the phase difference is lower than $\pi$, 1 if it is bigger. The selection of the tapped delay line of the fine time measurements reflects the phase difference between the START/STOP signal and CLK0. The measurement range of the coarse TDC is limited due to the counter width and the resolution is limited due to the clock frequency.

**Figure 4:** Carry chain delay line. Left: logic block diagram. Right: layout obtained using a Xilinx Virtex-5 FPGA

**Figure 5:** Simplified block diagram of the Virtex-5 slice

**B. Carry chain delay line**

In the FPGAs available today, there are high-speed chain structures that vendors designed for general-purpose applications. A few well-known examples are carry chains, cascade chains, sum-of-products chains, etc. These chain structures provide short predefined routes between identical logic elements. They are ideal for TDC delay chain implementation. The first architecture, shown in Fig.4 (left) uses carry chain delays. In this configuration the STOP signal is the 550 MHz system clock. The START signal after each delay unit is sampled by the corresponding flip-flop on the rising edge of the STOP signal. The tapped delay line layout is presented in Fig.4 (right) while in Fig.5 a simplified block diagram of the Virtex-5 slice is shown. In this configuration the delay line is created by a train of 64 multiplexers. The selection bit of every multiplexer is set to logic one, in order to let the START signal propagate through the line. The time quantization step of the TDC is determined by the multiplexers propagation delay $\tau$. Due to the short delay of the tapped delay line, it’s necessary to use two delay lines in order to cover the duration of a clock period. The first line is clocked by CLK0 and the second line by CLK180. The state machine decides which line is selected by setting the sel0/1 line to 0 or 1 logic level. We used the multiplexing of two delay lines rather than a longer line, to reduce the possible non linearity introduced by the clock distribution delay time between neighboring slices. Furthermore in this way, the output from the tapped line is more easily converted from thermometric code into binary natural code by using a priority encoder.

**Figure 6:** Vernier delay line: logic block diagram

**Figure 7:** Layout of the Vernier delay line obtained using a Xilinx Virtex-5 FPGA
C. Vernier delay line

The second architecture, shown in Fig.6, consists of two tapped rows working in differential mode. The first is created as a chain of the latch flip-flops L1, L2, ..., L63 and the other as a chain of noninverting buffers B1, B2, ..., B63. Hence the basic delay cell contains one latch having the delay \( \tau_1 \) and one buffer having the delay \( \tau_2 \). If the latch delay is longer than the buffer one, the time quantization step of the TDC is determined by their difference \( \tau_1 - \tau_2 \). An advantage of that direct coding is very short conversion time and very short dead time equal to the readout time of the output time. The time to be measured is defined between the rising edges of the pulses START and STOP. During the time-to-digital conversion process, the STOP pulse follows the START pulse along the line and all latches from the first cell up to the cell where the START pulse overtakes the STOP pulse are consecutively set. In the used configuration, the output from the tapped line is obtained in thermometric code and then converted into binary natural code. This is been possible thanks to an array of priority encoder realized on the FPGA. In this approach, the reset input signal is given to all latches contemporaneous only after the end of the acquisition time. As it is known, the current FPGA technologies offer logic cells to implement logic defined by the user and in particular the delay cell of the TDC. Fig.7 shows the layout of the Vernier delay line realized using the Virtex-5 slices.

To implement the design in FPGA, one must address one major problem: in the FPGA development software, a logic element (combinatorial or sequential) can be physically placed in nearly any place, depending on the optimization algorithm used. When left up to the program, routing between logic elements may also be unpredictable to the user. If the logic elements used for the architectures are placed and routed in this fashion, the propagation delay of each delay step will not be uniform. To avoid this, the designer is forced to place and route the logical resources by hand.

III. TEST BENCH

Preliminary tests have been made on our delay lines using the two architectures on the TDC Tester board. Each TDC structure has 64 steps. To execute our tests we have used an architecture based on an embedded microprocessor, as shown in Fig. 8.

Figure 8: Communication between PicoBlaze and the TDC delay line

PicoBlaze [7] is a FPGA based microprocessor which has an 8-bit address and data ports to access a wide range of peripherals. The PicoBlaze firmware allows the user to enter a delay value via a RS232 link. The intermediate stage receives data bus, decodes it and establishes which is the value delay. Each signal is connected to the respective carry. In this way arrival time (STOP) is changed by using carry of various lengths. Carry chain has been used to generate the delays because for each step they can be considered fixed for the particular physical technology, rail voltage and temperature range.

IV. TEST RESULTS

The time interval between START and STOP has been calibrated and then it is measured by TDC. Fig. 9 show a test result of the two architecture TDC outputs as a function of the signal input time. More than 1000 measurements were made for each point and the average of each set of measurements was plotted. In Fig. 9 a linear fit, to guide the eye, is superimposed on experimental data. Comparable resolution, of about 80 ps have been measured for the two different delay line designs. Some non-uniformity are due to the internal layout structure of the device.

![Figure 9: TDC output as function of the input time delay. Top: implementation of the carry delay line. Bottom: implementation of the Vernier delay line.](image)

V. CONCLUSION

Semiconductor devices are becoming faster and faster. This allows us to have high resolution digital counter and short delay elements. Therefore, it is possible to develop a low cost and high resolution TDC exploiting FPGAs based techniques. By using SRAM-based FPGAs, the user benefits from the in-system-programming (ISP) and reconfiguration
features increasing the flexibility and reliability of the measuring system. Resolution values of about 80 ps have been achieved.

VI. REFERENCES


ATLAS TDAQ Integration and Commissioning

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Abstract

The ATLAS detector will be exposed to proton proton collision at the center of mass energy of 14 TeV with the bunch crossing rate of 40 MHz. In order to reduce this rate down to the level at which only interesting events will be fully reconstructed, a three-level trigger system has been designed. The level 1 trigger reduces the rate down to 75 kHz via the custom-built electronics. The Region of Interest Builder delivers the Region of Interest records to the level 2 trigger which runs the selection algorithms with the commodity processors and brings the rate further down to \(3\) kHz. Finally the Event Filter reduces the rate down to \(\sim 200\) Hz for permanent storage. The subsystems will be reviewed. The commissioning in situ using detectors, the full trigger system and the DAQ system will be discussed. Results on system functionality and performance based on the cosmic data will be presented. Some studies on system scalability and reliability will be shown with preselected simulated events running through the trigger and dataflow system.

I. ATLAS TDAQ SYSTEM

The ATLAS detector \cite{1} is designed to study the proton proton collision at the Large Hadron Collider (LHC), at the center of mass energy of 14 TeV with the bunch crossing rate of 40 MHz. In order to fulfill the physics goals, the ATLAS detector is instrumented with the magnet system, the inner detector system, the calorimetry system, the muon system and several forward detectors. The magnet configuration consists a superconducting solenoid and three large superconducting toroids. The inner detector system combines the high resolution semiconductor pixel detector, strip detector and the straw tube tracking detector. The calorimetry system has the high granularity liquid argon electromagnetic sampling calorimeter and the scintillator tile hadronic calorimeter. The muon spectrometer includes high precision tracking chambers and trigger chambers. Forward detectors are mainly used to determine the luminosity.

The trigger/data acquisition (TDAQ) system will have to handle the extremely high data rates (Figure 1). The level 1 (LVL1) trigger reduces the rate down to 75 kHz via the custom-built electronics. The Region of Interest Builder (RoIB) delivers the Region of Interest (RoI) records to the level 2 (LVL2) trigger which brings the rate further down to \(\sim 3\) kHz, at which events will be fully built. Finally the Event Filter (EF) reduces the rate down to 200 Hz for permanent storage. Both LVL2 and EF, together High Level Trigger (HLT), run selection algorithms with the commodity processors.

II. LVL1

The ATLAS LVL1 system \cite{2} consists of three components, the Calorimeter Trigger (L1Calo), the Muon Trigger (L1Mu) and the Central Trigger (Figure 2). The Central Trigger includes the Central Trigger Processor (CTP) and the Muon-to-CTP-Interface (MUCTPI). The L1Calo system forms electron/photon, tau/hadron, and jet multiplicities as well as global event energy information. The MUCTPI obtains muon candidate information from the L1Mu system which includes the barrel (RPC) and endcap (TGC) muon trigger chambers, then produces muon multiplicities for six configurable transverse momentum thresholds. Based on these local trigger objects the CTP makes the trigger decision with a configurable trigger menu. The trigger decision, together with the clock and other signals, is distributed to the detector front end and readout systems via the Timing, Trigger and Control (TTC) system. Some LVL1 components are shown in Figure 3.
While deploying functionalities and improving performance with standalone tests, the LVL1 system joins combined runs with detectors for integration and cosmic data taking, more frequently L1Mu with RPC, TGC and monitored drift tube (MDT) chambers, L1Calo with the liquid argon calorimeter (LAr) and the tile calorimeter (TIL), sometimes all possible systems together. The focus of the combined runs has been turning from problem finding to combined studies. Figure 4 shows some results from the combined runs.

III. HLT

HLT algorithms are executed based on trigger chains and chains are activated based on result of previous level. Each chain is divided in steps and each step executes an algorithm sequence (one or more algorithms). A step failed to produce an expected result ends the chain and any chain can pass the event. The LVL2 algorithms are seeded by the RoI information identified at LVL1 while the EF ones access the full event [3].

The LHC startup luminosity is expected to be $10^{31} \text{cm}^{-2}\text{s}^{-1}$ with less bunches. The initial ATLAS data taking under this condition will focus on commissioning the trigger and detector systems, and studying the basic Standard Model physics signatures. A trigger menu ($10^{31}$ menu) is being deployed for this running phase, by applying low thresholds, loose selections and pass-through mode wherever possible. The $10^{31}$ menu has been continuously exercised in the final TDAQ infrastructure with the simulated data. Figure 5 shows the LVL2 processing time and EF processing time for accepted events.
IV. DATAFLOW SYSTEM

Figure 6 illustrates the baseline of the dataflow architecture [3]. Data fragments of LVL1 accepted events from the detector front readout are transferred to the Read Out Systems (ROSes), each contains several Read Out Buffers (ROBs). Based on RoI records assembled by LVL2 supervisors (L2SVs) from RoIB, L2PU request data fragments from selected ROBs and send output to the LVL2 result handler (pROS). Data fragments for LVL2 accepted events are then built, on the initiation of the Data Flow Manager (DFM), from the ROSes, across a switched Ethernet network, into a complete event by one of the event building nodes (SFIs). The SFIs then send the complete events to the Event Filter nodes (EFD/PT). Events passed the EF are sent to the local data storage (SFO) before transferred to permanent storage for offline reconstruction. Most of the element interconnection in the Dataflow system is performed with the standard Gigabit Ethernet network and switching technology.

A large fraction of the dataflow system has been installed and commissioned. Some components are shown in Figure 7. The system is kept operational 24/7 for performance study and detector commissioning. Stability and scalability have been improved significantly. A typical test of $10^{31}$ menu with the simulated data in a system including 136 ROSes, 4 L2SVs, 94 SFIs and 600 HLT nodes shows that the installed system is adequate for data taking in the early phase (Figure 8).

V. COSMIC RUN

The full trigger chain, including MUCTPI, CTP, RoIB and LVL2, was tested at the first time in Feb 2007. A trigger rate of 30 Hz at LVL1 for cosmic rays was achieved with partial RPC detector. Downward muons were selected with LVL2 algorithms and accepted events were built then stored with a Small event building system. Figure 9 shows the $\eta$ and $\phi$ distribution of the cosmic tracks.
Since then the TDAQ system has been continuously running to take cosmic data, with the detector coverage gradually increasing (Figure 10).

VI. Trigger Strategy for Startup

The TDAQ system, together with almost full detector, is ready for the LHC beam. With the beam condition changing from cosmic, to single beam, to proton proton collision, different date samples will be used for LVL1 to perform timing calibration, energy calibration, logic verification and efficiency study. A few iterations will be needed before the stable triggering can be achieved. HLT will be studied under condition with colliding beams and stable detector operating.

Beam pickups (BPTX) are installed on both sides of ATLAS. Minimum bias trigger scintillators (MBTS) are installed on the LAr cryostat, with 16 modules each side. Loose coincidence logic with BPTX, MBTS (and beam position monitor) will be used for early data taking to trigger any activity in the detector. MBTS provide the triggers while BPTX sets the precise timing. HLT will run in pass-through mode as much as possible. On September 10, 2008, the first beam was seen by the ATLAS detector (Figure 11).

REFERENCES


Electronics of LHCb calorimeter monitoring system
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Abstract
All calorimeter sub-detectors in LHCb, the Scintillator Pad Detector (SPD), the Preshower detector (PS), the Electromagnetic Calorimeter (ECAL) and the Hadron Calorimeter (HCAL) are equipped with the Hamamatsu photomultiplier tubes (PMT) as devices for light to electrical signal conversion [1]. The PMT gain behaviour is not stable in a time, due to changes in the load current and due to ageing.

The calorimeter light emitting diode (LED) monitoring system has been developed to monitor the PMT gain over time during data taking. Furthermore the system will play an important role during the detector commissioning and during LHC machine stops, in order to perform tests of the PMTs, cables and FE boards and measurements of relative time alignment.

The aim of the paper is to describe the LED monitoring system architecture, some technical details of the electronics implementation based on radiation tolerant components and to summarize the system performance.

I. INTRODUCTION
The main aim of the calorimeter light emitting diode (LED) monitoring system is to monitor the PMT gain in time of data taking. The other important role of the system will be during the detector commissioning and testing in the LHC machine stops for PMT, cables and FE board tests and relative time alignment.

Each LED of the system illuminates up to 40 tubes and total amount of the monitoring channels is about 700.

The LED monitoring system consists of three functional parts:

- Subsystem for a LED intensity control for variation of the LED intensity across a wide range includes 40 boards.
- 12 9U –VME boards for a LED triggering pulse control and distribution placed into the front-end crates.
- 700 of the LED drivers with LV power distribution.

Sketch of the ECAL and HCAL LED monitoring signal chain is shown on the Figure 1.

II. CALORIMETERS PHOTO-DETECTORS AND LED MONITORING OPTICS
All calorimeters are equipped with Hamamatsu photo tubes as devices for light to signal conversion. Eight thousand R7899-20 tubes [2] are used for the electromagnetic and hadronic calorimeters and two hundred 64 channels multi-anode R7600 -00-M64 for Scintillator-Pad/Preshower detectors.

R7899-20 tube has the following characteristics:
- Dimension: 25 mm Diameter, 81 mm Length
- Spectral Response: 185 to 650 nm
- Photocathode: Bialkali, effective area 20 mm dia.
- Window material: UV glass
- Number of dynodes: 10
- Supply voltage: 1800 V max
- Average Anode Current: 0.1 mA max
- Quantum Efficiency: 15 % at 520 nm
- Current Amplification: 106
- Dark Current: 2.5 nA
- Time Response: 2.4 ns
- Pulse Linearity: +/- 2 %
Each LED of the system illuminates up to 40 tubes. The light is distributed to a PMT light mixer by clear fiber. HCAL light distribution schema is shown on Figure 2.

For LED light stability monitoring the PIN diode is used. The PIN diode signal after amplification is sent to the FE electronics board.

III. ELECTRONICS OF LED MONITORING SYSTEM

A. LED driver and intensity control board

Designed LED driver produce the LED signals in a wide intensity range with pulse shape similar the particle response.

Design peculiarities:
1) Edge triggering circuit with fast pulse shaper on the board;
2) Decoupling by air transformer.

LED driver simplified circuit diagram is shown on Figure 3 and the signal shapes oscillogram for PMT response on 50 Gev particle and LED signal are shown on Figure 4 and 5.

LED intensity signals are produced by the electronics board common with HV system. The LED intensity signal distribution board consists of the mother card and four types of the mezzanine board:
- SPECS slave for interconnection with the LHCb ECS system.
- Control Logic board for interface between the SPECS slave and others functional parts of Distribution board.
- HV control signal generation mezzanine.
- LED control signal generation mezzanine with 12 bits DACs.
B. LEDTSB – 64 channels LED triggering board

The source of the calibration signal is the TTCrx broadcast command, generated by Read Out Supervisor. Then this command is distributed by LHCb TTC system to each detector and propagated throughout the detector specific chains. In the calorimeter electronics this command is distributed by a CROC card to each slot of FE crate. There is no any delay time compensation of the bus length difference for different slots of the FE crate. The time spread of the broadcast command on the FE backplane could be up to 3 ns. Due to the reason mentioned above, an additional time-alignment with 40 MHz clock is needed and implemented in LED Trigger Signal Board (LEDTSB).

LEDTSB distributes the LED trigger pulses to LED drivers by a twisted pair cable (RJ-45) with a different for each sub-detector length. Then a light pulse from LED comes to PMT through the optic fiber and from PMT the signal comes to FEB.

LEDTSB specification
- Number of channels – 64.
- 16 output connectors RJ45 type on a front panel,
- A level of the output signals is LVDS,
- Each channel equipped with individual delay line that varies from 0 to 300 ns with 1 ns step,
- A LED trigger signal width is 50 ns,
- LEDTSB boards, the same size as LFB board, will be placed in the FE crate,
- Control Logic FPGA is placed on a mezzanine card and equipped with radiation hard ACTEL proASIC chip APA300.

- SPECS slave mezzanine card (developed in LAL) is used for connection with ECS and TTCrx decoding,
- There are two operational mode:
  A. The main mode, when the LED trigger signals are generated from TTCrx command,
  B. The trigger signals are generated from a build in internal generator (Freq. ~ 1 kHz).

Power consumption: +3.3 V -> 0.6 A; +5 V -> 0.1 A; -5 V -> 0.16 A.

IV. PERFORMANCE OF THE LED MONITORING SYSTEM

The calorimeter monitoring system is placed on the detector in a radiation hard environment. The electronics has been designed taken into account this factor.

Main characteristics of the monitoring system are mentioned below:
- Precision of the PMT gain monitoring is about 0.3 %.
- LED stability monitoring by a PIN diode with precision of 0.1 %.
- Individual time setting for each LED in range of 400 ns with 1 ns step.
- PIN diode with amplifier is used for monitoring the LED stability itself.
- Control Logic FPGA is placed on a mezzanine card and equipped with radiation hard ACTEL pro-ASIC chip APA300.
Memory of the scanning algorithm FPGA with 64 patterns of the output trigger signals allows perform all needed sequences for LED flashing.

The calorimeter monitoring system is linked to the LHCb ECS system by the SPECS serial bus (developed in LAL).

Temporary LED and PMT stability plots are shown on Figure 9 and 10. Each point corresponds to the mean value of PM amplitude for 200 events.

Time scan technique is used for a correct time adjustment of the LED monitoring system and checking an inter-crate synchronization. For doing the detector time alignment the automated process has been implemented to scan the LED delay from PVSS project and collect data by DAQ (increment step by step the 1 ns delay of the LEDTSB). Precision and stability of the signal arriving time measurement [3] is about of 0.3 ns. Figure 11 illustrates the LED signal scanned shapes of the HCAL module [4] and Figure 12 shows the time and amplitude distributions of the PMT response on LED flash.

V. ECS SOFTWARE FOR CONTROL OF THE LED MONITORING SYSTEM

LHCb's Experiment Control System is in charge of the configuration, control and monitoring of all the components of the online system. This includes all devices in the areas of: data acquisition, detector control (ex slow controls), trigger, timing and the interaction with the outside world.

The control framework of the LHCb is based on a SCADA (Supervisory Control and Data Acquisition) system called PVSSII. Which provides the following main components and tools:

- A run time database
- Archiving
- Alarm Generation & Handling
- A Graphical Editor
- A Scripting Language
- A Graphical Parameterization tool
The LEDTSB and LED intensity boards configuring is performed by standard FSM way. In the same time to prepare or modify a recipe one needs a mechanism to update recipe content. The LEDTSB **half Configuration** panel allows loading new values from the configuration files or from the dedicated CALO Data Base. The LEDTSB parameters could be modified and with using the expert LEDTSB panels too. After updating the recipe content one can save the recipe with specified name. Examples of the LED monitoring panels are shown on Figure 13 and 14.

![Figure 13: Device Unit panel of the LEDTSB delay triggering pulse configuration](image)

The designed LED monitoring electronics have been successfully commissioned and using now for preparing the calorimeter detectors for first beam.

VI. REFERENCES


Development and Testing of an Advanced CMOS Readout Architecture dedicated to X-rays silicon strip detectors

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Abstract

Design methodology and first test results of a novel integrated readout front end analog processor in a 0.35 μm n-well complementary metal-oxide semiconductor technology are reported. The specific processing channel consists of a low noise preamplification block and a pulse shaping stage and has been designed for multi-channel radiation detectors with capacitance ranging from 2 to 10 pF. Important feature is the novel CR-RC pulse shaper configuration. In this section, transconductance circuits are used and a new design approach using the Leapfrog methodology is applied. Considering the architecture measured performance, the prototype provides peaking time 1.81 μs, conversion gain of 3.31 mV/fC and ENC of 382 e− + 21 e−/pF. The system consumes 998 μW and the occupied area of the full VLSI structure is 0.202 mm². Characterization of the analog processor and measurements are presented supporting the theoretical analysis and confirming that the system operates according to nuclear spectroscopy design specifications.

I. INTRODUCTION

The current trend in high energy physics, biomedical applications, radioactivity control, space science and other disciplines that require radiation detectors, is towards smaller, higher density systems to provide better position resolution. Miniaturization, low power dissipation and low noise performance are stringent requests in modern instrumentation where portability and constant increase of channel numbers are the main streamlines. In most cases CMOS technologies have fully proven their adequacy for implementing data acquisition architectures based on functional blocks such as charge preamplifiers, continuous time or switch-capacitor filters, sample and hold amplifiers, analog-to-digital converters etc. in analog signal processing for particle physics, nuclear physics and X or beta ray detection.

While literature is available on the noise behaviour of the front end stages [1]-[2], contrary few studies have been performed on the pulse shaper circuit. The main problem in the design of nuclear spectroscopy VLSI shaping filters is the implementation of long shaping times in the order of μs. In the past, the possibility of implementing RC networks in integrated versions of high-order semi-Gaussian shapers were limited by technology constraints (maximum R and C values are in the MΩ range for the resistors and in the 100 pF range for the capacitors) with time constants usually not exceeding few hundreds of ns. To implement integrated RC networks with time constants in the range of μs, as is specified in our application, some topologies have been proposed [3]-[6]. All these solutions are based on the common principle of using current mirror to demagnify the current flowing in a resistor in order to operate as a higher value resistor with respect to its nominal value.

In this work an alternative design technique and a novel long shaping time readout analog processor, is presented with purpose to be used with a specific radiation detector. In the specific architecture the shaping filter, in controversy to the typical structures, is not based on op-amps which generally demand large-area input transistors and high bias currents, but on operational transconductance amplifiers (OTAs). The total CSA – shaper system is characterized by low power and low noise performance compatible with the stringent requirements of high resolution nuclear spectroscopy and appears being greatly flexible providing programmable operating bandwidth and consequently adjustable output pulse characteristics.

II. PREAMPLIFICATION STAGE DESIGN

The Preamplifier circuit is shown in Fig. 1. The core amplifier is a folded cascode structure, because of its high DC gain and the relatively large operating bandwidth. This configuration allows the DC level of the output signal to be the same as the dc level of the input signal. The CSA reset device was configured with a PMOS transistor (M11) biased in the triode region in order to avoid the use of a high value resistance.

![Preamplifier circuit with output level shifting stage](image)

Figure 1: Preamplifier circuit with output level shifting stage
Transistors M11 and M12 comprise a level shifter for the CSA output signal providing the capability to externally control the pre-amplification stage output signal DC level. Regarding the noise optimization of the preamplifier, an NMOS transistor with optimized dimensions was selected as the circuit input device [1]-[2].

III. SHAPING FILTER ANALYSIS AND DESIGN

Semi-Gaussian (S-G) pulse shaping filters are the most common pulse shapers employed in readout systems, their use in electronics spectrometer instruments is to measure the energy of charge particles [7] and their purpose is to provide a voltage pulse whose height is proportional to the energy of the detected particle. The theory behind pulse shaping systems, as well as different realization schemes, can be found in the literature [7]-[9]. It has been proved that a Gaussian shaped step response provides optimum signal to noise characteristics. However, the ideal S-G shaper in non casual characteristics. However, the ideal S-G shaper in non casual domain behaviour or output pulse shape [10]. Concerning the shaper peaking time, in order to achieve a predefined from the application specifications value, the shaper model passive elements should be suitably selected. The total CSA – 2nd order S-G shaper system transfer function using a Laplace representation is:

\[ H(s)_{\text{total}} = \frac{A_{pr}}{1 + s\tau_{pr}} \left( 1 + s\tau_{d} \right) \left( 1 + s\tau_{i} \right)^n \quad (4) \]

where \( A_{pr} \) is the preamplifier gain and \( \tau_{pr} \) is its rise time constant. If as input signal is a dirac pulse \( \delta(t) \), considering the inverse Laplace transform of the product, the output signal in the time domain is given by:

\[ h_{\text{total}}(t) = \frac{\sigma + ja}{\sigma - ja} \left[ H_{\text{total}}(s) e^{\sigma t} ds \right] \quad (5) \]

Solving the above integral, the output signal of the readout system is:

\[ h_{\text{total}}(t) = A_{pr} \cdot A_{sh} \left( k_1 e^{-\frac{t}{\tau_{d}}} + k_2 e^{-\frac{t}{\tau_{i}}} + k_3 e^{-\frac{t}{\tau_{d}}} + k_4 e^{-\frac{t}{\tau_{i}}} \right) \quad (6) \]

\( k_1, k_2, k_3 \) and \( k_4 \) are the below constants:

\[ k_1 = \frac{a}{a^2 - a^2 - b + 2c + a \cdot c + b(c + 2b) - b(c)} \quad (7) \]

\[ k_2 = \frac{b}{(b - a) \cdot (c - b)} \quad (8) \]

\[ k_3 = \frac{a \cdot b - c^2}{(c - a)^2 \cdot (c - b)} \quad (9) \]

\[ k_4 = \frac{(a + b - c) \cdot c - a \cdot b \cdot c}{(c - a)^2 \cdot (c - b)} \quad (10) \]

where \( a = (\tau_{pr})^{-1}, b = (\tau_{d})^{-1} \) and \( c = (\tau_{i})^{-1} \).

In order to design a flexible IC shaper that can provide a peaking time (μs range), the above theory was combined with the leapfrog design technique. The respective to Fig.4 two-port passive element network, was configured to implement an equivalent IC 2nd order S-G shaper filter (Fig.3).

\[ V_{in} \quad C_1 \quad L \quad C_2 \quad \frac{R_s}{2} \quad V_{out} \]

Figure 3: Equivalent RLC minimum inductance two port circuit of a 2nd order S-G shaper
The above passive element topology has a respective transfer function (Laplace representation) to the typical shaper model of Fig.2. Its Laplace representation is given below (2nd order S-G shaper). From the above two port network, the signal flow graph (SFG) of a second order S-G shaping filter is extracted (Fig.4). The output signal of the passive network, in relation to the SFG is given in (12).

\[ H(s) = \frac{1}{s^2 + s(LC + R) + L} \frac{1}{LC} \left( V_1 - V_\text{out} \right) \]  

\[ V_\text{out} = \frac{1}{sLC} \left( V_1 - V_\text{out} \right) \]  

Using the extracted SFG and the Leapfrog (functional simulation method) design methodology a 2nd order shaper is designed. The main advantage of the Leapfrog method over others filter design methods which also provide integrated structures is the better sensitivity performance and the capability to optimize the dynamic range by properly intervening during the phase of the original passive synthesis [11]-[13]. In order to implement the shaping filter, operational transconductance amplifiers (OTAs) were selected as the basic building cells. The symbol of the OTA is shown in Fig.5. Ideally, the OTA is assumed to be an ideal voltage-controlled current source and can be described by:

\[ I_0 = g_m (V^+ - V^-) \]  

where \( I_0 \) is the output current, \( V^+ \) and \( V^- \) denote the non-inverting and inverting input voltages of the OTA, respectively. Note that \( g_m \) (transconductance gain) is a function of the bias current, \( I_b \). An S-G shaping filter implementation using OTAs is greatly advantageous, since programmable characteristics are providing. In particular, tunability is achieved by replacing the \( RC \) and \( CR \) sections in the original passive model with active \( g_m \)-C sections, where the \( g_m \) can be adjusted with an external bias voltage or current. The 2nd order shaping filter that was designed using the above SFG and the leapfrog method is shown in Fig.6. The capacitor values and the OTA transconductances of the above S-G shaper are given in Table I. The shaper configuration was designed in order to provide a peaking time equal to 1.8 μs, which refer to a BW of 260 kHz in the low frequency region (\( f_c = 140 \) Hz). The passive element values of the respective RLC two port network of Fig.3 are given in Table I.

<table>
<thead>
<tr>
<th>IC Shaper</th>
<th>Discrete RLC Network</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active and Passive Elements</td>
<td>Passive Elements</td>
</tr>
<tr>
<td>( g_m_1 )</td>
<td>23.8 μA/V</td>
</tr>
<tr>
<td>( R_s )</td>
<td>100 kΩ</td>
</tr>
<tr>
<td>( g_m_2 )</td>
<td>11.5 μA/V</td>
</tr>
<tr>
<td>( R_s )</td>
<td>100 kΩ</td>
</tr>
<tr>
<td>( g_m_3 )</td>
<td>950 nA/V</td>
</tr>
<tr>
<td>( C_1 )</td>
<td>10.33 pF</td>
</tr>
<tr>
<td>( C_2 )</td>
<td>12.36 pF</td>
</tr>
<tr>
<td>( R_s )</td>
<td>10.33 pF</td>
</tr>
<tr>
<td>( C_1 )</td>
<td>1.00 nF</td>
</tr>
<tr>
<td>( L )</td>
<td>83.7 mH</td>
</tr>
<tr>
<td>( C_2 )</td>
<td>13.77 pF</td>
</tr>
<tr>
<td>( C_3 )</td>
<td>13.77 pF</td>
</tr>
</tbody>
</table>

Because of the non-integrable value of \( C_2 \) in the leapfrog shaper, the specific capacitance was substituted with a grounded OTA-C capacitor simulator. The respective OTA architecture is described in Fig.7 and its calculated value is shown below [11], [13]. The values of the transconductances and the capacitor \( C \) are \( g_m_4 = g_m_5 = g_m_6 = 74.4 \) μA/V, \( g_m_7 = 950 \) nA/V and \( C = 12.8 \) pF.

\[ C_{eq} = C \frac{g_m_4 g_m_5}{g_m_4 + g_m_5} \]  

Figure 5: Symbol of the OTA  

Figure 6: OTA based 2nd order S-G shaper using the leapfrog technique  

Figure 7: OTA based architecture for grounded capacitance simulation  

\[ I_0 = g_m (V^+ - V^-) \]
IV. FULLY INTEGRATED READOUT SYSTEM

The total IC readout analog processor was designed – simulated and fabricated in a 0.35 μm CMOS process (3M/2P 3.3/5V) by Austria Mikro Systeme (AMS) for a specific low energy X-rays silicon strip detector [14].

In the VLSI readout architecture, the power supplies are $V_{DD} = -V_{SS} = 1.65$ V. Considering the system pre-amplification stage (Fig.1), the feedback capacitance $C_f$ is 550 fF and is placed between the input node and the gate of the source follower stage to avoid introduction on the closed loop of the follower stage complex poles and to isolate the $C_f$ from the following stage. The bias current $I_{bias}$ was selected to be $10 \mu A$. The reset device bias voltage is fixed to 150 mV and the level shifting bias voltage is equal to $-1.18$ V. The dimensions of the CSA MOS devices are given in [14]-[15].

Considering the S-G OTA based shaping architecture, capacitor simulator and amplification topology, they were implemented using a CMOS OTA design, shown in Fig.9. In the transconductance circuit, a typical CMOS cascade configuration is used, where changing the bias voltage results in approximately equal changes for both the transconductance and the 3-dB frequency.

The total simplified block diagram of the analog readout ASIC is given in Fig.10. A photograph of the fabricated prototype chip where the above readout system was contained is shown in Fig.11.

V. EXPERIMENTAL RESULTS

The measured X-ray IC front end system output signal is shown in Fig.12. The system provides dc gain equal to 120 dB. However this value can be externally modified by fixing suitably the bias voltages and consequently changing the $g_m$ values of the OTA based amplification topology. Regarding the application specifications, the output pulse has a peaking time value of 1.81 μs that shows no undershoot or pile up. The power consumption is 998 μW, far lower than the maximum allowed specified value of 8 mW, rendering the system as low power. The readout ASIC noise performance was also analytically studied. The system $enc$ is $382$ e− for a detector of 2 pF and noise performance increases with a slope of $21$ e−/pF. The $enc$ dependence on the detector capacitance variations is shown in Fig.13. Considering the front end system energy resolution – linearity, it is presented in Fig.14. The CMOS readout analog processor achieves an input charge gain-voltage output conversion of $3.31$ mV/fC and a linearity of 0.69%. In terms of the total occupied area, the specific IC system is again advantageous since it consumes only $201743$ μm² of a total $2983 \mu m \times 2983 \mu m$ microchip (Fig.11).

Finally, another great advantage of the specific topology, and in particular of the proposed design methodology having OTAs as the architecture building cells, is the flexibility of the implementation. Both 3-dB frequencies of the system band-pass AC response can be externally modified. As a result the operating bandwidth and consequently the output pulse peaking time and the signal undershoot can be externally adjusted in relation to the application. The output noise can be regulated in relation to each application, since the output signal can have an undershoot (narrow BW) or not
VI. CONCLUSION AND DISCUSSION

Using the leapfrog filter design methodology and the Semi Gaussian shaping theory an advanced front end analog processor for a particular X-rays radiation detector was proposed. In the specific ASIC a novel shaping filter topology based on operational transconductance amplifiers is addressed. The total IC readout system compatibility to the stringent nuclear spectroscopy requirements is examined performing measurements that confirm its satisfactory performance. The architecture although it provides a relatively long peaking time, is fully integrated and appears to be greatly flexible since the use of OTAs as the topology building cells results to externally adjustable characteristics.

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REFERENCES

Design and measurements of SEU tolerant latches


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Abstract

Latches based on the Dual Interlocked storage Cell or DICE are very tolerant to Single Event Upsets (SEU). However, for highly scaled processes where the sizes continue to decrease, the data in this latch can be corrupted by an SEU due to charge sharing between adjacent nodes. Some layout considerations are used to improve the tolerance of the DICE latches to SEU and especially the influence of sensitive nodes separation is tested for DICE latches designed with a 130 nm process.

I. INTRODUCTION

The requirement for total dose tolerance for the ATLAS pixel detector has been estimated to 50 Mrad. Because of this high level of irradiation, the performance of the innermost layer of ATLAS pixel detector, the so-called b-layer, will start degrading after 2-3 years of LHC working. So, it is proposed to upgrade the b-layer detector. For this purpose, improvement in the electronic design of the pixel front end is under study and development using the 130 nm process [4].

At the time of the b-layer replacement, the level of radiation will be 3 times higher than at the start of the LHC. The total dose is estimated to reach 150 to 200 MRad and peak fluencies are close to 1x10⁸ particles/cm²/sec.

In principle, the commercial 130 nm process used to design the front end chip is less sensitive than older process generations to the effect of the total ionizing dose and irradiation tests made on individual devices are very promising.

However, we have to consider carefully the SEU for this highly scaled process. In fact, the device dimensions are small and the capacitance of storage nodes becomes lower. The supply voltage needed is low (1.0 V to 1.4 V for the 130 nm process). The critical charge needed to provoke an upset becomes lower than in older processes and digital designs become less tolerant against SEU.

Traditional flip flops are not suitable to be used in the b-layer environment. D flip flops based on the dual interlocked cell (DICE) latches have redundant storage nodes and restore the cell original state when an SEU error is introduced in a single node [5]. The probability that multiple nodes are affected by an upset is low, making the DICE latch less sensitive to SEU. However, as the device size shrinks, the space between critical nodes is reduced. The redundancy becomes less efficient because of the charge sharing between sensitive nodes of the DICE latch. For this reason, some hardened by design (HBD) approaches are used to reduce the effect of charge sharing.

A 130 nm test chip has been designed in order to study the effect of some layout techniques on the tolerance to SEU. Layout considerations are based on spatial separation of critical nodes, isolation techniques like isolated wells and guard rings and cell interleaving. Some prototype layout structures have been investigated in order to develop some rules to follow in the new design of the front end IC developed for the b-layer replacement.

II. DICE LATCH STRUCTURE UNDER TEST

A. DICE Structure

The DICE latch structure is shown in Figure 1. It is based on the conventional cross coupled inverter latch structure. The 4 nodes X1 to X4 store data as 2 pairs of complementary values.

![DICE latch structure](image)

Figure 1: DICE latch structure

For example, when the stored data are 0 then X1-X2-X3-X4 = 0101 and particularly X1 is low and X4 is high. If we assume a positive upset pulse on the node X1, the transistor...
MP2 is blocked avoiding the propagation of this perturbation to the node X2. At the same time the transistor MN4 will propagate a negative pulse to the node X4 blocking MN3 and avoiding X3 level corruption. The perturbation is then removed after the upset transient since the nodes X2 and X3 have conserved the true information.

However, if 2 sensitive nodes of the cell storing the same logic state (X1-X3) or (X2-X4) change the state level due to the effect of a single particle impact, the immunity is lost and the DICE latch can be upset.

In this work, we will show that the SEU probability is reduced by layout considerations and essentially if the transistors drain areas corresponding to the sensitive nodes are separated in the layout.

B. Description of the compared layouts

In order to evaluate the layout importance for the SEU tolerance, three different layouts were implemented for the same latch as shown in Figure 2. The cells are identical in schematic and use the same devices dimensions. They are based on the conventional DICE latch structure.

The main difference between the three layouts is the separation length between the drain areas of the sensitive nodes. Layout parameters are summarized in Table 1.

### Table 1: Parameters of implemented layouts

<table>
<thead>
<tr>
<th>Layout type</th>
<th>Size (µm)</th>
<th>Area (µm²)</th>
<th>nmos separation (µm)</th>
<th>pmos separation (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Latch A</td>
<td>16×3</td>
<td>48</td>
<td>2.4</td>
<td>8</td>
</tr>
<tr>
<td>Latch B</td>
<td>12×4</td>
<td>48</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>Latch C</td>
<td>12×4</td>
<td>48</td>
<td>9</td>
<td>5.4</td>
</tr>
</tbody>
</table>

III. EXPERIMENTAL TEST SETUP

A. Test structure

The test structure is designed around shift registers and triple redundancy latches as illustrated in Figure 3. The shift register uses conventional flip flops and allows to load and read-back data into and from the cells under test.

Each tested cell is composed of 3 latches connected in triple redundancy structure. A circuit block based on combinatory logic generates two flags per block of register cells: the error flag and the parity flag.

The error flag signal switches from 0 to 1 when the content of one latch of the block is changed. This flag indicates a latch upset.

The parity flag at the output of the block is determined as an XOR of all parity bits coming from the cells. A majority voting circuit is implemented in each cell in order to generate the cell parity bit which is changing the state when at least 2 among the 3 latches of the same cell change the state.

The combination of the parity flag and the error flag allows to indicate if an error has occurred in the triple redundancy cell.

The serial output from the shift register corresponds to the effective data memorized in the triple redundancy structure. The comparison between input and output shift register data determines the upset rate of the triple redundancy cell.
B. Test chip

The test chip shown in Figure 4 is designed exclusively for SEU test and characterisation. It is manufactured with commercial 130 nm process. It contains different blocks of shift registers connected in parallel and using the same clock and the same control signals as reset, load and read-back. The same mask of data is applied to all blocks of memories. Each register block generates its own error flag, parity flag and output data.

![Figure 4: SEU test chip](image)

C. Experimental setup

Figure 5 illustrates the test set up used for SEU evaluation. The chip under test is packaged on a PLCC44 package with 44 pins. It is controlled and read out by a DAQ system based on a PCMCIA card from National Instruments and controlled by a laptop PC. The PCMCIA card generates digital signals to control and read back the tested chip. The software to control the PCMCIA IO signals is written in C++ code using Lab-windows interface.

![Figure 5: Experimental test setup](image)

An interface board located in the computing area converts 5V TTL signals into LVDS signals. Those differential buffers drive a 20 meter twisted pair cable transmitting and receiving pattern and control signals in differential mode. An intermediate board located in the irradiated zone is connected with a 5 meters flat cable to the board under test. This board uses commercial devices and converts differential levels into single ended levels before arriving to the chip under test.

D. Facility

Irradiation tests were carried out using IRRAD3 beam line of the proton synchrotron (PS) facility at CERN. The test beam provides a beam of 24 GeV protons. The structure of the beam is defined by the operation cycle of the PS accelerator. The machine super-cycle period depends on the operation mode. It contains several spills of particles and it is distributed to the experiments sharing the beam. IRRAD3 beam line, used for the chip irradiations receives 1 to 4 spills per super-cycle.

The duration of each spill is 400 ms and the intensity can be tuned typically from 5 $10^{10}$ to 1.5 $10^{11}$ protons/spill. A secondary emission chamber (SEC) monitors the proton beam intensity.

However, the proton fluence is most accurately measured by irradiating thin foils of Aluminium. This method, measuring the gamma decay of $^{24}$Na produced by the protons in Aluminium allows a fluence measurement with an accuracy of ~8 %.

During the irradiation test, the beam arrives to the front of the chip with an incident angle normal to the die area. For this test, total proton fluence provided to the chip is around $2 \times 10^{15}$/cm$^2$.

IV. TEST RESULTS

A. Irradiation procedure

The experimental procedure consists of the following phases:

At the beginning of the machine cycle and outside the spill, a known data pattern is pushed in the shift registers and loaded in the memory cells. The error out signal is continuously read out from the chip. If the “errout” bit of one block of latches passes from 0 to 1, all blocks of latches are read back outside the spill duration. After this, data pattern is rewritten in the shift registers and loaded in all latches blocks. This operation is repeated every machine cycle. Since the shift registers flip flop is more sensitive to SEU than the latches under test, the write or read operations are carried out only before the spill duration.

B. Upset rate determination

The cross section is determined as the number of errors $N_{\text{errors}}$ over the fluence $\Phi$ divided by the number of the latches implemented in the block $N_{\text{latches}}$.

$$\sigma = \frac{N_{\text{errors}}}{\Phi \cdot N_{\text{latches}}}$$

Figure 6 illustrates the cross section measurements for “1 to 0” upsets. It shows that the B and C latches are less sensitive to “1 to 0” upsets. Latch C is 5 times more tolerant than latch A. This is attributed to sensitive area separation and isolation techniques used for latch B and C layouts.
Cross section measurements for "all 1" pattern

1.5E-15
3.4E-16
3.0E-16
0.0E+00
4.0E-16
8.0E-16
1.2E-15
1.6E-15
2.0E-15

Cross section (cm²)

Latch.A
Latch.B
Latch.C

Figure 6: Cross section for “all 1” pattern

Figure 7 shows that the latch A is a little more tolerant to upsets from “0 to 1”. It shows also that the latch C which uses interleaved layout is less sensitive than the latch B because sensitive areas are more separated.

Cross section Latch for "all 0" pattern

2.2E-16
5.9E-16
3.6E-16
0.0E+00
1.0E-16
2.0E-16
3.0E-16
4.0E-16

Cross section (cm²)

Latch.A
Latch.B
Latch.C

Figure 7: Cross section for “all 0” pattern

Figure 8 gives the cross section measurements with the “0101..01” pattern. Test results are obtained from a different device than the device used in previous measurements of cross sections. It shows that latches B and C are more tolerant to SEU when the stored pattern contains the same number of 0 and 1.

Cross section for "0101…01" pattern

5.9E-16
3.6E-16
2.4E-16

Cross section (cm²)

Latch.A
Latch.B
Latch.C

Figure 8: Cross section for “0101..01” pattern

V. CONCLUSION

It is well known that the DICE latch with redundant storage nodes makes the latch more tolerant to single event upset than a standard latch. However, the tolerance to SEU is affected by the charge sharing between sensitive nodes for DICE latches designed with highly scaled processes.

We developed in this work some layout considerations in order to improve the tolerance to SEU in the high scaled process. The influence of spatial separation of node pairs in DICE latch was measured. By reorganizing the layout of the studied latch, we obtained an improvement of a factor 3 in the SEU tolerance showing that the layout has a great importance in the charge sharing and so in the tolerance to SEU.

Some advanced simulations tools could be used to study the influence of other layout aspects like the effect of guard rings and nWell separation.

In the future, this work will be continued in order to measure the effect of the triple redundancy and the test set up will be improved in order to evaluate the sensitivity to SEU at 40 MHz.

VI. ACKNOWLEDGEMENTS

We would like to thank Maurice Glaser who is in charge of the PS facility at CERN for his precious assistance during the irradiation test. We would like also to thank P. Ollive and K. Arnaud for the test board design.

VII. REFERENCES

Characterization of the Noise Properties of DC to DC Converters for the sLHC

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Abstract

The upgrade of the Large Hadron Collider (LHC) experiments sets new challenges for the powering of the detectors. One of the powering schemes under study is based on buck converters mounted on the front-end modules. The switching noise emitted by these converters is susceptible to affect the performance of the powered systems. A model to identify and to control the noise sources of the converter was developed. A reference test setup with associated measurement methods is used to characterize the noise properties of the converter. Complementary tools and simulations were also used to evaluate the noise couplings at system level.

I. INTRODUCTION

The experiments at the Super Large Hadron Collider (sLHC) will be more demanding in terms of power and cabling than at the LHC, in particular for the trackers. The cabling constrains of the detectors, together with the thermal management and the overall power efficiency, force the development of new radiation hard and magnetic field tolerant powering schemes. One of the proposed schemes is based on air core buck converters [1] to be distributed on the front-end (FE) modules of the trackers [2].

The switching converter and its air core inductor will be placed in the close vicinity of the FE detectors and electronics. The FE system will be exposed to new sources of noise from the power converters (Fig. 1), in the form of conducted and radiated electromagnetic noise.

Like in industrial, medical or military applications, the reduction and control of electromagnetic interferences (EMI) is also a topic of primary importance for today’s high energy physics experiments. These interferences can produce malfunctions on the devices, because of this it has been necessary to establish limits for the maximum amount of radio frequency (RF) noise that an equipment can emit and the minimum noise that it must be able to tolerate. The electromagnetic compatibility (EMC) tries to achieve that goal, establishing limits for the harmony and well operation of the equipments when they are put together in a system. International EMC standards as CISPR were born, forcing the manufacturers to fulfill those limits for being able to sell their products in Europe and in the USA.

The theory of electromagnetic compatibility is well described in the literature [3][4], providing valuable guidelines for the engineers to develop systems in compliance with the standards at early stages of the design process. The understanding of the EMC aspects of a system requires a deep analysis, usually carried out on the basis of models that enable simulations. Several models have been published aiming to predict the common mode (CM) and differential mode (DM) noise for different kinds of switching converters. These models rely on simplifications, the most relevant one being the substitution of the switching devices with the waveforms seen across their nodes [5]. Further simplifications assume an ideal characteristic of critical passive components [6] or neglect the presence of parasitic capacitances between the board nodes and the ground plane [7].

This paper proposes a model to predict the CM current at the input and output ports of a PWM buck converter, considering the dV/dt that results from the switching action of the MOSFETs as the primary source of common mode current. The proposed model is based on the substitution described earlier of the power transistors with the switching voltage developed between the drain and source nodes. However, aiming for an improved accuracy of the model, the parasitic properties of the passive components and the stray capacitances between the board nodes and the ground plane are taken into account. This model was analyzed through parametric simulations, in order to find the fundamental factors that contribute to the generation of the CM noise. The determination of the noise sources and the associated coupling paths allow applying suitable grounding, shielding and filtering methods to achieve the required detector performance. Experimental results will be compared with the simulations, in order to validate the model.
II. MEASUREMENT METHOD FOR COMMON MODE CURRENT

To ensure an accurate and reproducible measurement of the conducted noise of a specific equipment under test (EUT), a standard and well-defined test setup is required. Fig. 2 illustrates the scheme used for measuring the common mode current of a power converter, where the following items are found:

- A copper ground plane to define a low impedance return path for the common mode currents. The converter is placed 40 mm above the ground plane, fixing in that way the stray capacitances with respect to earth of every node of the converter’s PCB.
- A standardized line impedance stabilization network (LISN) on both input and output ports. The LISN provides ideally a 50 \( \Omega \) common mode impedance to the ground plane between 150 kHz and 30 MHz, allowing for reproducibility and comparison of the results obtained at different test places. The LISN also provides the isolation of the conducted noise coming from the power mains and a port for measuring the RF voltage emitted by the EUT.
- Input and output shielded cables, with the shield ends bonded to the ground plane to prevent capacitive and inductive couplings.

Figure 2: Scheme of the measurement setup for DC/DC converters.

The common mode current is measured with a calibrated current probe and a high resolution EMI receiver. Fig. 3 shows a picture of the test bench used for the measurements.

Figure 3: Test setup.

III. CONDUCTED COMMON MODE NOISE MODELING

The arrangement of the power converter to be tested, fixed on the test bench and properly connected to the LISN, can be modeled for simulation purposes. This model tries to give an insight in the prediction of the CM current before the converter has been built, helping in the early design stage.

A prototype buck converter was modeled on this basis. The principal nodes of the buck converter and the stray capacitances between them were identified and are showed in Fig. 4. A 3D model of the converter’s printed circuit board was analyzed with Ansoft Q3D (Figure 5) in order to obtain the values of the stray capacitances between all the critical nodes and the ground plane. The obtained result is displayed as a matrix of order \( N \times N \) (see the Table 1), \( N \) being the number of nodes.

Table 1: Stray capacitance matrix in pF.

<table>
<thead>
<tr>
<th></th>
<th>Earth</th>
<th>N1</th>
<th>N2</th>
<th>N3</th>
<th>N4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Earth</td>
<td>- -</td>
<td>0.069</td>
<td>0.0062</td>
<td>0.0074</td>
<td>3.8097</td>
</tr>
<tr>
<td>N1</td>
<td>0.069</td>
<td>- -</td>
<td>0.018</td>
<td>0.0012</td>
<td>11.926</td>
</tr>
<tr>
<td>N2</td>
<td>0.0062</td>
<td>0.018</td>
<td>- -</td>
<td>0</td>
<td>3.3286</td>
</tr>
<tr>
<td>N3</td>
<td>0.0074</td>
<td>0.0012</td>
<td>0</td>
<td>- -</td>
<td>5</td>
</tr>
<tr>
<td>N4</td>
<td>3.8097</td>
<td>11.926</td>
<td>3.3286</td>
<td>5</td>
<td>- -</td>
</tr>
</tbody>
</table>

The power converters can have a switching frequency up to few MHz, and the resulting spectrum of harmonic frequencies that contribute to the conducted noise can span up to many tens of MHz. In this range of frequencies, the passive components
can’t be considered as ideal anymore. The impedances of the real passive components in Fig. 4 ($C_{in}$, $C_{out}$ and $L$) were measured using a HP 4194A impedance analyzer, and a three component model was obtained for each of them. The ideal passive components were replaced with the high frequency models (Fig. 6). Their values are shown in the Table 2.

In order to model the effect of the switches on the CM noise and to make the circuit linear, they are replaced by normalized AC voltage sources of 1V, phased out by 180 degrees. The substitution enables the fast AC simulation of the linear circuit using PSpice. These simulation runs predict the input and output common mode current for a normalized switch voltage of 1V for all the frequency range, expressed in ampere per volt. To compute the net common mode current emitted by the modeled converter, the frequency spectrum of the switch voltages is determined by means of the FFT of the waveform (Fig. 7). The obtained frequency voltage peaks are multiplied with the normalized CM current curves obtained from the simulation.

The method is exercised on the buck converter model described previously, taking into account the stray capacitances (Fig. 4), high frequency models (Fig. 6) and voltage sources instead of the switches (Fig. 7), as is shown in Fig. 8. The converter switches at 1 MHz, with a duty cycle of 25%. The drain to source voltage across the switches was measured with differential probes and its spectrum (obtained by FFT) is used to weight the normalized simulation data to explore the validity of the proposed model.

Table 2: High frequency model’s values

<table>
<thead>
<tr>
<th></th>
<th>R</th>
<th>L</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{in}$</td>
<td>8.8mΩ</td>
<td>0.72nH</td>
<td>30µF</td>
</tr>
<tr>
<td>$C_{out}$</td>
<td>8mΩ</td>
<td>1.45nH</td>
<td>14.1µF</td>
</tr>
<tr>
<td>$L$</td>
<td>90mΩ</td>
<td>531.8nH</td>
<td>22.5pF</td>
</tr>
</tbody>
</table>

Figure 6: High frequency model of the real components.

Figure 7: FFT of the temporal Drain-Source voltage in the lower switch.

Figure 8: Conducted Common Mode noise simulation model.
IV. MODEL ANALYSIS

The model allows exploring, with parametric simulations, the impact of each element on the input and output common mode current. It predicts that the conducted noise emissions are strongly dependent of the electrical properties of the input and output capacitances, in particular of the lead inductance (Fig. 9) and the series resistance (Fig. 10). Nevertheless, the value of the capacitance itself doesn’t play a major role, except at low frequencies (Fig. 11).

The proposed setup (Fig. 2) makes the measurement result insensitive to the stray capacitances to the ground plane, being the noise exclusively contributed by the design of the converter. This was corroborated empirically placing the converter at different heights and measuring the respective CM noise, finding no differences between the measurements. Actually, the LISNs provide a relatively low impedance path for the CM current, such that the current flowing through the stray capacitances is negligible. The design of the converter, and in particular the choice of the passive components, can be explored experimentally on the basis of the model simulations, making abstraction of any stray capacitance between the converter and the ground plane. It must be noted that this is not longer true if a short circuit is made between the return path and the ground plane.

In order to estimate the effect of the stray capacitances, the output LISN must be replaced by the model of the targeted load (taking into account the capacitance between the load and earth). In this configuration, the CM noise model becomes sensitive to the high frequency model of the load that is used, enabling the optimization of the grounding of the front-end to minimize the amount of noise current injected by the converter into it.

Figure 9: Normalized input common mode current versus $L_{C_{out}}$.

Figure 10: Normalized input common mode current versus $R_{C_{out}}$.

Figure 11: Normalized input common mode current versus $C_{C_{in}}$.

V. MODEL VALIDATION

To validate the results obtained with the model, a comparison between the simulation and the measurement was done for the converter prototype. Fig.12 shows the comparison for the measured and simulated first ten harmonic peaks. The simulations are in good agreement with the measurements, the bigger difference being found for the 4th and 8th harmonic, attributed to inductive near field couplings that are not taken into account by the proposed model.

Figure 12: Predicted and measured CM currents with the nominal array of capacitors.

The model analysis revealed a dominant contribution of the decoupling capacitors properties to the conducted noise current. To validate this, the same buck converter prototype was simulated and measured using different decoupling capacitors. The capacitors were measured and modeled with an impedance an-
alyzer, and then included in the PSpice model (Table 3). In the same way, the CM noise for the new converters was measured. First, 100µF ceramic capacitors were put at the input and output of the converter (Table 3). The comparison between the simulation and the measurement is illustrated in Fig. 13. In comparison with the original configuration (Fig. 12), it can be seen that the model predicts a 7.5dB increase of the CM current for the converter equipped with the new 100uF ceramic capacitors that is corroborated by the measurements.

If electrolytic capacitors are used instead (Table 3), the model predicts again a further increase of 12.9 dB of the noise current respect to the ceramic capacitors, again verified with the measurements. This proves empirically that the decoupling capacitors have a significant impact in the conducted CM noise emitted by the converter (Fig. 14).

VI. CONCLUSIONS

The powering challenge for the sLHC requires the understanding of the noise couplings mechanisms between power converters and the front-end electronics. For this, a model of the common mode current for a buck DC/DC converter has been proposed, considering the two switches as the dominant contributor of the emitted noise. An innovative method to make the circuit linear has been proposed, enabling simple parametric simulations that allowed the identification of the decoupling capacitors as critical components for the design process.

The simulation results were cross checked on prototypes with different arrangements of decoupling capacitors, confirming the announced sensitivity to the capacitors parasitic. The model appears to be in agreement with the measurements up to 10 MHz. Discrepancies are observed at some harmonic frequencies, attributed to inductive near field couplings that are not taken into account by the proposed model that considers the capacitive coupling as the major contributor in the noise.

The test setup on which the model is defined, using LISNs on the input and output power ports, is intended for standard measurements. It allows measuring the output common mode noise, to make the model insensitive to its position with respect to the ground structure and to maximize the noise emissions for their analysis.

For front-end specific studies, the output LISN must be replaced by the front-end load model that should include the real parasitic parameters with respect to the grounded structure.

REFERENCES


SUB-NANOSECOND MACHINE TIMING AND FREQUENCY DISTRIBUTION VIA SERIAL DATA LINKS

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Abstract

FERMI@ELETTRA is a 4th generation light source under construction at Sincrotrone Trieste. It will be operated as a seeded FEL driven by a warm S-band Linac which places very stringent specifications on control of the amplitude and phase of the RF stations. The local clock generation and distribution system at each station will not be based on the phase reference distribution but rather on a separate frequency reference distribution which has significantly less stringent phase stability requirements. This frequency reference will be embedded in the serial data link to each station and has the further advantage of being able to broadcast synchronous machine timing signals with sub-nanosecond temporal accuracy. The phase and amplitude of the phase reference line is measured for each pulse and used to calibrate the other measurements. This paper describes the architecture used to distribute the frequency reference along with the precision machine timing and clocking signals.

INTRODUCTION

The FERMI Linac under construction at Elettra will be used as an injector for a FEL and thus has very stringent stability requirements for the cavity RF fields. The proposed low level RF (LLRF) control system will utilize several novel techniques in order to meet the RF field specifications [1]. Among these is the distribution of a frequency reference in addition to the stabilized phase reference. The frequency reference can be distributed over the same high speed data links which will connect the individual cavity controllers to a central hub. The addition of an integrated digital phase shifter and external PLL at each controller enables all of the station clocks to be phase aligned to within several 10’s of picoseconds, providing very high temporal resolution for trigger transmission of and time stamping of data.

FERMI LLRF FREQUENCIES

Fig. 1 shows the necessary clocks and LO frequency for the S-band low level control system for FERMI. The entire phase error budget is 0.1˚, of which, it is reasonable to assume, 1/3 could be allocated to frequency and clock generation.

This translates to a total integrated drift/jitter of 22 fs in the LO and 156 fs in the ADC and DAC clock, if their shares is split 2/3, 1/6, 1/6 respectively. It will be exceedingly difficult to maintain these values so a scheme is proposed where the distributed phase reference (Pref) is measured in the same manner as the other S-band cavity signals, but using the LO and clocks generated from a reference frequency (Fref) which has significantly looser phase stability requirements. Variations in the measured value of Pref, which is necessarily assumed to be perfectly stable, become an indication of the drift/jitter of Pref, and are used to calibrate the other inputs measured with the same clocks. If Pref is measured on a millisecond timescale, then Fref can be allowed to have sizable drift/jitter below 1 kHz. Fref can also have significant jitter at frequencies above the system bandwidth of 5 MHz without degrading the performance of the controller.

The frequency reference can be generated locally at each station from the distributed Pref signal, but this approach has limitations and is problematic: tapping off Pref, either with a coupler or splitter, would have to be done with an isolation above 75 dB in order to introduce a phase error below 0.01˚. On the other hand, distributing Fref, as described below, leaves Pref untouched and also gives the LLRF stations clocks that are phase coherent to a fraction of a cycle.

Fref DISTRIBUTION ARCHITECTURE

Fig. 2 shows the architecture for distributing Fref as well as the generation the local clocks and LO. The individual LLRF controllers are connected via high speed serial Gigabit Transceiver Pairs (GTPs) to a µTCA standard module and backplane known as 'The Matrix' currently under development at CERN [2]. Each module has a single FPGA and hosts 16 serial links operating from the same clock. The backplane supports up to 12 modules. The GTPs are the main communications link between the individual controllers and the Matrix which has an Ethernet connection to a conventional workstation. The module FPGA will be driven by an external 241.6 MHz clock which is encoded into the transmitted data. At the receiver side the clock is recovered and passed through an 8-bit digital phase shifter (DLS). It then exits the FPGA and is used as the reference phase for an external PLL. A ultra low phase noise OCXO must be used to meet the jitter requirements at the LO frequency. Furthermore, the OCXO tuning range must be limited to 200 Hz so that the round trip phase length over the fiber (150 meters each way) changes by less than 0.1˚ over its entire frequency tuning range. The loop filter of the PLL is implemented digitally inside the FPGA. The OCXO output provides the clock for the bulk of the FPGA as well as the GTP transmitter,
PHASE LOCKING SCHEME

In the architecture shown in Fig. 2 data as well as the frequency reference (Fref) are transmitted over the same fiber link. The addition of a digitally controlled phase shifter, as well as an external PLL, allows for the phase locking of multiple systems to the same transmitted clock. Furthermore, the GTP links have a ‘loop-back’ feature providing the system with the ability to measure the round trip latency of the link in integer clock cycles. The sum of these features allow for the implementation of a global clock at each station with an absolute time resolution on the order of 20 ps. The following details this procedure.

Distributing the Reference Frequency

Fig. 3 shows the first step in the process: the distribution of Fref as the recovered clock from a serial link. Since the fiber links are of different length, and in different locations, there is no way to ensure that the phases are aligned or that they remain fixed in time.

Locking to the Phase Reference

Fig. 4 shows the second step: the phase reference is measured with the recovered clock and the error controls the DLL which compensates for drifts in the fiber. The 8-bit phase shifter has a granularity of about 1.4˚ or 16 ps at 241 MHz. At this stage the clocks at each station are still incoherent (since the phase of Pref is ultra stable but unspecified), however, their drift is now limited to 16 ps.

Aligning the Clock Phases

Fig. 5 shows the method that will be used to align the clock phases at each station.

Figure 2: Frequency reference (Fref) distribution scheme.

Figure 3: Distribution of Fref. Clock phases are not coherent and can drift.

Figure 4: Locking Fref to Pref. Clock phases are fixed.

Figure 5: Eliminating the fractional cycle with the DLL.
First, the GTP transceiver of the Matrix module is placed in ‘loop back’ mode which effectively short-circuits the transmitter to the receiver. This in turn presents a fixed phase to the PLL at the station. Since the OCXO has a limited range, the loop will quickly saturate. The round-trip phase of the fiber link can be seen as an integer number of cycles, NT, plus a fractional cycle, ΔT. Next, the phase of the DLL (δ) is incremented, and at some value, δ0, the fractional cycle, ΔT, will either be absorbed or augmented into a full cycle. At this point the PLL will saturate to the other limit or regain control if, by chance, δ0 happens to land within the OCXO’s tuning range (0.1˚) of zero phase. In either case at the point which this occurs the round trip phase of the link plus DLL is within one tick (1.4 ˚) of zero and the fractional cycle, ΔT, has essentially been eliminated. The module’s GTP can then assume normal operation with δ0 as the nominal operating point of the DLL. As this procedure is performed at every station the resulting clocks become phase aligned. Their long term coherence is guaranteed because they are locked to Pref, however, if a phase stable signal is not available the above procedure can be repeated, as necessary, to compensate for drifts.

Setting the Time and Sending Triggers

With the fractional cycle eliminated, the only ambiguity remaining is the integer cycle delay of each link. This, of course, is measured naturally with ‘loop-back’, and dividing the result by two gives the one way link delay for each station. The time can now be set at each station, ideally with a resolution of 1/256 of a cycle. This is shown in Fig. 6.

![Figure 6: Setting the time and sending triggers.](image)

Triggers can be pre-delayed at the Matrix, or adjusted at each station to compensate for the individual link delays.

NOISE CONSIDERATIONS

The above procedure for aligning the clocks, as well as the distribution of Pref, relies on the assumption that the serial link, clock recovery, and DLL will not add significant jitter to the transmitted clock. This has been tested with a GTP link, over coax, between two Xilinx ML506 test boards. Fig. 7 shows the results.

Three traces are shown. The bottom trace (blue), which serves as the baseline measurement, is the 240 MHz system clock used to encode the data on the transmitter board. It has an RMS jitter of 5 ps integrated from 1 kHz to 5 MHz. The middle trace (red) is the recovered clock from the receiver board which has an integrated jitter of 11 ps. The top trace (green) is the recovered clock after going through the DLL. Its integrated RMS jitter is 21 ps, which is less than two ticks of the DLL. The GTP link and DLL add about 15 ps of jitter indicating that the phase aligning procedure should be feasible. It is expected that the actual system, with an OCXO derived clock and PLL filtering, will have even lower jitter thus allowing the controller clocks to be aligned to 16 ps, the limit of the DLL.

![Figure 7: Noise measurements on GTP link with DLL.](image)

CONCLUSION

Presently a GTP link has been established between two FPGA test boards over coax. A phase shifter has been instantiated in the FPGA and tested with the 240 MHz recovered clock. The external PLL has not been tested nor have the ultra low noise OCXOs been acquired. This is the next step. The technique outlined here has the potential of establishing an trigger/event/data link among the individual controllers along an accelerator with a temporal accuracy in the few 10’s of picoseconds. Key to this development is the advent of a central FPGA based data hub, the ‘Matrix’, with its multiple, phase synchronized, serial data links. This architecture promises other interesting developments along the line of medium bandwidth (10’s of kHz) accelerator-wide control.

REFERENCES

A prototype ASIC buck converter for LHC upgrades

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Abstract
Given the larger number of channels and the need for reduced material budget in the SLHC trackers, alternatives to the present power distribution scheme have to be explored. In this context we are envisaging a new architecture based on custom switching converters able to work in the high radiation and high magnetic field environment of the experiments. A prototype converter has been designed and integrated in an ASIC. This includes the fundamental building blocks of a buck converter that can be used in later and more complete designs and even in different topologies. Design techniques and functional tests of the prototype will be discussed.

I. INTRODUCTION
In view of a possible upgrade of LHC trackers where the number of channels will increase and the front end (FE) circuits will probably require larger supply current at lower voltage, it is necessary to evaluate alternative power distribution schemes.

A promising approach consists in the distribution of power through a higher voltage bus (up to 12V) to DC-DC converters positioned close to the FE electronics. These locally convert the bus voltage to the low voltage needed by the FE chips, reducing the current in the bus by a factor close to the voltage conversion ratio, hence decreasing the power lost in the cables.

Commercial components are not targeted to work in the harsh experiment environment characterized by high radiation (more than 100Mrd in total dose) and high magnetic field (up to 4T). It is therefore necessary to develop a custom inductor-based switching converter where tolerance to radiation and magnetic field are specifically addressed.

As proposed in [1], a very attractive power distribution scheme based on DC-DC converters is composed by two different conversion stages. In particular, the first stage converts the 10V from off-detector power supplies to the voltages required for the analog (2.5V) and digital (1.8V) intermediate bus. This paper will present the development of a first prototype of a dc-dc converter for this conversion stage. Design techniques used for the stability of the feedback loop will be presented and layout specificities will be discussed.

II. DC-DC BUCK CONVERTER
The first prototype of the DC-DC converter integrates the basic building blocks of the buck converter that can be used in later and more complete designs and also in different converter topologies. It contains the two power switches and the control circuit. It is designed in a high voltage 0.35 um CMOS technology usually employed in automotive applications. Radiation tolerance can be achieved with the use of custom-modified layouts. Magnetic tolerance can be achieved using air core inductors that avoid magnetic core saturation, although at the price of introducing constraints in the design of the converter (mostly the switching frequency) [2]. This first prototype was designed for a maximum output current of 2A.

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The design of the converter follows the division of the converter in two main building blocks. The following subsections will explain the design methodology for the power transistors and the control circuit.

A. Power transistors

The power transistors design is one of the crucial parts of the development of the converter. It is necessary to optimize the dimension to reduce the switching and conductive losses as much as possible. Studies in this direction were already presented [3] together with radiation tolerance results. As already done for the frequency, it is possible to calculate the efficiency for different dimension of the switches and for different output currents. Fig. 4 shows that a good compromise for the different currents is reached for a transistor width close to 0.2m. This leads to an on-resistance of 165mOhm for a gate capacitance of 2nF.

B. Control circuit

The control section has to be properly studied in order to compensate for the disturbances caused by input line voltage and output load current variations and hence to ensure stability over a wide frequency range (bandwidth of the converter control loop). This means that the control circuit is able to maintain the output voltage stable for disturbances whose frequency is comprised in the bandwidth of the control loop.

We can notice that an increase of this bandwidth improves the stability of the converter, making the fidelity band of the voltage regulator wider. The second advantage, probably most important, of larger bandwidth is the raise of the speed of the voltage regulator to react to and compensate for input line and output load perturbations.

Nevertheless, an upper limit for the control circuit bandwidth is represented by the switching frequency f_S because the feedback loop does not have to be sensitive to the output ripple generated by the converter itself. In reality, such upper limit is rather in the range of f_S/10 due to op-amp limited bandwidth (ideally infinitive).

The control circuit design requires a system level model of the converter. The small signal model of the converter is normally used to analyze the variations of the output voltage around the desired steady-state value. This analysis was developed in [4]. The design of the control circuit can be divided in two main tasks: the design of the ASIC blocks (error amplifier, comparator, level shifter and bootstrap) and the choice of the external compensation network components. They will now be shortly expanded.

1) Error amplifier

The error amplifier (EA) circuit is a key point in the design of the control loop because its realization can produce considerable shifts on the transfer function. It is necessary to design the EA with a bandwidth larger than the one desired for the full control loop, otherwise this last will be reduced. Moreover, the gain has to be very high (at least 70dB) to
avoid errors on the value of the output dc voltage [3]. In this design the EA is implemented with a Miller amplifier with a DC gain of 80dB and a bandwidth of 15MHz. The power dissipated by this element is around 6mW.

2) Comparator
The comparator generates the PWM modulation from the output of the EA and the sawtooth ramp. The latter has very high frequency components, hence the comparator needs to have a very large bandwidth to avoid distortions of the output signal possibly affecting the width of the PWM modulation. The comparator was implemented as a 3 cascaded stages amplifier with a bandwidth of 100MHz and a dc gain of 50dB.

3) Non overlapping driver
The signal provided by the comparator is used to generate the drive signal of the two power switches. It is necessary to avoid any overlap of the two gate control signals to prevent shoot-through between the input node and ground at every cycle which could damage or at least drastically affect the efficiency of the converter. The correct timing of the two gate signals is depicted in Fig.5.

![Figure 5: example of non overlapping gate signals](image)

4) Level shifter and bootstrap circuit
The driving of the SW1 is difficult because the source of this transistor is connected to the output node, which is cyclically connected to Vin or ground. A special circuit is needed to shift the signal referred to ground (generated by the non overlapping driver) and refer it to the source potential. This can be done by a level shifter in combination with a bootstrap circuit. Basically the circuit maintains a capacitance (called bootstrap capacitor) charged to 3.3 V and it connects this capacitance between source and gate of the power MOS to switch it on. To switch it off the level shifter circuit connects the gate to the source.

5) Driver of the power transistor
The driving circuit needs to be able to switch on and off the transistor in few nanoseconds; therefore the drivers were carefully sized to cope with this requirement.

6) External compensation network
The compensation network is necessary to increase the bandwidth of the control loop and its DC gain. Three different compensation networks are available; they have been explained in [4].

For this development a type 3 compensation network is used in order to achieve a crossover frequency of 200KHz with a phase margin of 70°. The value of these passive components can be found using the equations given in [4].

IV. CIRCUIT LAYOUT
The design of the layout must take into account different issues. First of all the NMOS transistors have to be custom modified to increase their radiation tolerance. Low-voltage NMOS transistors in the control circuit are modified with standard ELT techniques [5][6][7] whilst high-voltage transistors require a slightly modified enclosed topology. Given the large current flowing (up to 4 A) in the power transistors their layout was studied to minimize the resistance between input and output terminals. The layout was also optimized to maintain low gate resistance to achieve short propagation delay of the gate signals. Multiple unit cells have been used for the design of these large transistors. This allows a more uniform distribution of the current over the different cells, hence a more efficient use of each cell. It also has the benefit that many more drain contacts are available, which improves the possibilities for routing and help increasing the yield of the circuit. The choice of the dimensions of the unit cell is driven by the necessity to compromise the occupied area and the time propagation of the gate signal. With this technology the resistance of the polysilicon and the gate capacitance set the maximum dimensions of the width of each transistors finger at 50 μm in order to have a gate rise-fall time below about 2ns (simulation). The optimum choice of 8 fingers for the unit cell, each with W=50 μm, yields a W of 400 μm. The 0.2 m width transistor is hence composed of 512 unit cells.

The external pad needs to be placed in order to decrease parasitic capacitance, resistance and inductance and to simplify the PCB design.

![Figure 6: layout of the DC-DC prototype](image)
V. PCB DESIGN

The PCB was developed, produced and mounted in RWTH, Aachen.

The PCB is depicted in Fig. 7. Inside the red circle the ASIC is bonded directly on PCB and covered by a globetop layer. High-frequency decoupling ceramic capacitors are located as close as practicable to their decoupling target (for example the input and output line), making use of the shortest connection paths to reduce inductive loops. It is mandatory to locate the components associated with the feedback circuit close to their respective controller pins, since they belong to a high-impedance circuit loop, sensitive to EMI pick-up. The area of node IND (Fig. 2 and Fig. 6) was kept as low as possible to decrease the capacitive coupling to the ground plane.

VI. MEASUREMENT ON THE PROTOTYPE

The prototype converter was manufactured and measured to verify its performance in terms of efficiency and noise emission. Fig. 8 shows an example waveform, measured with an oscilloscope, of the input and output voltage and the voltage at the inductor node. The measured output ripple is 30mVpp.

A. Efficiency measurements

Fig. 9 and Fig. 10 show the calculated (lines) and measured (dots) efficiency of the buck converter for different loads at room temperature. In Fig. 10 the efficiency is also shown when the converter is cooled with CO₂ ice. The measured efficiency is obtained by the output/input power ratio.

For Vin=5V (Fig. 9) the simulated and measured efficiencies are similar for frequencies up to 600KHz. For higher frequencies the measured efficiency drops. The same behaviour but with a higher drop can be appreciated in Fig 10 where Vin=10V. At 1Mhz and Iout=1A the measured efficiency is around 10% lower than the estimate.

Our hypothesis concerning the origin of this discrepancy is not yet fully confirmed. We suspect an overlap in the signals driving the gate of the two switches, because of which a large current (proportional to Vin/(R_{onSW1}+R_{onSW2})) flows to ground for few nanosecond at each cycle, leading to an additional loss. In this case the efficiency should be inversely proportional to Vin and f_{sw}, in agreement with our observations. Further measurements will be carried on to verify this hypothesis.

B. Noise Measurements

Output common mode noise measurements were carried out at CERN on the reference test bench of the ESE group [8], [9]. Fig. 11 and Fig. 12 show the output common mode noise current in dBua vs the frequency for an output voltage of 2.5 V, a load current of 1A and a switching frequency of 1Mhz.
The input voltage is set at 5V for Fig. 11 and 10V for Fig.12.

The highest peak coincides with the switching frequency and all the other harmonics are present. The red line represents the limit of the CISPR Standards [6]. This can help to fix a limit and compare the results when converters parameters are changed. When the ratio Vout/Vin is close to 0.5 the duty cycle tends to 50% and we can see a decrease of the even harmonics (Fig. 11). This can be explained through the study of the FFT of a square wave. If the duty cycle is 50% we have complete cancellation of the even harmonics.

Compared to other prototypes with commercial components theses noise performances are promising for a first prototype. This prototype was used to power two different silicon strip fron-end modules [10][11], in one of the cases without penalties to the noise performance.

VII. CONCLUSIONS

In view of a new power distribution scheme in the SLHC detectors, we have shown how to integrate a simple DC-DC stepdown converter that copes with the magnetic field requirements of the SLHC environment. The main building blocks of this first prototype, in particular the control circuit whose performance is very satisfactory, will be used in more mature versions of the converter, and are usable also in different converter topologies. Measurements of common mode noise are also encouraging, since the performance is comparable with the one measured for commercial components.

The origin of the lower efficiency measured with respect to our estimate has to be investigated further to confirm our hypothesis on gate signals overlap, and shall be eliminated in further prototypes. Radiation tests are also foreseen, although the available radiation data on the used technology indicate that our objectives in terms of radiation tolerance can not be met by the power switches used in this design.

Work has started in view of the integration of the sawtooth generator, the reference voltage and the compensation network on-chip in the next prototyping cycle.

VIII. ACKNOWLEDGEMENTS

Acknowledgments go to Walcaw Karpinski for the development of the PCB.

IX. REFERENCES

Mezzanine Cards for the EMU CSC System Upgrade at the CMS

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Abstract

In this paper we discuss two ideas related to the design and application of mezzanine cards in the Endcap Muon (EMU) Cathode Strip Chamber (CSC) electronic system at the CMS experiment at CERN. The first is a proposal to upgrade the FPGA-based mezzanines using the most advanced Xilinx Virtex-5 family of FPGA. The second is related to design of a simple and compact mezzanine card with a commercial serializer/deserializer (SERDES) device and industry standard pluggable optical or copper transceiver module. Such a card could be a basic element of the general purpose gigabit data transmission link.

I. INTRODUCTION

The CSC detector comprises 468 six-layer multi-wire proportional chambers arranged in four stations in the Endcap regions of the CMS [1]. Wires run azimuthally and define track’s radial coordinate. Strips are milled on cathode panels and run lengthwise at constant width. The goal of the CSC system is to provide muon identification, triggering and momentum measurement.

The numbers of cathode and anode channels in the CSC system are 218K and 183K correspondingly [1]. There are almost 15,000 electronic boards with approximately 5,000 Xilinx FPGA [2] in the entire CSC system. More than 1,000 FPGA are mounted on small mezzanine cards that have been produced and installed on host boards of five types. The host boards reside directly on the chambers, in 9U crates on the periphery of the return yokes and in the Track Finder crate in the underground counting room. The mezzanine approach allows us to independently design, develop and upgrade the FPGA-based processing logic while preserving the host board interface part. The present electronic system is based on mature Virtex-E and Virtex-2 technologies. The new and most advanced family of Xilinx FPGA, the Virtex-5, offers several advantages over previous generations. We have targeted two of our existing FPGA projects, the Muon Port Card (MPC) and the Muon Sorter (MS), to the Virtex-5 XC5VLX family of FPGA.

The mezzanine approach can also be applied to data transmission links. The main parts of a typical serial digital link include the serializer (SER) and optical or copper transmitter on a transmission end and the optical or copper receiver and deserializer (DES) on a receiver end. In many cases the SER and DES functions are combined in a single SERDES device. Optical modules are typically transceivers; among industry standards in the range from 1Gbps to 4Gbps the most popular is the Small Form-factor Pluggable (SFP) standard [3]. In addition to optical, copper SFP modules (either passive or active) are also available. The idea of combining a SERDES device and a pluggable transceiver on a mezzanine card is not new, but existing implementations usually require relatively large space. Since both the Texas Instruments TLK family of SERDES devices [4] and the SFP standard have significant potential for future projects, including the CMS upgrade, we have decided to build a simple, small and inexpensive mezzanine card using these components. We describe this mezzanine card in detail in the paper.

II. CSC ELECTRONIC SYSTEM

The CSC electronic system consists of: (1) on-chamber anode and cathode front-end boards (AFEB and CFEB); (2) Trigger and DAQ boards in sixty 9U crates on the periphery of the return yoke of CMS; and (3) one Track Finder (TF) and four Front-End Driver (FE) 9U crates located in the underground counting room (Fig.1).

The Level 1 CSC Trigger Electronics provides four trigger candidates to the CMS Muon Trigger within 80 bunch crossing (2 μs) latency.

There are three types of electronic boards mounted on each chamber: Anode Front End Boards (AFEB), Cathode Front End Boards (CFEB), and one Anode Local Charged Track (ALCT) board. The AFEBs (12..42 per chamber, depending on chamber size) amplify and discriminate the anode signals. The CFEBs (4 or 5 per chamber) amplify, shape and digitise the strip charge signals. The anode patterns provide more precise timing information than the cathode signals, and also provide coarse radial position and angle of passing particle for the trigger chain. The FPGA-based processing unit in the ALCT searches for patterns of hits that would be consistent with muon tracks originating from the interaction point. The patterns are considered valid, if hits from at least four planes are present in the pattern.

Two valid anode patterns, or ALCT’s, are sent to the Trigger Motherboard (TMB). Based on comparator half-strip hits sent from CFEBs, the TMB searches for two patterns of hits from at least four planes and then matches these two CLCT patterns with two ALCT ones, making a correlated two-dimensional LCT.
Up to nine TMBs, in pairs with Data Acquisition Motherboards (DMB), one Clock and Control Board (CCB), and one MPC reside in the peripheral crates mounted along with the outer rim of the endcap iron disks. Every bunch crossing, the MPC receives up to 18 LCTs from 9 TMB boards, sorts them and sends the three best selected track stubs via optical links to the Sector Processor (SP) residing in the TF crate in the underground counting room.

The TF comprises 12 SP boards, the MS and the CCB. Each SP receives 15 data streams with trigger primitives from five MPCR and performs track reconstruction. The decision, three selected tracks, is sent to the MS over custom backplane. The MS sorts out 36 incoming tracks and selects the four best ones and transmits them over copper links to the Global Muon Trigger receiver in the Global Trigger crate.

The four Front End Driver (FED) crates include 36 Detector Dependent Unit (DDU) boards and 4 Data Concentrator Cards (DCC). They assemble the data from all the 468 DMBs for transfer to the main CMS DAQ system as well as to local DAQ farm for real time monitoring.

### III. UPGRADE OF THE FPGA MEZZANINE CARDS

The design and construction of the CSC Trigger electronic system was a collaborative project lasting approximately 10 years from 1997 to 2006 with participants from several US universities, Fermilab, CERN, and PNPI (St. Petersburg, Russia). Given stringent requirements on latency and elaborate track reconstruction algorithms, it was decided from the very beginning to build a flexible Trigger and DAQ system based on programmable logic devices. The Xilinx family of Virtex FPGA devices was chosen as the most advanced in the industry (Table 1). It was also proposed to put the FGPA on relatively small mezzanine boards to allow independent development and future upgrades of the FPGA-based processing logic.

#### Table 1: Evolution of the Xilinx Family of Virtex FPGA

<table>
<thead>
<tr>
<th>Xilinx Family</th>
<th>Virtex</th>
<th>Virtex-E</th>
<th>Virtex-2</th>
<th>Virtex-4</th>
<th>Virtex-5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Year</td>
<td>1999</td>
<td>2000</td>
<td>2001</td>
<td>2004</td>
<td>2006</td>
</tr>
<tr>
<td>Technology</td>
<td>220 nm</td>
<td>180 nm</td>
<td>130 nm</td>
<td>90 nm</td>
<td>65 nm</td>
</tr>
<tr>
<td>Core power</td>
<td>2.5V</td>
<td>1.8V</td>
<td>1.5V</td>
<td>1.2V</td>
<td>1.0V</td>
</tr>
</tbody>
</table>

The two main requirements for the FPGA and its mezzanine card are defined by: (1) the amount of logical resources (configurable blocks, memory) for a given functionality and (2) the required number of input/output (i/o) pins. It was estimated that for the ALCT, TMB and MPC boards the number of i/o of less than 500 is sufficient, while the numbers of i/o for the SP and MS are very similar and significantly higher, close to 750. So, in 2001-2002, when the mezzanine idea was adopted, it was decided to build two custom mezzanine cards: one (108×104 mm) for the ALCT, TMB and MPC, and another one, (140×80 mm), with more i/o, for both the SP and the MS. The same family of high-density 4-row Samtec 100-, 140-, 160- and 200-pin connectors was chosen for both mezzanines, with sockets installed on the motherboard, and shrouded pins on the mezzanine.

For the first mezzanine, the Xilinx XC600E/1000E pin compatible FPGAs were selected. While the design of all motherboards continued to evolve (all the host boards underwent typically two or three revisions), it became clear that even the XC1000E FPGA does not have enough logical resources for the TMB functionality. So the second version of the mechanically compatible mezzanine based on XC2V4000-5FF1152 FPGA was built specifically for the production TMB2005 board. Due to lower power voltages required by the Virtex-2 FPGA, this mezzanine, however, is electrically incompatible with the initial version. Both versions were designed and built at the UCLA and PNPI.

Another mezzanine for the TF boards was designed at the University of Florida (Gainesville) and PNPI. It is based on the same XC2V4000-5FF1152 FPGA, but has six connectors to provide more i/o connections with the host boards. All three boards are shown in Fig.2. In addition to FPGA (that resides on the top side for the TF mezzanine and on the bottom side for another two boards) each board carries 3, 4 or 5 PROMs of the XC18V04 type.

![FPGA Mezzanines for the CSC Trigger Boards](image)

The FPGA configuration mode is set to “SelectMAP” which provides a parallel 8-bit path between the FPGA and EPROM and the fastest reconfiguration time (25 ms for XC600E, 40 ms for XC1000E, 100 ms for XC2V4000). All the mezzanines have four large mounting holes. The ALCT/MPC/TMB mezzanines are 63 mil thick printed circuit boards and have an additional thick metal plane on the bottom side for rigidity. The TF mezzanine is 93 mil thick.

#### A. Advantages and Limitations of Virtex-5

Virtex-5 [3], the most recent addition to Virtex family of Xilinx FPGA, has several advantages over previous generations of Virtex-2 and Virtex-4, including better performance due to advanced 65 nm technology, more flexible basic slice that contains four LUT and four flip-flops, and, potentially, shorter configuration time from the PROM.

Virtex-5 comprises four sub-families: general purpose LX, serial connection oriented LXT, signal processing oriented SXT, and embedded applications oriented FXT. Out of these four sub-families, the general purpose LX is the most suitable for the CSC Trigger system.
for our applications. Among the disadvantages of the Virtex-5 compared to the Virtex-2 are fewer package options and reduced (on average) number of I/O pins (Table 2). For example, for the XC2V4000 FPGA there are two packages available, FF1152 and FF1517, with 824 and 912 I/O pins correspondingly. For a comparable Virtex-5 FPGA, the XC5VLX110, two large packages, FF1153 and FF1760 are available as well, but the maximum number of I/O is only 800 for both. This limitation is not critical for the ALCT, TMB and MPC boards, but could be important for the SP and MS.

Table 2: Selected package options for Virtex-2 and Virtex-5

<table>
<thead>
<tr>
<th>Package</th>
<th>27 x 27 mm</th>
<th>35 x 35 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex-2 XC2V1500/2000/3000</td>
<td>392/456/484</td>
<td>FF666/FF676</td>
</tr>
<tr>
<td>Virtex-5 XC5VLX30/50/85/110</td>
<td>400/440/440/440</td>
<td>FF1152/FF1153</td>
</tr>
<tr>
<td>Virtex-2 XC5VLX4000/6000/8000</td>
<td>824/924/924</td>
<td>FF1152/FF1153</td>
</tr>
<tr>
<td>Virtex-5 XC5VLX50/85/110</td>
<td>560/560/800</td>
<td></td>
</tr>
</tbody>
</table>

B. FPGA Choice for the New Mezzanine

Based on requirements listed above, for the new TF mezzanine the number of available I/O should be in order of 800. 7 members of the LX family of Virtex-5 FPGA are offered in 4 packages [2], and either FF1153, or FF1760 meets our requirement. The FF1760 package would be best due to pin compatibility of the three largest devices (XC5VLX110, XC5VLX220, XC5VLX330), but its layout, obviously, is more challenging. The XC5VLX110 chip in the FF1153 package is the second option.

For resource estimate the most recent Muon Sorter project was targeted to the XC5VLX110 FPGA and compiled using the Xilinx ISE 9.1 development system. A comparison with the XC2V4000 FPGA is shown in Table 3. As one can see, the resource usage is 30..50% lower for the XC5VLX110 FPGA while the performance is about the same for the speed grade –1 (slowest) device and ~48% higher for the middle grade –2 device. So, the XC5VLX110 FPGA seems to be the optimal solution, unless a significant increase in design functionality and resource usage is expected.

For the ALCT, TMB and TMB the number of I/O pins is in order of 500, so the FF1153 package is the most suitable. Three lower end pin compatible devices in the family, the XC5VLX50, XC5VLX85 and XC5VLX110 have 560, 560 and 800 I/O pins respectively.

For resource evaluation the Muon Port Card project was targeted to the XC5VLX50 FPGA and compiled using the Xilinx ISE 9.1 development system. A comparison with the XCV600E-8FG680C FPGA that is being used on the present MPC mezzanine is shown in Table 4. As we can see, the resource usage is lower for the XC2VLX50 while the performance is ~47% higher for the speed grade –1 (slowest) device and ~66% higher for the grade –2 device. So, the XC5VLX50 or XC5VLX110 FPGA seem to be the optimal solution, unless a significant increase in design functionality and resource usage is expected.

The total number of configuration bits for the XC5VLX50, XC5VLX85 and XC5VLX110 devices is 12.6M, 21.8M, and 29.1M bits correspondingly, so only one XCF32P Flash PROM is required for any of these devices. The speed of downloading for the XCF PROMs is twice higher than for the XC18V PROMs. Using the SelectMAP configuration option and an 8-bit parallel path at 33MHz, configuration time will be 54, 80 and 100 milliseconds correspondingly for these devices. It is possible to use 16- and 32-bit configuration options and reduce the configuration time twice or even four times, but then either two, or four PROMs would be needed. For comparison, the configuration time of the XC2V4000 FPGA from four XC18V04 PROMs is 100 ms.

IV. MEZZANINE GIGABIT LINK

Low-cost low-power TLK SERDES devices [4] available from Texas Instruments have proven to be reliable in many applications, including existing LHC sub-systems. Seven pin compatible devices support serialization and deserialization of 16- or 18-bit parallel data patterns from 25MHz to 156.25MHz with the industry standard 8B/10B or start/stop encoding, provide either current- or voltage-mode serial interface and have an embedded PRBS generator (Table 5).

Table 5: Texas Instruments TLK Family of SERDES Devices

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Parallel Bits, bit</th>
<th>Serial Interface</th>
<th>Bit Rate, Gbps</th>
<th>Reference Clock Frequency, MHz</th>
<th>Encoding Method</th>
<th>Embedded PRBS generator</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLK50H</td>
<td>16</td>
<td>CML*</td>
<td>0.5-1.3</td>
<td>125-156.25</td>
<td>Stop/Start</td>
<td>100</td>
</tr>
<tr>
<td>TLK70H</td>
<td>16</td>
<td>CML*</td>
<td>1.2-2.5</td>
<td>80-153</td>
<td>Stop/Start</td>
<td>100</td>
</tr>
<tr>
<td>TLK1501</td>
<td>16</td>
<td>VML*</td>
<td>2.3-3.24</td>
<td>80-153</td>
<td>Stop/Start</td>
<td>100</td>
</tr>
<tr>
<td>TLK1502</td>
<td>16</td>
<td>VML*</td>
<td>0.5-1.3</td>
<td>60-65</td>
<td>None</td>
<td>100</td>
</tr>
<tr>
<td>TLK1503</td>
<td>16</td>
<td>VML*</td>
<td>1.2-2.5</td>
<td>56-125</td>
<td>Stop/Start</td>
<td>100</td>
</tr>
</tbody>
</table>

* CML – Current Mode Logic, VML – Voltage Mode Logic

The SEFDES card [5] design is optimised for minimal width. Its dimensions are 103 mm in length, 23 mm in width and 13.7 mm in height (Fig.3). We have chosen the Samtec MOLC-120-31-S-Q 80-pin 4-row high density (1.27 mm pitch) thru-hole connector for connection to the host board.
The host board requires the FOLC-120-01-S-Q mating socket. The TLK device, SFP connector and cage are all assembled on one side of the mezzanine card which is facing the host board when plugged in. There is a small (~1.5 mm) clearance between the SFP cage and a host board.

![Figure 3: SERDES Mezzanine Board (top and bottom views)](image)

All seven TLK devices are pin compatible, but there are minor differences in serial and control/status interfaces. While three TLK1501/2501/2701 devices have current-mode (CML) output drivers, the others use voltage-mode logic (VML). The VML drivers have the advantage that they do not need to have pull-up or pull-down resistors, so the two corresponding resistors on a mezzanine card are not required for the VML-compliant devices. The TLK3101 also has an embedded biasing and termination circuits for the serial receiver, so even fewer external components are required. More technical details are available in [6]. The coupling between the TLK transceiver and SFP module is always AC-type; serial capacitors on the receiver and transmitter data paths are embedded into the SFP optical or copper module.

The host board interface supports the following signals: 16-bit transmit and 16-bit receive paths for the TLK device, reference clock for the transmitter and recovered clock from the receiver; 6 control inputs and two status outputs to/from the TLK, 5 control outputs and 2 status inputs to/from the SFP module. Note that all the TLK devices require a very stable reference clock with a jitter below 40 ps. The host board also provides the +3.3V and +2.5V supply voltages. Alternatively, the +2.5V can be produced on the mezzanine from +3.3V using the on-board voltage regulator. This option is selected by a jumper.

Typical power dissipation at a maximal data rate is 250mW, 362mW, and 450mW for the TLK1501, TLK2501 and TLK3101 devices respectively. Power dissipation of the SFP optical modules varies from vendor to vendor, but usually is approximately 500mW (typ) and 750mW (max).

V. CONCLUSION

The mezzanine approach proved to be a valuable solution in large electronic systems, such as the CSC EMU system at CMS, requiring extensive maintenance and upgrades. It could be applied to such parts as FPGA, data transmission links and other parts requiring flexibility and modifications.

The results of simulation of two of our designs targeted to Virtex-5 FPGA, show an increase in performance of ~50% for the mid-grade speed devices while more logic resources are still available for additional functionality. The ability of the Virtex-5 FPGA family to self-correct single event errors and report double errors using the Internal Configuration Access Port (ICAP) is essential for the future SLHC upgrade.

We have designed and built a small mezzanine card that houses one of the Texas Instruments pin compatible gigabit transceivers of TLK series, pluggable SFP optical or copper module and a high density 80-pin connector that provides parallel 16- or 18-bit interfaces to transmitter and receiver and all the required control and status signals to a host board. Seven Three pin compatible TLK devices operating at data rate from 25MHz to 156.25MHz can be used. The low height of below 14 mm allows to place the mezzanine on most standard carrier boards. For example, up to 8 mezzanines can be placed on a 6U VME or CompactPCI card; and up to 14 on a 9U VME board. Sample boards with the TLK1501/2501/3101 devices are available for evaluation.

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Detector Control System for the Electromagnetic Calorimeter in the CMS Experiment
Summary of the first operational experience

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Abstract

A full scale implementation of the Detector Control System (DCS) for the electromagnetic calorimeter (ECAL) in the Compact Muon Solenoid (CMS) experiment is presented.

The operational experience from the ECAL commissioning at the CMS experimental cavern and from the first ECAL and global CMS data taking runs is discussed and summarized.

I. INTRODUCTION

The CMS experiment is one of the two large multi-purpose detectors at CERN’s Large Hadron Collider (LHC) \([1]\). CMS is currently installed at LHC’s access point number 5 (P5) situated at Cessy (France) and is under final commissioning. One of the most accurate, distinctive and important detector systems of the CMS experiment is the high precision Electromagnetic Calorimeter (ECAL). It will provide measurements of electrons and photons with an excellent energy resolution (better than 0.5% at energies above 100 GeV \([2]\)), and thus will be essential in the search for new physics, in particular for the postulated Higgs boson.

In order to successfully achieve these physics goals the ECAL collaboration has designed the calorimeter as a homogeneous hermetic detector based on 75848 Lead-tungstate (PbWO\(_4\)) scintillating crystals. Avalanche Photo Diodes (APD) and vacuum phototriodes (VPT) are used as photodetectors in the barrel part and in the end-cap parts of the detector, respectively \([2]\). All these components and front-end (FE) readout electronics inside the ECAL satisfy rigorous design requirements in terms of their response time (less than 25ns), signal-to-noise ratio, immunity to high values of the magnetic field induction (up to 3.8T in the barrel part of the ECAL) as well as in terms of radiation tolerance (expected equivalent doses of up to 5 kGy and neutron fluence of up to \(10^{12}\) neutrons/cm\(^2\)) \([2]\). However, it has been shown that the light yield of PbWO\(_4\) crystals and the amplification of the APDs are highly sensitive to temperature and bias voltage fluctuations \([3, 4]\). Therefore, the usage of these components has directly imposed challenging constraints on the design of the ECAL, such as the need for rigorous temperature and high voltage stability. At the same time, mechanisms that allow radiation to induce changes in crystal transparency (and hence in its response), imposed additional requirements for “in situ” monitoring of the crystal transparency \([2]\). For all these reasons specific ECAL sub-systems that provide the necessary services had to be designed. These include: Cooling system \([5]\), High Voltage (HV) and Low Voltage (LV) systems \([6,7]\), Detector Control Units (DCU), Precision Temperature Monitoring/Humidity Monitoring (PTM/HM)\([8]\) and ECAL Safety System (ESS)\([8]\). In addition, a Supervisor application to summarize the status of all ECAL DCS subsystems was also implemented. The structure of ECAL DCS is summarized in Figure 1.

All ECAL DCS applications were developed in a SCADA (Supervisory Control and Data Acquisition) system called PVSS II (Prozess Visualisierungs und Steuerungs System)\([9]\).

![Figure 1: ECAL DCS layout](image)

II. ECAL SUPERVISOR

Implemented as a Finite State Machine (FSM) using the Joint Controls Project (JCOP) FSM component, the supervisor allows authorized users to issue commands and displays calculated states from all ECAL subsystems. Access control was implemented at all levels in order to prevent unauthorized use of the system.
Updates with new features and improvements are released regularly and so far problems concerning the application were observed only during installation processes. Figure 2 shows the main screen of ECAL Supervisor.

The main issue during commissioning, still under investigation, is related to the JCOP framework FSM blocking from time to time, which necessitates it being restarted.

During the initial phase of commissioning several problems were experienced related to the CMS primary cooling circuit, which caused interruptions on the ECAL cooling. Apart from that the system was always stable and reliable.

The development of the connection between the cooling control and the cooling monitoring system, developed as part of the ECAL DCS, is still ongoing.

III. ECAL COOLING CONTROL AND MONITORING

This has been implemented through the Unified Industrial Control System (UNICOS) framework, designed by CERN. The final hardware configuration consists of 72 pneumatic valves, 45 temperature PT100 sensors, 42 flow meters reading in magnetic field and radiation, 150kW heater powered by thyristors controlled by PID with PWM regulation.

The system has failsafe hardware interlocks connected to ESS with Supermodule(SM)/Dee granularity. The cooling PLC (Programmable Logic Controller) is monitored by ESS (watch-dog) as well.

Recently the regulation was tuned to +/- 0.02°C at the detector input. A sample of regulation plots showing recent performance can be found in Figure 3.

The final configuration for the barrel hardware consists of 18 CAEN crates, with 8 boards per crate and 9 channels per board totaling 1296 channels, from which 1224 are used. The endcaps hardware consists of 2 crates, with 2 boards per crate and 4 channels per board, totaling 16 channels, all in use.

The power cuts were the main issue during commissioning and first runs, resulting in an average of up to 10 channels not working after each event. Part of the affected channels could be repaired, resulting in only 0.2 to 0.5% of unrecoverable channels from the total of 1240. It is very important to emphasise that all repairs were realized without delaying operations.

IV. ECAL HV

Running on four computers in order to reduce the Central Processing Unit (CPU) load, the HV application is fully implemented to support ECAL. It controls CAEN crates, by switching ON/OFF specific sets of channels, configures output voltage setpoints with SM/Dee granularity and troubleshoots and monitors CAEN hardware.

Figure 4 shows the panel used to configure and monitor HV settings at the SM level.

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V. ECAL LV

Running on three computers (2 for the barrel and 1 for the endcaps) in order to reduce the CPU load, the LV application is fully implemented to support ECAL. It controls WIENER crates by configuring output voltage setpoints with SM/Dee
granularity, troubleshoots and monitors the WIENER hardware.

The LV panel used to configure and monitor LV settings at the SM level is displayed in Figure 5.

![Figure 5: SM LV panel](image)

The final barrel hardware configuration consists of 108 crates (3 crates per SM), with 6 to 7 channels per crate and 4 TT (trigger towers) per channel. The endcaps hardware consists of 28 crates (7 crates per Dee), with 6 to 7 channels per crate and 4 SC (super crystals) per channel. The total number of channels used for the LV system is 860, where 684 are for the barrel and 176 for the endcaps.

During the commissioning and first operations all hardware problems were fixed with minimum delay to the operations.

VI. ECAL DCU

DCUs are ADC based microcontroller chips used to monitor on-detector electronics; basically, they provide measurements of supply voltages, APD leakage currents and temperatures (more than 2000 parameters per SM/Dee).

The DCU readout is implemented via regular DAQ channels in a shared mode using dedicated timeslots for data transmission. All DCU data then goes directly to the CMS conditions database.

In order to have DCU data in DCS a software connection between DAQ and DCS has been implemented which is based on the JCOP PSX SOAP service (Figure 6).

![Figure 6: Software connection between DAQ and DCS](image)

The biggest challenge for the DCU DCS application was to present in a compact way (Figure 7) an enormous amount of information (the DCU information volume is ~10 times bigger than the one of all other ECAL DCS subsystems). This was achieved based on the experience of the ECAL DAQ team in data quality monitoring (DQM).

![Figure 7: DCU panel](image)

All problems during the commissioning phase, most of them concerning database access and configuration, were successfully solved.

VII. ECAL PTM/HM

This system monitors temperatures and humidity inside the ECAL detector (relative temperature measurement precision is approximately 0.01°C, in order to monitor the cooling system and provide precise information for physics data processing). It is designed to have its own readout chain (probes, electronics, cabling and computing), completely separated from the ECAL DAQ readout. The PTM/HM provides non-stop monitoring even during CMS shutdowns.

Warnings and alarms are generated and propagated to the ECAL Supervisor to shutdown LV/HV, when over-temperature or high humidity conditions (SM/Dee granularity) are detected.

The application is about to be fully integrated into the CMS DCS and runs stable since the very beginning of operations in the CMS cavern.

During commissioning it became apparent that the temperature monitoring could be used to check the LV status of SMs and Dees by comparing the difference in temperature of the input and output water. This feature was implemented (Figure 8) and has been used as an extra resource by experts to support operations.
The remaining relevant issues concerning this subsystem are the migration to the CMS conditions database, as at the moment all data is stored in local data files, and the design and implementation of further services for equipment troubleshooting.

VIII. ECAL ESS

Designed to be fully autonomous and radiation tolerant[10], the ESS monitors the air temperature around the SM/Dees electronics with precision better than 0.1°C, detects water leaks inside SM/Dees and in the LV racks and issues reliable interlocks to ECAL subsystems in case of unsafe conditions.

The panel displayed in Figure 9 shows all relevant parameters in a SM/endcap quadrant level, such as temperatures, warning and alarm levels, interlock status, as well as the ESS PLC and CMS Detector Safety System (DSS) status.

The most significant experience during one of the global runs was a problem related to the main power supply to the main UPS system, which triggered a CMS DSS shutdown signal to ESS. The safety system took correct actions by shutting down safely all ECAL subsystems.

Currently the main issue, still under investigation, is related to two Siemens communication modules CP 341 that became defective during commissioning.

IX. CONCLUSIONS

DCS has supported the entire ECAL (barrel and endcaps) since it has been installed and cabled. So far there were no periods of DCS unavailability and delays in the ECAL commissioning due to DCS related problems.

Power cuts were responsible for most of the problems concerning the hardware during commissioning and affected in general all subsystems. All problems induced by these events were handled in such a way that there was no significant interruption in ECAL operations.

The rather smooth DCS services extension in terms of scaling and functionality has been made possible due to several development workbenches, where applications could be tested before moving to the final system. However, it was not possible to reproduce the actual scale and exact configuration (CMS networks, database servers, etc) and therefore developers faced many challenges “in the field”, such as considerable time spent to get the software interface DCS-DAQ running in stable manner and to provide a connection between the ECAL cooling system and DCS cooling monitoring application. The ECAL Supervisor was modified many times according to new demands from ECAL operation.

Summarizing, despite many obstacles and problems which seem natural for such a huge scale installation as CMS, ECAL DCS has demonstrated a reliable and always available support for ECAL commissioning and operation.

X. REFERENCES


The Common Infrastructure Control of the ATLAS experiment

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Abstract – ATLAS is one of the experiments at the Large Hadron Collider (LHC), constructed to study proton-proton collisions at the unprecedented energy of 14 TeV. In order to guarantee efficient and safe operation of the ATLAS detector, an advanced Detector Control System (DCS) has been implemented. With more than 150 PCs, the DCS is a highly distributed system, hierarchically organized for operating the detector. An important role is played by the Common Infrastructure Control (CIC), supervising the experimental area. The CIC provides monitoring and control for all common services and for the environment in the cavern and in the counting rooms. Distributed I/O concentrators, called Embedded Local Monitor Boards (ELMB), have been developed to operate under the special conditions of the experiment such as strong magnetic field and ionizing radiation. They are used for a variety of applications and are geographically distributed over the whole experiment. The communication is handled via the Controller Area Network (CAN) fieldbus using the CANopen protocol. Information and high level control is available to the users by a Finite State Machine (FSM) software running in the control room and information is also displayed on the web. The technical infrastructure of ATLAS has continuously been supervised during the commissioning phase by the CIC and ensures safe operation.

I. THE BE OF THE DCS

The DCS has the task to permit coherent and safe operation of ATLAS and to serve as a homogenous interface to all sub-detectors and to the technical infrastructure of the experiment. The DCS must be able to bring the detector into any desired operational state, to continuously monitor and archive the operational parameters, to signal any abnormal behavior to the operator, and to allow manual or automatic actions to be taken.

The DCS uses the SCADA product PVSS II 3.6 [3], a device-oriented and event-driven control system which can be distributed over a large number of PCs running Windows or Linux as operating system. Four main concepts of PVSS make it suitable for a large scale control system implementation such as the ATLAS DCS:

- A control station (PC) runs a so-called “Project” which contains a number of processes, called “Managers”. Different types of Managers may be used depending upon the type of application the Project is being used for, therefore avoiding unnecessary overhead.
- Each PVSS Project uses a central database for all current data values, stored in objects called “Data Points” (DP). All Managers have full Oracle database access for which PVSS provides transparent synchronization. Data processing is performed in an event-based approach using multithreaded callback routines upon value changes.
- Different Projects can be connected via LAN to form a “Distributed System” allowing to remotely access the databases and events of all connected Projects. This provides scalability up to the full size of ATLAS.
- A generic API allows extending the functionality of control applications using additional software components.

Due to the enormous size and complexity of detector and the large amount of data to be monitored, the full BE hierarchy of the DCS, from the operator interface down to the level of individual devices, is represented by a distributed Finite State Machine mechanism allowing for standardized operation and error handling in each functional layer [4]. Each functional part is represented in the FSM by a “Device Unit” (DU), attributing a “State” of operation and a “Status” reflecting an anomaly. The BE is organized in three layers (see Fig. 1): the Local Control Stations (LCS) for process control of subsystems, the Sub-detector Control Stations (SCS) for high-level control of a sub-detector allowing stand-
alone operation, and the Global Control Stations (GCS) with server applications and human interfaces in the ATLAS control room for the overall operation.

Efficient error recognition and handling for each DP is provided by a centralized alarm system which raises alarms at the granularity of the individual FE devices and propagates these alarms within the FSM hierarchy.

In order to synchronize the state of the detector with the operation of the physics data acquisition system, bi-directional communication between DCS and run control is provided.

The Joint Controls Project (JCOP) [5] was founded in order to maximize synergy effects for the DCS of the four experiments at the LHC by using common DCS components. Within JCOP, standards for the use of DCS hardware were established and a commercial controls software product has been selected to serve as the basis for all DCS applications. This software package was substantially extended by a comprehensive framework of software components and implementation policies.

II. THE CIC CONTROL SYSTEM

All parts of ATLAS which are common to the experiment are supervised by the CIC and the External Systems as shown in Fig. 2. The architecture is also reflected in the FSM.

The CIC is part of the ATLAS FSM like a sub detector and reflects the “State/Status” of the cooling, the environment and of the 5 counting rooms, for the control of the racks and the power supplies. The information is relevant for the users in the ACR and on dedicated WebPages [6], thus allowing the monitoring of the hardware equipment.

The CIC comprises 6 Control Stations, measuring in total about 5000 Data Points Elements via CAN buses using the CANopen protocol [7]. A Control Station includes 2 Intel Xeon processors (3 GHz), 2 disks (250GB each), 2GB RAM, an Intelligent Platform Management Interface (IPMI) for remote control and has 3 PCI slots for CAN interface boards.

A. A read-out chain based on the ELMB

There are essentially two categories of Front-End devices: commercial systems like power supplies and Embedded Local Monitor Board, which is a purpose-built flexible I/O system. The ELMB resists to the magnetic fields and is radiation tolerant. It has been developed in order to achieve as much homogeneity in the interfacing of various types of sensors and therefore to save development effort and ease maintenance.

The ELMB is separated in three powering sections. The CAN bus cables for the CIC are composed of 2 wires for the signals, 4 wires to provide 2 sources of 12V – Analog/Digital and CAN power – and 1 wire for the grounding. It has 64 analogue input channels of 16-bit resolution, 24 digital input/output lines and a serial bus to connect further I/O devices.

The front side of the ELMB motherboard is occupied by connectors for the CAN bus, digital I/O, analog inputs. The back side carries the ELMB and has sockets for signal conditioning adapters for all 64 analog input channels (see Fig. 3). Adapters for different sensors, for example NTC, 2-wire PT1000 or 4-wire PT100, are available. With these adapters sensors can be directly connected to the motherboard. More details can be found in [8].
(Premium) which control local PLCs (Twido). Commands can be sent to act on the powering of the racks.

The racks in the experimental area are equipped with a Turbine Unit to ventilate and cool the air. A special monitoring board using the ELMB has been developed and is placed in the Turbine Unit [9] to read out about 20 parameters, like Temperatures, Humidity, Dew Point, Turbine currents... Additional sensors for specific needs (i.e. temperature sensor, leak detection system...) can easily be interfaced. The turbines placed in the cavern are especially designed to tolerate magnetic field.

The racks in the TDAQ counting rooms, housing computers for data taking are cooled with fans and heat exchangers placed on the rear doors.

The FSM displays the State of operation and the Status reflecting any abnormal parameter at different levels. The operator interface allows visualizing the State/Status of a counting room up to an individual rack represented by a DU. The panel for a rack displays the parameters measured and the equipment it houses. One can also obtain the trend of a chosen parameter; an illustration in shown in Fig. 4.

![Figure 4: CIC Rack Control operator screen in USA15 Level1](image)

### C. Cavern and Counting Room Environment

In each of the 5 counting rooms, sensors are installed to supervise the ambient conditions (temperature, humidity and pressure) and the cooling system (see Fig. 5).

![Figure 5: Ambient Environment panel in USA15 Level1](image)

The general environment in the experimental cavern is also supervised. Ambient parameters are read out at several locations and a network of CAN buses with about 90 ELMB nodes, which covers the whole volume of the experiment, has been deployed. About one third of the 8000 channels are presently used, the rest are foreseen for future upgrades.

More than hundred PT100 probes have been placed on the aluminum structures of the detector. These sensors and their connections are designed to be able to localize and assess major accidents, e.g. a fire or a cryogenic leak.

The level of radiation inside ATLAS needs to be continuously monitored. About 60 radiation sensors [10] are installed just outside of the calorimeter and on the Muon detectors. Their FE electronics is also read out by the ELMB.

### III. THE EXTERNAL SYSTEMS

#### A. Infrastructure Services

The data exchange between the ATLAS DCS and external control systems is handled via the Data Interchange Protocol (DIP). This protocol is a thin layer on top of the Distributed Information Management (DIM) process communication interface [11] designed for highly reliable event-based data transfer. A DIP server publishes data items to a dedicated name server, while a client process can fetch the server publication information from the name server and can subscribe at the DIP server to selected data items, resulting in an event-triggered, pushed data transfer from the server to the client.

All external control systems are interfaced to the ATLAS DCS using a dedicated DCS Information Server in the GCS layer (see Fig. 1). Information from the external systems is transferred via DIP into the IS PVSS Project, thus made available to all DCS stations within the Distributed System, and stored in the PVSS Oracle database. A generic error handling mechanism using the DIP quality monitoring facilities has been implemented for all subscriptions on the DCS IS signaling any error condition related to the DIP communication via the PVSS alarm system.

The external systems are:

1) **Cooling and Ventilation (CaV)**

Cooling and ventilation is an infrastructure service provided by CERN. A primary water cooling plant is installed at the ATLAS site on the surface. It provides cooling to secondary plants underground, which cool the racks, equipment like vacuum pumps, cables or sub-detector specific equipments. The operational parameters of each of these secondary plants are read out by the respective sub-detector. In addition, the CIC monitors the overall status of the primary and all secondary cooling plants. The ventilation system for the underground rooms and the cavern is operated autonomously and its status will be transmitted to the DCS IS.

2) **Electricity Distribution**

The electricity distribution system as part of the CERN infrastructure is supervised by a dedicated control system. The part relevant for ATLAS (e.g. distribution cabinets, switch boards, UPS systems) is also monitored by the DCS.
3) Gas systems

Each of the gas systems of the different sub-detectors is controlled by a dedicated PLC. All PLCs are supervised by one PVSS system, which is not part of the ATLAS distributed control system. The operational parameters are published by DIP and the DCS IS transfers them into PVSS data points for further distribution to the sub-detectors. The relevant sub-detector control project sets up a FSM hierarchy for its gas system and includes it in its sub-detector tree.

4) Magnets and Cryogenics

The ATLAS magnets and cryogenics systems are also controlled by dedicated PLCs and monitored by a stand-alone PVSS station and information is retrieved via DIP to the DCS. The systems are represented in the CIC FSM hierarchy including corresponding status panels. All infrastructure parameters are available to the sub-detector applications.

5) LHC parameters

The interaction by software between ATLAS and the LHC is handled by DCS. Dedicated instrumentation on both sides provides detailed information about luminosity and backgrounds via the DIP protocol. The state of the LHC accelerator is presented to the ATLAS operator by the DCS. A Beam Interlock System (BIS) combines signals in ATLAS indicating high backgrounds, and in case of danger for the detector sends a hardware interlock signal to LHC in order to dump the beams. The status of the BIS is presented by the CIC as an FSM unit.

B. The FPIAA system

The experimental area is accessible in periods without beam. As the volumes are often quite small, confined and interconnected in a very complex way, a dedicated system called Finding Persons Inside ATLAS Area (FPIAA) [12] has been developed in order to be able to track people inside the ATLAS cavern, e.g. during detector maintenance periods. It is based on 800 passive infrared sensors that detect the movement of people. These signals are analyzed in real time and in case of an abnormal situation of a person not moving for a too long time, a PVSS alarm is generated. The synoptic panel of the FPIAA system (Fig. 6) allows the operator in the control room to know if and where people are in the cavern.

C. The Detector Safety System

The Detector Safety System (DSS) [13] has the task to detect possibly dangerous situations for the detector e.g. due to overheating, failure of services, etc. and to shut down the relevant detector automatically. It is based on redundant PLCs which drive hardware interlocks and is supervised by a stand-alone PVSS system. All alarms of DSS are transmitted to DCS. DSS actions can be delayed in order to enable DCS to execute shut-down procedures in a controlled way before DSS switches off the equipment.

CONCLUSIONS

During the ongoing commissioning, it was proven that the Common Infrastructure Control system, with notably the Rack Control application, is able to continuously provide stable control and supervision of the experimental area. The use of the standardized read-out chain based on ELMB and PVSS has the advantage to facilitate long-term maintainability. The monitoring and control of the common infrastructure is provided by a Finite State Machine mechanism, which effectively reduces the complex set of FE component states to a single overall state.

Information is displayed in the ACR on the main FSM and on the Alert Screen. There are permanently a DCS shifter and a Shift Leader in Matters of Safety (SLIMOS) in the control room in charge of the supervision of the infrastructure.

To have remotely an overview of the state of the ATLAS Infrastructure and to give access to this data to everyone, Web pages are displaying the main information on the Internet. At the time of writing this paper, the control of the common Infrastructure is integrated within the overall DCS and is ready for the start-up of the LHC.

REFERENCES

Digital part of PARISROC: a photomultiplier array readout chip

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Abstract

PARISROC is the front end ASIC designed to read 16 PMT for neutrino experiments. It’s able to shape, discriminate, convert and readout data in an autonomous mode. The digital part manages each channel independently thanks to 4 modules: top manager, acquisition, conversion and readout. Acquisition is in charge to manage the SCA with a depth of 2 for charge and fine time measurement. Coarse time measurement is made with a 24 bits gray counter. Readout module sends converted data of hit channels to an external system. Top manager controls the start and stop of the 3 others modules. The ASIC was submitted in June 2008.

I. GENERAL OVERVIEW

A. Experiment overview

PARISROC (Photomultiplier ARray Integrated in Sige ReadOut Chip) is the front end ASIC designed for the PMM2 R&D project dedicated to neutrino experiments [1]. This project is funded by the French National Agency for Research under the reference ANR-06-BLAN-0186.

Next generation of neutrino experiments which will take place in megaton size water tanks will require very large surface of photodetection and volume of data [2]. For the funded project, this large surface of photodetection is segmented in macro pixels made of 16 PhotoMultiplier Tubes (PMT) connected to an autonomous front end ASIC: PARISROC. A module with 16 PMT is shown in Figure 1.

![16 PMT module](image1)

Figure 1: 16 PMT module

B. ASIC overview

PARISROC is able to read 16 PMT. It’s a triggerless chip and can work in an autonomous mode [3]. The block diagram of the ASIC is given after in Figure 2.

![Block diagram of PARISROC](image2)

Figure 2: Block diagram of PARISROC

It allows time tagging and charge measurement. Time tagging is composed of a coarse and a fine time measurement. Coarse time is handled by a 24 bits counter at 10 MHz and fine time by a 12 bits TDC ramp. The main characteristics of the ASIC are in table 1 below.

<table>
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<tr>
<th>Parameter</th>
<th>Value</th>
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<tr>
<td>Technology</td>
<td>Austria-Micro-Systems (AMS)</td>
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<td>Power Supply</td>
<td>3.3 V</td>
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Table 1: Main characteristics

C. Overview of the digital part

The digital part of PARISROC is built around 4 modules which are acquisition, conversion, readout and top manager. Actually, PARISROC is based on 2 memories: during acquisition, discriminated analog signals are stored into an analog memory (the SCA: switched capacitor array). The analog to digital conversion module converts analog charges...
and times from SCA into 12 bits digital values. These digital values are saved into registers (RAM). At the end of the cycle, the RAM is readout to an external system. A simple view of operation is shown on Figure 3.

![Figure 3: High level operation](image)

## II. ASIC DESCRIPTION

### A. Low level block diagram

The low level block diagram of the ASIC is given below in Figure 4.

![Figure 4: Low level block diagram](image)

The 16 channels of PARISROC are managed independently, 2 state machines are dedicated to handle one channel: 1 for write pointer and 1 for read pointer. Besides, 32 registers of 24 bits are needed to save coarse time for each depth of SCA. We can consider that the SCA of one channel is controlled as an analog FIFO.

Conversion is common for all channels and needs 32 registers of 12 bits to store converted data: 16 for charges and 16 for fine time measures.

As the readout will only treat hit channels, this module will tag each frame with its channel number.

### B. Detail of one SCA channel

The chip has 16 channels. Each channel has a depth of 2 for charge and 2 for fine time storage. The SCA column is selected, read and erased by the digital part. The detail of 1 SCA channel is shown below in Figure 5.

![Figure 5: Detail of 1 SCA channel](image)

“Track & Hold Cell” allows to lock the capacitor value only when a calibrated trigger occurs within the selected column. This operation is given below in Figure 6.

![Figure 6: Operation of T&H cell](image)

Detailed description is shown in Figure 7.

![Figure 7: Detailed description of T&H cell](image)

## III. MODULES OF THE DIGITAL PART

### A. The Top Manager

The top manager module controls the 3 others ones. It allows to start and to stop them in order to realize the right sequence for an autonomous working.

When 1 channel is hit, the top manager waits for a constant time to allow triggers on others channels. Then, it...
starts ADC conversion and readout of digitized data. The maximum cycle length is about 200µs when all channels are hit.

During conversion and readout, acquisition is never stopped. That’s mean that discriminated analog signals can be stored in the SCA at any time of the sequence if SCA is not full. This operation mode is managed by the state machine given in Figure 8.

![Diagram](image)

Figure 8: Top manager state machine

**B. Acquisition**

This module is dedicated to charge and time measurements. It manages the SCA where charge and fine time are stored as a voltage. It also integrates the coarse time measurement thanks to a 24 bits gray counter with a resolution of 100 ns.

Each channel has a depth of 2 for the SCA and they are managed individually. Besides, SCA is treated like a FIFO memory: analog voltage can be written, read and erased from the memory. The acquisition block diagram is given below in Figure 9.

![Diagram](image)

Figure 9: Acquisition module

Analog FIFO memory for one channel is managed by 2 state machines: 1 for write/erase and 1 for read operation. The state machines are shown in Figure 10 and 11.

**C. Conversion**

The main purpose of this module is to convert analog values stored in the SCA in digital ones thanks to a 12-bit Wilkinson ADC. The ADC clock frequency is 40 MHz, it implies a maximum ADC conversion time of 103 µs.

Each ADC run converts the fine time and the charge of each channel even if it was not hit: 32 conversions in 1 run. Only the data of hit channel will be treated by the readout module. The block diagram is given after in Figure 12.

![Diagram](image)

Figure 12: Conversion module

**D. Readout**

The Readout module, shown in Figure 13, permits to empty the registers. It works as a selective readout: only hit channels are transferred. In the case of all channels hit, about 832 bits of data are transferred to the concentrator with a 10 MHz clock.
The pattern used is composed of 4 data: 4-bit channel number, 24-bit coarse time, 12-bit charge and 12-bit fine time. Each data is coded in gray and the length of one frame is 52 bits.

When all channels are hit, the readout takes about 100 µs: the time between 2 frames is about 1 µs.

![Figure 13: Readout module](image)

IV. DIGITAL PART LAYOUT

The layout of the digital part was realized in 0.35 µm technology from Austria Micro System (AMS) [4] and designed with Soc Encounter from CADENCE.

The layout is on 3 metals (blue, red and green) and its size is 1800 µm by 1000 µm.

The layout is composed by 10K standard cells (equivalent to 71K transistors).

It integrates 1152 memory registers and has a total net length of 1 meter. It’s given in Figure 14.

![Figure 14: Digital part layout](image)

V. CONCLUSION

PARISROC is a complete triggerless and autonomous ASIC for the PMM2 experiment. It was submitted in June 2008 and the first results are expected at the end of the year.

Digital part has many features included to manage the entire chip for acquisition, conversion and readout. As the acquisition module is completely new in order to have all channels independent, many tests will be performed on this new structure.

VI. REFERENCES

Instrumentation for Gate Current Noise Measurements on sub-100 nm MOS Transistors

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Abstract

This work describes a measuring system that was developed to characterize the gate current noise performances of CMOS devices with minimum feature size in the 100 nm span. These devices play an essential role in the design of present day mixed-signal integrated circuits, because of the advantages associated with the scaling process. The reduction in the gate oxide thickness brought about by CMOS technology downsizing leads to a non-negligible gate current due to direct tunneling phenomena; this current represents a noise source which requires an accurate characterization for optimum analog design. In this paper, two instruments able to perform measurements in two different ranges of gate current values will be discussed. Some of the results of gate current noise characterization will also be presented.

I. INTRODUCTION

In the last decade, the requirements of high granularity in the design of the readout electronics for HEP experiments have led to an extensive use of deep-submicron CMOS processes. While approaching the 100 nm span, the CMOS technology has entered the sub-3 nm gate oxide thickness regime. In such a regime, MOSFET devices exhibit a non-negligible gate-leakage current, due to the finite probability of electrons directly tunneling through the insulating $SiO_2$ layer [1].

As an example, Fig. 1 shows the gate current density for NMOS devices belonging to two CMOS processes with 90 nm and 130 nm feature size; in the 90 nm process the leakage current is about 2-3 orders of magnitude higher than in the 130 nm process. This leakage current, which originates from discrete charges randomly crossing a potential barrier, is affected by noise fluctuations which may degrade circuit performance in analog applications.

In particular, in solid state detector readout circuits integrated in sub-100 nm CMOS technologies, the resolution, which is limited by the noise from the input transistor of the charge sensitive amplifier, may be degraded by the parallel noise source in the device gate current. In order to evaluate the effects of this noise contribution on the resolution of readout circuits, and to supply suitable design criteria for IC designers, accurate characterization and modeling of gate current noise are mandatory.

In this work, the noise characterization is carried out by means of purposely developed instrumentation with the required accuracy in a frequency range large enough to include both white and 1/f or Lorentzian-like components, considering the dependence of the gate current from device geometry and bias conditions. This measuring instrument consists mainly of a transimpedance stage amplifying the noise in the DUT (device under test) gate-leakage current, which is converted into a voltage signal integrated circuits, because of the advantages associated with CMOS technology downscaling leads to a non-negligible gate current due to direct tunneling phenomena; this current represents a noise source which requires an accurate characterization for optimum analog design. In this paper, two instruments able to perform measurements in two different ranges of gate current values will be discussed. Some of the results of gate current noise characterization will also be presented.

II. GATE-LEAKAGE CURRENT NOISE

In MOS devices with ultrathin gate oxide thickness, direct tunneling appears to be the dominant mechanism of gate-leakage current. This current can be divided into three major contributions [2]: the gate-to-inverted channel current ($I_{g_{ce}}$), the...
gate-to-source ($I_{gs}$) and the gate-to-drain ($I_{gd}$) components due to the path through the source and drain overlap regions. The gate-leakage current noise performances of a CMOS device can be characterized in terms of the gate noise current spectrum, which can be modeled by means of the equation [3]:

$$S^2_P = S^2_W + \frac{A_{fg}}{f^{\alpha_{fg}}}$$

(1)

The first term in (1) describes the white noise component of the spectrum while the second one is given by flicker noise, where $A_{fg}$ is a power coefficient of the $1/f$ noise while $\alpha_{fg}$ determines the slope of this low frequency noise contribution. The term $S^2_W$ in (1) can be expressed by means of the well known shot noise law [4]:

$$S^2_W = 2qI_G$$

(2)

where $I_G$ is the sum of the absolute values of each gate current contribution for a given bias condition.

III. INSTRUMENTATION FOR NOISE MEASUREMENTS

In this section two interface circuits used to perform noise measurements will be presented. These circuits have been designed with different resolution on the basis of the expected noise level for a given gate current of the DUT.

![Figure 2: system for the noise measurements.](image)

The driving criterion in the design of the amplification systems was the minimization of their input-referred noise with respect to the current noise of the DUT, $S_{I,DUT}$. Noise measurements are performed by means of the system described in Fig. 2. The noise in the gate current of the DUT is converted into a voltage by means of a low noise transimpedance amplifier, and then detected by a commercial network/spectrum analyzer. The test signal source of the analyzer is applied, through the resistor $R_F$ and the switch $S$, to the input of the interface circuit, in order to evaluate the transfer function of the measuring system. The transfer function is obtained by applying a voltage signal, converted into a current signal by means of the resistor $R_{FDT}$ shunted to the amplifier input virtual ground. The equivalent input noise current spectrum is calculated by dividing the output noise spectral density by the measured transfer function and taking into account the value of the resistor $R_{FDT}$. By means of gate and drain bias circuits it is possible to obtain different bias conditions and gate current contributions and make one of these components dominant with respect to the others.

A. Interface circuit for high DUT gate currents

Noise measurements at high gate current values (from hundreds of nanoamps to few microamps) can be performed by means of the interface circuit shown in Fig. 3.

![Figure 3: high-gate-current interface circuit.](image)

The voltages $V_D$ and $V_G$ are applied respectively to the drain of the DUT and to the resistor $R_G$, used to regulate the voltage at the gate of the device. By adjusting $V_D$ and $V_G$ it is possible to obtain the desired device bias conditions. The value of feedback resistor $R_F$ and bias resistor $R_G$ has been chosen taking into account the value of the static gate current of the DUT and the expected noise level for that current. Actually, $R_F$ and $R_G$ provide the main noise contribution to the overall system performances. The value of the gate current can be obtained by measuring the voltage drop across the $R_G$ resistor. $C_I$ is a decoupling capacitor, while $C_F$ has been introduced to avoid resonance peaks in the circuit response and $C_D$ includes the input capacitance of the amplifier and parasitics from the PCB. High gain all over the frequency range is also needed to overcome the noise of the spectrum analyzer. The frequency response of the system can be expressed by means of the following equation:

$$G(j\omega) = \frac{R_F}{1 + j\omega R_F C_F}.$$
A noise analysis of the measuring system can be carried out considering the main noise sources, shown in Fig. 5, where $S_{I,RF}$ and $S_{I,RG}$ are current noise sources relevant to the thermal noise of the $R_F$ and $R_G$ resistors, while $S_{I,OP}$ and $S_{V,OP}$ are the equivalent input noise sources of the amplifier.

![Figure 5: transimpedance stage with the main noise sources.](image)

The noise of the measuring system can then be modeled by means of an equivalent input current noise source, whose power spectral density is given by the following equation:

$$S_{SYS}^2(\omega) = 4kT \left( \frac{1}{R_F//R_G} \right) + S_{I,OP}^2(\omega) +$$

$$S_{V,OP}^2 \left( \frac{1}{R_F//R_G} \right)^2 \cdot$$

$$1 + \left[ \omega \left( \frac{R_F R_G}{R_F + R_G} \right) (C_D + C_F) \right]^2,$$

where $k$ is the Boltzmann’s constant and $T$ the absolute temperature. Expression (4) can be minimized choosing high value resistors; the choice for the operational amplifier used in the transimpedance stage has been dictated by its performances in terms of parallel input-noise $S_{I,OP}$.

![Figure 6: input-referred noise contribution of the amplifier, and calculated contributions.](image)

Fig. 6 shows the measured input-referred noise of the interface circuit, and the theoretical noise contributions calculated by means of (4), for an estimated $C_D$ of 25 pF. Considering that $S_{I,OP} = 1.5 \, fA/\sqrt{Hz}$, and neglecting the series noise contribution from the operational amplifier, which has an impact on the resolution only at frequencies higher than 100 kHz, the total input noise of the interface system is mainly due to resistors $R_F$ and $R_G$. Assuming that minimum gate-leakage current noise for the DUT can be expressed by means of (2), it is possible to determine the value $I_{G,min}$ for the gate current which leads to a signal to noise ratio ($S_{I,DUT}^2/S_{SYS}^2$) equal to unity:

$$I_{G,min} \approx \frac{4kT}{2q} \left( \frac{1}{R_F + R_G} \right).$$

With the values used for $R_F$ and $R_G$, $I_{G,min} = 52 \, nA$.

**B. Interface circuit for low DUT gate currents**

Measurements of noise spectral density arising from smaller currents, can be carried out by decreasing the noise contributions in the interface circuit. A solution which suitably improves the noise performance of the amplifying system is described in Fig. 7. The main difference with respect to the schematic of Fig. 3 lies in the absence of the gate-biasing resistor $R_G$, which leads to a significant noise reduction in the interface amplifier. In particular, the dominant noise source in this configuration is represented only by the feedback resistor $R_F$. Adopting a 100 MΩ resistor, it is possible to measure the noise arising from a minimum gate-leakage current in the order of few nanoamps, as highlighted in Fig. 8, where the signal-to-noise ratio is represented as a function of the gate-leakage current. DUT biasing is done by means of the voltage $V_G$ applied to the non-inverting input of the transimpedance amplifier and the voltage $V_D$ applied to the drain of the DUT.
At low gate current, the noise at the output of the transimpedance amplifier requires an additional gain stage in order to overcome the noise of the spectrum analyzer; in particular, a 40 dB gain stage has been included in the circuit. Resistor $R_0$ and capacitor $C_0$ perform the high-pass filtering action needed to decouple the two stages of the circuit. Adequate values for these components were chosen in order to obtain an extremely low cut-off frequency. Stray capacitor $C_A$ in parallel with resistor $R_A$ introduces an high-frequency pole in the frequency response of the system. The value of the feedback resistor $R_F$ of the transimpedance amplifier has to be chosen as a compromise between the noise performance of the measuring system and the range of the gate current values in the DUT, which is limited by the output dynamic range of the amplifier. Fig. 9 shows the good agreement between measured and theoretical frequency response, which can be calculated as follows:

$$G(j \omega) = \frac{R_F}{1 + j(\omega R_F C_F)} \left( 1 + \frac{R_A}{R_B} \right) \frac{1 + j\omega \left( \frac{R_A R_B}{R_A + R_B} \right) C_A}{1 + j \omega R_A C_A}.$$  \hspace{1cm} (6)
This low-frequency noise exhibits a quadratic dependence on the gate current [5]. For devices belonging to the 130 nm process the $1/f$ noise component of the spectrum is not clearly visible at 1 Hz as shown in Fig. 11a, while the white noise contribution confirm the good accuracy of the model for the theoretical behavior expressed by (2). In order to detect $1/f$ contribution it has been necessary to perform measurements from lower frequencies, as shown in Fig. 11c, relevant to a gate current smaller than 1 nA. As it can be seen in the presented spectra, white and $1/f$ noise increase by increasing the gate current; moreover, at a fixed current, white noise seems to be almost independent of the gate geometry. Some devices exhibited Lorentzian-like noise behavior, as shown in Fig. 11d).

V. CONCLUSION

This paper described a laboratory instrument for gate-leakage current noise measurements that is an effective tool for the characterization of CMOS devices with oxide thickness in the 2-nm span. In the frequency range used for the presented results, it was possible to fully characterize the noise behavior of the DUTs. Measuring the $1/f$ noise component in extremely low gate currents (a few nanoamps or less) requires measuring the DUT noise spectrum from very low frequencies as the flicker term rapidly decreases with the gate-leakage current. With this instrumentation it is possible to carry out a complete characterization of the technologies used in the design of low-noise charge sensitive amplifiers, where the gate-leakage current can represent a limit in the achievable resolution.

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Control, Test and Monitoring Software Framework for the ATLAS Level-1 Calorimeter Trigger


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Abstract

The ATLAS first-level calorimeter trigger is a hardware-based system designed to identify high-$p_T$ jets, electron/photon and tau candidates and to measure total and missing $E_T$ in the ATLAS calorimeters. The complete trigger system consists of over 300 custom designed VME modules of varying complexity. These modules are based around FPGAs or ASICs with many configurable parameters, both to initialize the system with correct calibrations and timings and to allow flexibility in the trigger algorithms. The control, testing and monitoring of these modules requires a comprehensive, but well-designed and modular, software framework, which we will describe in this paper.

I. INTRODUCTION

The ATLAS[1] detector at the CERN Large Hadron Collider (LHC) consists of an inner tracker surrounded by electromagnetic (EM) and hadronic calorimeters enclosed by a muon spectrometer. The calorimeters provide the trigger with just over 7200 analogue signals.

The first-level calorimeter trigger[2] (L1Calo) is a hardware-based system with a high degree of adaptability provided by widespread use of FPGAs to implement the trigger algorithms that identify high-$p_T$ jets, electron/photon and tau candidates and which measure total and missing $E_T$ seen in the calorimeters.

The real-time path of the L1Calo trigger (see figure 1) is subdivided into a Preprocessor which digitizes the analogue signals from the calorimeters, followed by two digital processor systems working in parallel: the Jet/Energy-sum processor (JEP) and the Cluster Processor (CP). The outputs of the digital processor are sent to the ATLAS Central Trigger Processor. All stages of the L1Calo processor chain are read out to the data acquisition for monitoring the operation of the trigger.

The system comprises over 300 VME modules of about 10 different types, each of which has a unique register and memory map. The most complex of these modules contains around 2000 individually programmable registers, as well as many kilobytes of look-up table memory.

It is clear that the software needed to control a system on this scale needs to be sophisticated enough to manage the different properties of each module, but also modular enough to be maintainable over the long period of commissioning and running of the ATLAS experiment.

There are several distinct areas of software that can be clearly separated, but which must have some means of interaction. For example, the configuration parameters must be stored.
in a common database framework which is independent of the rest of the software, but many of the other software components (e.g., configuration, monitoring) will need access to this information. The software framework must also fit into the existing ATLAS online software environment to successfully participate in a standard integrated run.

The following sections give an overview of the software architecture and provide details of the design choices and implementations of the main components.

II. L1Calo Online Software Architecture

The L1Calo online software is designed to control, test and monitor any configurable subset of the trigger system, from a single module under test to the complete installation at ATLAS. The L1Calo software is primarily written in C++ with some Java libraries included. It consists of about 75 software packages in our code repository (CVS), built together using the standard ATLAS code management tool (CMT). These packages are grouped into about eight main categories whose internal and external dependencies are shown in figure 2.

![L1Calo online software architecture](image)

Figure 2: L1Calo online software architecture.

At the lowest level there is a collection of infrastructure packages that define basic classes, tools and interfaces to external software such as the ATLAS Trigger and Data Acquisition (TDAQ) software[3] and the CERN LHC Computing Grid (LCG) packages. Several database related packages provide a uniform interface between the various ATLAS databases and the higher layers of L1Calo software.

One of the most fundamental areas is the set of underlying VME access libraries that encapsulate the detailed programming models of our modules. They were designed so that they could be used in several ways: under the ATLAS run control to configure modules at run start, from standalone programs or via an interactive GUI for expert intervention at the VME register level. Another large body of the software is dedicated to a detailed simulation of the hardware at the level of data that can be probed at each stage of the trigger processing.

A further group of packages handles the interaction with ATLAS run control and other distributed services. The main module types in the three processors also have dedicated packages for testing the system and for performing calibrations, both of the signal timing and the energy of the input signals. These are based around a common calibration strategy which extends the run concept to encompass multi-step runs, where parameters are adjusted between each step of the run.

Finally, and most recently, a set of libraries dedicated to monitoring and event-by-event analysis has been developed. These are used to ensure that the trigger is operating correctly during normal data taking, immediately flagging up errors, inconsistencies or merely unusual features to the shift crew. The monitoring area also includes packages for various graphical tools and displays.

III. Databases

The L1Calo software needs access to several different databases used in ATLAS.

The TDAQ database describes the hardware and software configuration that is available for data taking. The hardware configuration includes the crates, modules and cables connecting them. This database also contains sets of L1Calo “run types” with the specifications of the test vector configuration to be used for each type of test run. All calibration values and most configuration settings used to load the L1Calo modules are stored in a COOL database which provides “interval of validity” history of the settings. The trigger thresholds are taken from the ATLAS trigger configuration database, which is a purely relational database. Volatile information for the current run is also read from the TDAQ distributed information service (IS).

L1Calo database packages provide read (and where required, write) access to these databases. The details are encapsulated and each type of module in the system has its own database subclass that provides it with the view of the data it requires.

In addition to custom code for L1Calo, we have also developed a browser and “editor”, ACE, for the LCG COOL database. This is now distributed as part of the LCG software.

IV. Hardware Access and Diagnostics

The design philosophy of our hardware access packages addresses a number of requirements. It needs to provide complete low level access to our VME modules for debugging and it should also implement a well defined access for higher level code. Each type of module in the system has its own programming model, i.e. the sets of registers and memories at the level of the module and its component submodules, some of which
may have their own substructure. The hardware access packages provide complete descriptions of the VME address structure of each module together with bit field formats of each register and memory type. These descriptions, stored in configuration files, are used dynamically in a graphical diagnostic program, HDMC, for debugging down to level of individual register bits. HDMC reads the hardware configuration from the ATLAS TDAQ database so that it can show a complete view of all the modules in one crate.

A code generator uses the configuration files to create classes for use by higher level code. This layered approach means that some access checks can be policed by the compiler – only registers and bits declared in the configuration file can be accessed. Also some common run-time checks can be implemented at a low level. Restrictions on higher level code are not imposed at the expert debugging level.

In addition to the completely generic HDMC display, there is also a dedicated debugging tool for the preprocessor which uses the higher level access code.

V. SIMULATION AND TESTING

The L1Calo project has evolved through phases of “demonstrator” and prototype development, preproduction and production testing to final installation and commissioning in the ATLAS cavern. All those phases require the ability to perform tests on any subset of the trigger system, using arbitrary test vectors. This requirement was met by providing both hardware and software support.

All modules in the real time path provide both playback and spy memories to feed generated data into the system and capture the results at any point in the digital pipeline. A detailed simulation of the system, down to the bit level, was written using VHDL-like software components (processes and ports) that can be connected together to simulate any module or collection of modules.

Figure 3 shows how part of the system may be connected. Any “process” box may itself be a container for a complete set of lower level processes and port connections. The simulation, like the hardware, is configured from the TDAQ database. A generic test is performed by the user selecting suitable test vectors, where to load them and from where to capture the outputs. Bit by bit comparison of the results either verifies the correct operation of the system or else helps to pinpoint errors. The test vectors used can range from simple, complex or random patterns to events from offline simulation or, eventually, from real Physics data.

VI. MONITORING

The ATLAS TDAQ monitoring framework allows whole events or event fragments to be collected from any stage of the readout and dataflow chain. Monitoring clients can obtain events from the monitoring system, decode them and fill histograms that can be published on TDAQ histogramming servers. Any histogram published to any server may then be displayed to the user via a histogram browser, such as the ATLAS Online Histogram Presenter (OHP)[4] which was co-developed by a member of the L1Calo collaboration.

L1Calo has developed a number of programs that use this framework to monitor the operation of each of the three L1Calo subsystems and of the trigger as a whole. These programs provide a large number of histograms for experts to debug problems and a set of summary plots for the shift crew to monitor the behaviour of the system from run to run.

VII. CALIBRATION PROCEDURES

The L1Calo trigger has about 50 configurable parameters for each of its 7200 channels. Many of these are configuration choices, but the majority must be determined from calibrations. The general procedure for performing a calibration is to configure the system as normal using the run control and module libraries, then execute a number of steps changing one selected parameter at each step. The operation mode (“run parameters”) of each type of calibration is defined in the COOL database. The timing parameters for the digital processors (CP and JEP) are determined by scanning clock phases and counting parity errors via VME[5]. However the analogue parameters (pedestals, FADC strobe phase, filter coefficients, latency delays, noise cuts, etc) require data to be read out via the normal ATLAS DAQ path[6].

The data is analysed and the results of each calibration are stored to the COOL database. A separate validation procedure checks the quality of the calibration. A calibration may be marked as “validated” for use in the next run if it passes the checks and if the new calibration constants are significantly different from the previous set.
VIII. RUN CONTROL AND MODULE SERVICES

The normal operation of the L1Calo trigger is handled under the ATLAS TDAQ run control framework. This provides initialisation of the distributed environment with numerous information, histogramming, monitoring and other services. Configuration and periodic status monitoring of L1Calo and other ATLAS subsystems is carried out via synchronous run control commands, most of which result in state transitions. Under the run control framework, each ATLAS component to be configured is controlled by a run control application.

In the L1Calo system, there is one such application per VME crate. This is responsible for loading and monitoring all the modules in that crate. An overview of the main classes involved is shown in figure 4. To insulate the module libraries from the TDAQ services, the functions required of each module are split into two distinct classes. The \texttt{RcModule} class is completely generic and acts as a façade for any hardware module subclass. Together with its parent run controller object, it is responsible for accessing the database, responding to run control commands and publishing the status, trigger rates and (soon) onboard histograms to the corresponding TDAQ servers. \texttt{HwModule} subclasses are responsible for configuring one type of module via VME and collecting data from it. This split has proved useful in hiding changes in the TDAQ API from the bulk of the hardware access libraries. The information published by the run control packages is available for display via run control panels and other tools.

IX. DISPLAYS

A number of graphical displays have been developed in addition to those, such as ACE, HDMC and OHP, which have already been mentioned.

The TDAQ run control GUI allows ATLAS subdetectors to add their own panels. The L1Calo panel in this GUI displays the detailed status of each module in the system in a hierarchical tree view with a colour code to propagate an error state up the tree.

Monitoring of trigger rates at the level of individual towers and for the whole system is crucial. The ATLAS TDAQ software includes a display for the final Level-1 trigger rates. In addition the L1Calo software provides a tabular display of many detailed rates from L1Calo and other parts of the Level-1 trigger.

Finally, there is a visualisation tool displaying the space of L1Calo trigger towers in pseudorapidity and azimuth. This shows the mapping of towers to hardware and cables throughout the system. It can also show database settings, status and trigger rate for each tower and can act as simple event display.

X. SUMMARY

A large body of software has been written for configuring, testing, calibrating and monitoring the ATLAS level-1 calorimeter trigger. This has been successfully used at several stages of the L1Calo project. Initially for testing prototype and production modules, subsequently for the installation and commissioning the final trigger system in ATLAS and most recently for configuring it to trigger on events from the first beam in the LHC.

XI. ACKNOWLEDGEMENTS

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The TOTEM Roman Pot Motherboard

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Abstract

The TOTEM Roman Pot Motherboard (RPMB) is the interface between the hybrids with silicon detectors and front end chips in the Roman Pots, and the outside world. The RPMB is glued in the vacuum flange which separates the vacuum chamber containing the detector hybrids, and forms the feed through between vacuum and atmosphere. The hybrids have a flexible part with on-board connector for connection to the motherboard. The motherboard is equipped with connectors to the detector hybrids from one side and front panel with connectors to the patch panel form the other side.

The RPMB needs to provide power and control, clock and trigger information to the 10 hybrids. It acquires tracking and triggers data from the hybrids, performs data conversion from electrical to optical format and transfers the data to the next level of the system \cite{1}. It also collects information like temperature, pressure and radiation dose inside the pot. This paper presents the TOTEM RPMB in detail.

I. INTRODUCTION

TOTEM (Total Cross Section, Elastic Scattering and Diffraction Dissociation Measurements) \cite{2} is an experiment dedicated to the measurement of total cross section, elastic scattering and diffractive processes at the LHC. The full TOTEM detector consists of Roman Pot Stations (RPS), Cathode Strip Chambers T1 (CSC) and Gas Electron Multipliers T2 (GEM). The T1 and T2 detectors are located on each side of the CMS interaction point in the very forward region, but still within the CMS cavern. Two Roman Pot stations are foreseen on each side of the interaction point at 220 m and 150 m. Each Roman Pot station consists of two groups of three Roman Pots separated by a few meters to obtain a sufficiently large lever arm to establish co-linearity with the LHC beam for the tracks prior to generating a level one trigger for the corresponding event. Each Roman Pot contains 10 silicon strip detectors with 512 strips read out by 4 VFAT2 readout chips \cite{3}.

II. GENERAL DESIGN SPECIFICATIONS

Apart from the electrical functionality described in detail below, the design of the RPMB was constrained by the mechanics and by radiation tolerance.

The RPMB has to fit in the Roman Pot mechanics, connect to 10 hybrids in a secondary vacuum (the primary vacuum is that of the machine within the beam pipe, the primary and secondary vacuum are separated by a window of about 100 micron thick), and feed through about 800 signals to and from the outside world. The connections to the outside are naturally on the end opposite to the hybrids. The maximum width of the feed through for these 800 signals is about 12 cm and together with the other size limitations this results in a very challenging layout with 16 layers for the RPMB.

The RPMB is also subject to radiation, imposing radiation tolerance for all components. In particular all on-board integrated circuits are full-custom circuits designed in 0.25 micron CMOS technology with special techniques to increase the radiation tolerance \cite{4}\cite{5}.

Safety regulations imposed also fabrication of the board with halogen free material.

Figure 1: RPMB Photo - top and bottom side

Figure 1 shows the pictures of both sides of the completed board without mezzanine cards mounted. A front panel (at the right of the picture) with connectors for low and high voltage, control, data and trigger bits transfer is used to facilitate the connection to the central patch panel of the RP stations. The narrow part on the left with the connectors for the hybrids is the part placed inside the pot. The feed through (area glued in the flange) is the large copper stripe on the narrow part.
III. TOTEM ROMAN POT MOTHERBOARD

The TOTEM RPMB functional block diagram is shown in Figure 2. The blocks are described in detail below.

A. Power Distribution

The RPMB needs to receive low voltage power at 2.5 V for its own operation, and for the operation of the hybrids. The power on the hybrids has been carefully separated between analog and digital blocks, both powered at 2.5 V.

The silicon detectors need to be biased up to 500 V after irradiation. The RPMB receives this high voltage supply and distributes it to the detector hybrids. The supply is separate for all detectors; grouping is done in the counting room. This allows isolating defective detectors from the rest if needed.

B. The slow control

The slow control system has been copied from the CMS tracker and ECAL detectors [6]. A FEC-CCS board in the counting room sends and receives optical control data, on the detector side a Digital Opto-Hybrid Module (DOHM) converts this data back to electrical form and interfaces with the RPMB via two 20pins 3M high speed connectors placed on the front panel. A Communication and Control Unit mezzanine (CCUM) on the RPMB (see Figure 3) decodes this information and provides 16 I2C interface channels and one 8 bit parallel control port for use on the RPMB. All integrated circuits including the VFAT2 are controlled using these I2C interfaces.

In addition to the slow control information transmitted over I2C, several sensors mounted on the RPMB or on the hybrids provide additional information like temperature, pressure and radiation dose.

PT100/1000 sensors are used for temperature, and a piezoelectric pressure sensor measures the pressure inside the pot to verify the pressure remains close 0 (a secondary vacuum has to be maintained in the Roman Pot).

A special small carrier card (RADMON) [7] is used for radiation monitoring on the RPMB. This carrier is made of a thin (~500 m) double-sided PCB. It can host up to 5 p-i-n diodes and five RadFETs mounted inside a proper package. It also includes a temperature sensor (10k NTC). This total of 11 devices can be read out via a 12-way flat cable: 11 for sensor signals and a common Return Line (RL) connection. A photo of the carrier is shown on Figure 4.

![Figure 2: RPMB Functional Block Diagram](image)

![Figure 3: CCUM Mezzanine photo](image)
C. Clock and Fast Commands

The FEC-CCS card receives clock and fast commands in the counting room and includes these with the slow control data for transmission to the detector using the same channel as the slow control. On the RPMB the clock and fast command signals are reconstructed by the PLL25 chip. The QPLL, a quartz based PLL, is used to further reduce the clock jitter necessary for serialization and optical transmission of data. The clock and fast command tree has been designed to minimize timing spread over all components on the RPMB.

D. Tracking Data transmission

The data sent by the VFAT2 front end chips upon a level 1 trigger signal is converted from LVDS to CMOS on the RPMB and then presented to the gigabit optical hybrids GOH modules, which serialize and convert the electrical data to optical for transmission to the Data Acquisition (DAQ) system in the counting room. Three GOH modules are used to send data from 40 VFAT2 chips.

E. Trigger Data generation and Transmission

Each VFAT2 front end chip has 8 trigger outputs of which 4 are used in the Roman Pots. Every hybrid therefore generates 16 trigger outputs, and 5 hybrids have the same orientation of the silicon strips (U coordinate), and the 5 others have strips oriented at 90 degrees (V coordinate). The trigger signals are put into coincidence in two separate Coincidence Chips (CC), one for the U and one for the V coordinate. The CC chips are mounted on the RPMB as mezzanine cards (CC mezzanine), one mezzanine per CC. The CC provides 16 outputs (so the number of trigger signals is reduced from 2x80 to 2x16), and these signals have to be transmitted to the counting room.

For these coincidences a full custom chip rather than using a Field Programmable Gate Array was developed for two reasons:

- the latency constraints on the generation of the trigger bits especially from the Roman Pots are very severe: after subtraction of cable delays only about 8-10 bunch crossings are left for the generation of the trigger signals to be provided to CMS from the signals generated by the Roman Pot. A full custom chip with dedicated logic can implement the required coincidence in one clock;
- the CC needs to be placed on the RPMB or at least near the detectors and is therefore subject to radiation. Special design techniques were used to make the CC much more robust against radiation both with regard to total dose and single event effects than a standard FPGA. The CC mezzanine was designed to carry one Coincidence Chip and two 130 pins input/output connectors. Figure 5 shows a photo of the CC mezzanine.

To transmit trigger bits to the counting room two ways have been selected: optical fibers are used for the 150m RP stations and in TOTEM standalone runs also for the 220m stations. The runs with CMS on the other hand are subject to CMS’s limited trigger latency time, imposing trigger bit transmission with LVDS signals through fast electrical cables, because the serialization and deserialization and optical transmission in the fiber (~5 ns/m) take too much time. The electrical transmission over such a long distance requires care to preserve signal integrity. This can only be achieved by restoring the LVDS signals to full levels at regular intervals over the transmission distance. A special integrated circuit was designed for this purpose: the LVDS repeater chip can treat 16 LVDS channels in parallel and was designed in special layout to guarantee radiation tolerance. This chip will be mounted on a small repeater board. At regular intervals of about 70m a repeater station is introduced which consists of 12 repeater boards (one for every cable carrying 16 LVDS signals).

Since the trigger signals are sent every clock cycle some time reference has to be included in the trigger data stream to facilitate recovering the correspondence between the event and the transmitted bits. This is done from the fast command bunch crossing 0 (BC0) by the VFAT trigger mezzanine (Figure 6). The VFAT on board decodes the BC0 signal and provides this to some circuitry which actually disables the GOH’s data valid signal upon reception of the BC0 signal for the duration of one clock cycle. This can be recognized in the counting room, and provides the time reference.
In addition the VFAT trigger mezzanine records the trigger bits and merges them upon a level one trigger with the tracking data, so that the trigger bits which lead to a triggered event are recorded with the tracking data from that event.

Figure 7 shows a block diagram of the trigger generation and transmission block on the RPMB.

Figure 7: Trigger Generation and Transmission Block

IV. SUMMARY

The TOTEM RPMB is a complex system which forms the interface between the silicon detector hybrids and the outside world. It provides the feed through between vacuum and atmosphere for about 800 connections. It has to fit in a relative small space and is subject to radiation. All integrated circuits on board were full custom designed for radiation tolerance. Special precautions were taken for power, clock and data distribution and transmission. The use of mezzanines allowed testing at several stages.

In total 24 Roman Pots (and RPMB) are foreseen for the TOTEM experiment. Currently 2 are installed, one on each side of the experiment at 220 m (sectors 4-5 and 5-6). The others will be installed over the next several months.

V. ACKNOWLEDGMENTS

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VI. REFERENCES

Infrastructures and Monitoring of the on-line CMS computing centre

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Abstract

This paper describes in detail the infrastructure and installation of the CMS on-line computing centre (CMSOLC) and its associated monitoring system. In summer 2007, 640 PCs acting as detector Readout Units for the CMS Data Acquisition System (DAQ) were deployed along with ~150 servers for DAQ general services. Since summer 2008, ~900 PCs acting as DAQ Event Builder Units/Filter Units have been added and today, the CMSOLC has an on-line processing capability sufficient for a Level 1 trigger accept rate of 50 kHz. To ensure that these ~1700 PCs are running efficiently, a multi-level monitoring system has been put in place. This system is also described in this paper.

I. INTRODUCTION

The Compact Muon Solenoid (CMS) experiment [1] at CERN’s Large Hadron Collider (LHC) will search for new physics at the TeV scale such as the Higgs mechanism or Super-Symmetry. At its design luminosity of \(10^{34} \text{ cm}^{-2} \text{s}^{-1}\) the LHC will provide proton-proton collisions at a centre-of-mass energy of 14 TeV with a bunch crossing frequency of 40 MHz. Each bunch crossing will give rise to about 20 inelastic collisions in which new particles may be created. Decay products of these particles are recorded by the sub-detector systems of CMS comprising on the order of \(10^8\) readout channels. After zero-suppression, the total event size per bunch crossing is expected to be on average 1 MB. A highly selective online-selection process accepts on the order of \(10^5\) events per second to be stored for offline analysis.

In CMS, this selection process consists of only two levels. The first level, the Level-1 Trigger [2] that is a dedicated system of custom-built pipelined electronics, reconstructs trigger objects (e.g. muons, electrons/photon, jets) from coarsely segmented data of the muon and calorimeter subdetectors. Based on concurrent trigger algorithms which include cuts on transverse momentum, energy and event topology, it accepts interesting events at an average maximum rate of 100 kHz (minimum rejection ratio 1:400 bunch crossings).

All further steps of on-line event processing including the read-out, data transport to the surface and event-building at an aggregate data rate of 100 GB/s, high level trigger processing and data storage are handled by the CMS Data Acquisition (DAQ) System [3]. The \(\sim 10^8\) readout channels are grouped into approximately 650 data sources by the Front-End Driver (FED) electronics. Full event data are buffered during the 3 µs latency of the Level-1 Trigger and pushed into the DAQ System upon a Level-1 accept. The event building process is implemented with a two-stage event building architecture [3]. The fully assembled events are passed to the filter farm which executes the high-level trigger decision based on reconstruction algorithms similar to the full off-line reconstruction. The rejection factor achieved by the filter farm is about 1:1000. Hence, about 100 events per second are sent to the central storage system in the Meyrin computer centre.

Figure 1: CMS DAQ block diagram
II. CMS DAQ INFRASTRUCTURES

A. Civil engineering and racks

The DAQ building on the CMS experimental site contains the general detector control room, the DAQ farm control room, a sub-detector control room, a conference room and the DAQ farm itself. Everything but the farm is located on the ground floor. The farm occupies the whole of the second floor (See figure 2).

The computer room features a 1m deep false floor and has a total capacity of 180 racks for a maximum power dissipation of 800 kW. Currently 106 racks are installed which corresponds to a data processing capacity of a 50 kHz trigger rate. The remaining half will be equipped as the luminosity of the LHC ramps up. Nevertheless, the entire plumbing infrastructure has been installed for the full 100 kHz system.

In 2003, the total number of servers and their projected power consumption was estimated at ~140 racks and ~750 kW of dissipated power. The power density in the room is about 2 kW/m2 and depending on the PC type (readout unit or builder/filter unit), the power per rack ranges from 4 kW to 10 kW. Given such high power densities, custom designed water-cooled racks were chosen to remove the heat load from the servers.

After preliminary studies carried out within the “LHC PC Rack Cooling Project” [4], CMS purchased about 150 water cooled PC racks from CIAT [5] with the following features:

- 47 U high, 19 inch mounting standard
- 44 U usable internal space
- 60 cm x 90 cm footprint, 106 cm total depth
- 10 kW thermal capacity

- 2 m³/h water flow, ΔT 4 °C.
- 3 fans, 2450 m³/h air flow, front to back

To maintain a very low cost, minimal monitoring capabilities are implemented at the rack level comprising a fan failure signal per fan and a thermostat with a threshold at 40 °C.

The racks are arranged in group of 8 (7 when pillars were present) and placed according to the hot/cold aisle principle. Although this arrangement is not needed for cooling efficiency, it is practical for human access to the front faces of the PCs without being subjected to cold air blasts. The distance between rows of racks is 1.50 m front to front and 1 m back to back (see figure 3).

B. Cooling water and electrical power

A cold water plant located next to the building provides the cold water for the racks. With the nominal inlet water temperature being 14 °C, it is important to control the air humidity in order to avoid condensation. Therefore, a 100 kW air conditioning unit is connected to the computer room in order to absorb daily heat fluctuations and control the air humidity, hence maintaining the air dew point below 12 °C.

The power distribution relies on a Canalis system feeding from the top each group of 8 or 7 racks. A Canalis power bar brings a maximum of 64 Amps on 4 phases in each rack for a maximum power of 14 kW. Each phase is equipped by a D-type breaker of 16 amps. For each phase there is a 10 outlet power distributor including a sequencer on 3 groups of outlets with a 200 ms delay between groups to prevent the phase breaker from tripping due to the inrush current when all servers are switched on at the same time.

C. Fire safety

Eight smoke detection devices are installed in the room. The smoke input pipes are located above the racks at the air exhaust. If smoke is detected in the room, electrical power is cut and a water mist system from Marioff [6] can be automatically activated. HI-FOG is a fire protection technology utilising high pressure to produce a fine water mist with average drop size of 50 - 120 µm, combining the extinguishing characteristics of water with the penetrative qualities of gases with no danger to people or the environment. Specific tests have been carried out and showed that running computers are not damaged and continue to perform their tasks when exposed to water mist.

D. Networks

The different communication networks are laid in cable trays beneath the false floor. The cable trays are organized in three layers of 40 x 10 cm². The main networks are:

- The optical Myrinet switch-Readout Units (RU) network. This network distributes the data coming from the underground counting rooms to the RU machines
- The service network (copper). This network is used to access the machines for maintenance and monitoring purposes. For example, the IPMI (Intelligent Platform Management Interface) temperature monitoring process runs over this network.
The data network (copper). This network is used to exchange data packets during the event building process between the RU's and the Builder Units/Filter Units (BU/FUs).

Exhaustive information about the network topology can be found in [7].

III. CMS DAQ HARDWARE MONITORING

To ensure that the servers perform their tasks according to expectations, the environmental conditions and the servers themselves must be monitored.

E. Physical parameters monitoring

Physical parameters are monitored at the room level and at the server level giving detailed information about the operating parameters.

At the room level, the monitored values are the following:
- Temperature
- Relative humidity
- Inlet water temperature
- Outlet water temperature
- Water flow

Those values are provided by the air conditioning system and the cold water plant through DIP (Data Interchange Protocol)[8] which is a communication protocol developed at CERN that allows relatively small amounts of soft real-time data to be exchanged between very loosely coupled heterogeneous systems. Very low latency is not required for the monitoring of these systems. The data is assumed to be mostly summarised data rather than low-level parameters from the individual systems, e.g. cooling plant status rather than the opening level of a particular valve.

PVSS [9] applications have been developed in order to monitor the room level values as provided by the water plant and air conditioning unit. If any of these values are not within nominal ranges, an alarm notifies the DAQ group of the problem. A month history is stored in order to make correlations with other events if necessary. (See figure 4).

In nominal cooling conditions, the internal temperature of the machines is close to 20 °C. In the case of cold water service interruption, the server internal temperature will start to rise. When it reaches 27 °C, a warning is issued on the server console. When it reaches 30 °C for RU's and BU/FUs (called hereafter the soldiers) and 33 °C for the general services servers, a daemon, which checks the temperature every 5 minutes, powers of the machine in a graceful way. If all protection mechanisms failed, a hardware thermostat cuts the power supply at the Canalsys level when rack internal temperature is above 40 °C. The different temperature thresholds for soldiers and servers are there to give priority to the servers over the soldiers. With the soldiers shut down, the room temperature ceases to rise, hence keeping the important servers on-line.

A latency of ~30-45 minutes has been observed between the cold water service interruption and first soldier graceful shutdowns. Up to now, graceful shutdowns of servers have never been observed.

As mentioned above, IPMI is used to retrieve the internal temperatures, voltages and fan speed. The IPMI module collects also warning and error messages generated by the system itself. For example, if the memory failed to correct an access error, a message will be logged and be available through the IPMI port. These kinds of messages allow problems to be discovered at an early stage. Every hour, a script reads new messages and stores them in the maintenance database.

F. Services monitoring

Monitoring the physical parameters of servers is necessary but not sufficient to ensure that the machines are performing as expected. The services must also be monitored by dedicated tools. Nagios [11] has been chosen to perform the service monitoring. Nagios is a system and network monitoring application. It watches hosts and services defined by the user and sends alerts when things go bad and when they get better. Nagios has built-in modules for monitoring things like network services (SMTP, POP3, HTTP, NNTP, PING, etc.) or host resources (processor load, disk usage, etc.) A simple plug-in design allows users to easily develop their own service checks for specific needs. Depending on the server function, different sets of tests have been implemented. Amongst them are:

- Check if IPMI is accessible remotely
- Check if JOBCONTROL is running. This application is needed to integrate the server in the data taking process.
- Check if Kerberos authentication is working
- Check if the machine is reachable via Ping
- Check if Secure Shell (SSH) is running
- Check if SLP (Service locator protocol) is running.
- Check installation - if the Quattor (a CERN specific system administrative tool) [12] installations have completed successfully
- Check CPU load
- Check free space on disk partitions
- Check total number of running processes
- Check number of users logged-in
- Check if zombie processes are present

When a problem is detected by Nagios, system administrators are notified and corrective actions are scheduled.

G. Hardware maintenance tracking

The total number of machines installed up to now is close to 2000, including the machines located in the underground counting rooms, and this number will grow along with LHC luminosity. We expect a total of 3000 machines in the near future. Given this considerable number, a database has been implemented to store the characteristics of each machine (i.e. serial number, physical location, system name, Network hardware addresses, interfaces, warranty duration, etc) and all warning/error messages collected through IPMI every hour. The user interface of the database allows the display of the last warning/error messages and related machine maintenance history. This database is also used to store hardware changes (e.g. change of location) and track the hardware interventions on the machines. Summaries and statistics can be made through the user interface.

H. What next?

As already mentioned above, the next important milestone is to complete the CMS on-line computing facilities and reach the processing power needed to filter 100 kHz of Level 1 trigger rate. Before launching the tender for these additional filter units, some infrastructure must be completed: the false floor modification for one meter deep racks and the purchase and installation of new water-cooled racks with a thermal capacity of 16-18 kW. This increased thermal capacity is required for housing the next generation of multi-core multi-processor machines. These steps are scheduled for the beginning of 2009.

Regarding the computing services monitoring, the target is to continue to develop and customize existing management tools and integrate them into a single user interface that will be used for the different actions performed on a machine in the computing centre:

- Creation of a new machine or replacement of an existing machine.
- Operating system and software deployment and update
- Monitoring of the behaviour of the machine, and if needed automatic notifications of hardware or software problems
- Maintenance actions tracking
- Summaries and statistics production

IV. SUMMARY

The on-line CMS computing centre, located at the surface of the experimental site, performs the event assembly (640 event fragments produced by the detector are assembled into a single event of ~1MB) and subsequently, executes the high level trigger algorithms (HLTs) in order to select the events to be stored for later off-line analysis.

The heavy infrastructures (false floor, water ducts, racks, power rails) were installed in 2005 and 2006. The cabling for the first batch of 800 servers (event builder PCs) started early 2007. The event builder PCs have been installed and commissioned in summer 2007. They are acting also as event filters as long as the data volume does not require dedicated PCs to run the HLT algorithms. About 900 servers for on-line event filtering have been installed this summer in view of the LHC start-up. Installation of an additional 1000 servers is foreseen for 2009 to reach the full processing power.

There is a three level monitoring system for all the machines: the first level is dealing with physical parameters (voltages, temperatures, fans) and maintenance/repair actions. The second level is monitoring the services provided by each server (ssh, tcp, presence of drivers, etc). The third level is looking at the application performances. Data retrieved by the three levels of monitoring are stored in a database.

V. REFERENCES


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Achieving Best Performance with VME-based Data Acquisition Systems and 2eSST

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Abstract

The double edge Source Synchronous Transfer (2eSST) is the fastest block transfer cycle offered by the VME64x standard. The maximum achievable data-rate foreseen by the protocol is 320 MByte/s. In this paper we present a reference design based on a FPGA, for the reader willing to implement 2eSST in his VME64x application. By using this template, we have designed a custom Bit Error Rate Tester, in order to probe the block transfer reliability within and beyond the data rate limit presently set by the standard. Our results show that 800 MByte/s data transfers can be achieved in a 21 slots crate with a BER smaller than 10^{-12}.

I. INTRODUCTION

THE ANSI/VITA 1.5-2003 standard \cite{1} adds to the VME64x bus \cite{2} a source-synchronous, double data rate block transfer cycle known as 2eSST. It allows the bus master to move across the backplane bursts of up to 256 words, each 64-bit wide, for a total of 2 KByte. In order to achieve the highest bandwidth, data is clocked by both positive and negative edges of a strobe, with no handshake. The protocol adopts an iso-synchronous scheme and the data producer is also in charge to drive the double rate strobe. According to the transfer direction, different lines are used to strobe the data. With this approach, the value of propagation delay does not affect by itself the timing performance and the maximum data transfer rate is set by the skew between the specific strobe and the data lines. Different loading on the bus lines and spread in the driver’s behaviors shrink the timing budget for a correct data transaction. Even board layouts with a significant difference in the flight time of signals between bus connectors and on-board logic contribute to this effect. In a real system, the designer faces the challenge to optimize the system performance taking into account line transmission effects, asymmetric bus loading of legacy boards and even different behavior between read and write cycles. The latter is due to the privileged master location, which usually sits nearby the impedance termination network in the leftmost slot, at the far end of the line. Data driven in a read cycle is then received by the master in the cleanest environment. In a write cycle, on the contrary, a slave board located in the middle of a populated backplane might sample a signal distorted by multiple reflections. The protocol greatly improves the skew tolerance by placing the strobe at the center of the data window. The double data rate architecture invites the designer to work with a dual phase clock or at double the frequency and this makes it quite simple to set the strobe timing. However, in order to toggle the strobe as close as possible to the ideal central position, the transmitter logic needs a careful layout with balanced I/O timing between data and strobe. On the receiver side, the setup and hold requirements of the input logic should define a timing window centered on the strobe edge with the smallest width. The present version of the 2eSST protocol specifies three speed grades, with nominal strobe widths of 50, 30 and 25 ns, equivalent to a total bandwidth of 160, 267 and 320 MByte/s. For each speed, the standard analyzes the timing budget, stating the maximum allowed skews on the transmitter section, on the backplane, on the receiver and the worst-case setup and hold of the input registers. The burst speed is negotiated in the first steps of the transaction by transmitting a specific code in a bit field. It is interesting to note that the protocol reserves codes for even faster speed grades, which could be announced in the future. In this view we have tested the present physical layer beyond the maximum specifications. With a careful Printed Circuit Board (PCB) layout and keeping in mind the main sources of skew in the transmitter and receiver sections, we have designed a companion board-set capable to transfer data beyond the 320 Mbyte/s limit. The two boards are strictly VME64x-compliant and are designed around off-the-shelf components, including mature low cost Xilinx Spartan III Field Programmable Gate Arrays (FPGAs). The backplane as well is a commercial 21-slot, 6-layer VME64x implementation with active terminations. Transmitter and receiver suffer from the ground bounce and the simultaneous switching noise out of the 64-bit busses. While already important at standard speeds, these noise sources become a serious issue when pushing the data transfer rate; they challenge the signal integrity and add jitter and skew to the lines. The payload switching activity during a burst determines the noise level on the boards and on the transmission lines. At higher transfer rates this parameter affects significantly the achievable performance.

II. THE BIT ERROR RATE TESTER

Our tests on VME64x bus aim at studying the performance beyond the current data rate limit set by 2eSST specifications. We have designed a custom Bit Error Rate Tester (BERT) that can work with data rates up to 1 Gbyte/s. The BERT is based on two VME boards: a transmitter (TX), which sends custom data pattern across a VME backplane, and a receiver (RX), which compares it with a local copy of the pattern, flagging an error if a difference occurs (Fig. 1).The TX includes a programmable circular pattern generator with a length of 2k words. The clock frequency of the TX is set using an external clock generator and is halved to provide the strobe burst.
The output is transmitted in VME block transfer cycles in 256 word bursts, according to 2eSST VME specifications. The structure of a burst is shown in Fig. 2. A transition on a strobe line (DS1* or DTACK*), either positive or negative, validates data on A31-A1, LWORD, D31-D0 lines. Every burst begins with a negative transition on the strobe line and ends with a positive transition. The time interval between data bursts is programmable. Using an output register, the 40 bits output of the encoder are used to feed the J1 connector lines (D0-D15, LWORD, A1-A23), and the 24 least significant bits are also sent on J2 connector lines (D16-D31, A24-A31). The RX stores the data in a DDR input register clocked by the strobe line. Data is then transferred to a DDR FIFO, which has independent clocks domains for double rate writing and single rate reading. The VME strobe line is used as write clock and a 80 MHz internal clock as read clock. The DDR FIFO is used to decouple the VME clock domain from the receiver’s internal clock domain. Also, using an input FIFO reflects what a designer would do in a real application. The BERR* VME bus line allows the TX to provide an external reset to the FIFO and to the input register. This signal makes only one transition at power up, thus doesn’t affect the signal integrity of the adjacent data lines. Data coming out from the FIFO is compared in parallel with the output of a local pattern generator identical to the one in the TX. Each of the 64 comparators drives a clock enable of a 8-bit error counter. If a received bit is different from its local copy, the corresponding counter is incremented. An embedded microprocessor handles those counters and takes care of error displaying via a serial link. A 24 bit counter counts the number of VME words received and, when it overflows, issues an interrupt request (IRQ) to the microprocessor. The interrupt service routine reads the error counters and resets them. The CPU accumulates the value read from each error counter in a different 16-bit variable, thus extending the countable errors from $2^8 - 1$ to $2^{16} - 1$. If more than 255 errors occur on the same bit between two interrupts, the corresponding counter saturates. We did not take measurements in data rate ranges that make any counter saturate. However this has not been a limiting condition for our measurements which aimed at very low BER levels. The microprocessor periodically prints out the content of the variables and the number of the received words on a RS-232 serial port in ASCII format. Receiver and transmitter units have been implemented using two identical boards hosting a Xilinx Spartan IIE XS300 FPGA. Boards are equipped with SN74VMEH22501 bus transceivers [3]. They offer the latest available driving technology for 2eSST cycles and are required by the ANSI standard. A detailed characterization of these devices in VME applications can be found in [4] and [5]. Our boards have test points for some VME bus lines either on input and on the output of each driver. Timing performance of the data transfer has been optimized both on the TX and RX FPGAs. The output register of the transmitter is implemented into FPGA IOBs, thus all the bits have almost the same clock to output delay (Tco). As Spartan IIE FPGAs don’t provide Double Data Rate (DDR) primitives, each bit of the receiver’s input
register has been implemented with a pair of flip-flops, each in a different slice of the same CLB, with inverted clocks (Fig. 3). The layout has been manually optimized to have balanced setup and hold times around the clock edge and to make them as similar as possible for all the flip-flops (Fig. 4). The setup (hold) time has a mean of 0.20 ns (0.27 ns) and a standard deviation of 0.13 ns (0.13 ns).

Newer devices (e.g. Xilinx Virtex-II Pro) do offer DDR capable primitives. By means of those, we would not have to manually optimize the layout to equalize setup and hold times from different flip-flops, which would have been all the same. The DDR structure we designed using one IOB and two single rate flip-flops from two different slices could have been conveniently obtained by using just one double data rate IOB (Fig. 5).

Data patterns in the transmitter and receiver FPGAs are stored in ten 1k x 8 bit RAM banks. Their content is embedded in the bit-stream and they are initialized during the FPGA configuration. We developed a simple software utility to generate user defined data patterns and to load it in the right spots of the bit-stream. In this way we don’t need to regenerate FPGA configuration files on a pattern change. Our setup makes it possible to measure the bit error rate of every VME data line as a function of the data rate and pattern. It also allows us to investigate the effect of the bus invert coding on the BER and signal integrity.

III. TEST RESULTS

In our setup we have the two tester boards acting as master (TX) and target slave (RX). The master executes write cycles toward the slave. Five more boards, all VME64x compliant, have been used to load a 21-slot backplane and to take into account the change in the bus line impedance present in a real environment. The master has been placed in slot 0. According to the VME64x protocol, all the slaves participating to the 2eSST should be clustered in adjacent slots. By grouping them at the center of the backplane, we obtain a significant perturbation of the line impedance, giving us a typical scenario in data acquisition systems [6]. The target slave has been placed in slots from 9 to 14, with the other boards filling all the remaining slots in the range 9-14. We focused on this configuration, because earlier studies indicate this one as signal integrity worst case [7]. We measured the BER as a function of the data rate in all slots from 9 to 14. We spanned the range from 320 Mbyte/s to 800 Mbyte/s, equivalent to 40 Mbps to 100 Mbps rate on each data line. As data pattern, one would like to use the worst case switching activity pattern, which is obtained making all the data lines toggle at every cycle.

This choice would not generate a reasonably good pseudo-
random pattern, because the length of the pattern would be just of 2 words. To overcome this problem, we used a random pattern with a 7/8 switching activity per each byte, which has the next highest switching activity (for our bus partitioning). Our BERT recorded zero errors on all data lines with more than $10^{13}$ words transferred. This result gives a $10^{-12}$ BER with a confidence level bigger than 99% [8]. At 40 Mbps each BER run takes more than 120 hours, while the measurement lasts more than 48 hours at 100 Mbps. In order to reveal the BER trend versus the bit rate, one should increase the number of transferred bits. It is evident that this approach is not practical due to the too long run time needed. To gain insights into the available timing budget of the transaction, we instead performed alternative measurements based on data and clock edge relative timing. For this purpose we used a Serial Data Analyzer (SDA) oscilloscope with 20 Gsample/s maximum sample rate and 6 GHz bandwidth [9]. For each data edge the oscilloscope measures the timing interval between the data and clock edge, i.e. the Time Interval Error (TIE) (Fig. 2 bottom). The instrument collects the TIE measures in a histogram. This histogram is an estimate of the probability density function (p.d.f.) of the TIE, which is the probability to observe a data transition at a certain instant with respect to the clock edge. From the p.d.f. it is possible to calculate the BER as a function of the instant at which a data transition occurs. From this function one can obtain the timing budget (Tb) and thus the total jitter (Tj = UI – Tb, where UI is the unit interval) at a given BER. So, the TIE p.d.f. defines a biunique relationship between the total jitter of the data edge and the bit error rate.

The oscilloscope uses a specific software tool [10] to extrapolate the expected total jitter (Tj) at a given bit error rate ($10^{-12}$ in our case) from the measured TIE histogram. In our tests, we measured Tj at $10^{-12}$ BER as a function of the data transfer rate (from 40 Mbps to 100 Mbps) and of the slot occupied by the slave (from slot 9 to slot 14). In the following discussion we will refer to Tj/UI instead of Tj. Our results show that Tj/UI grows moving the RX unit from the slot 14 toward 9, so in our set-up slot 9 (the nearest to the TX board) exhibits the worst behaviour. Fig. 6 illustrates the Tj/UI trend versus data rate measured at slot 9 and slot 14 for both the un-encoded and the coded case. Tj/UI is a strictly increasing function of the data rate. At slot 9 Tj/UI almost reaches 60% at a 100 Mbps data rate, while at slot 14 it does not exceed 40%. Note in Fig.6, how slot 9 shows a smaller open “eye” with respect to slot 14. The value of Tj increases as a function of the data rate (1/UI) because of the deeper impact of the transmission line effects on the signal integrity. Our setup is able to directly measure a non zero BER (with a run time of the order of one day) at data rate
of 111 Mb/s. In the data rate range between 111 Mb/s and 112 Mb/s the BER gains 6 orders of magnitude. The bit with the highest BER is D10. The nearest bits on the connector’s C row exhibit a similar behaviour. The histogram in Fig. 7 shows the BER distribution on part of the J1 connector, when D10’s BER reaches $10^{-11}$. Fig. 8 shows the bit error rate versus the data rate per line at slot 9.

### IV. CONCLUSIONS

Our results show that VME 64x 2eSST block transfer can currently sustain data transfer up to 800 MByte/s with a BER of $10^{-12}$ (estimated with a 99% confidence level) for typical loading conditions found in a high performance DAQ system. By direct BER measurements and jitter analysis, we studied the timing budget versus the data rate as a function of the slot occupied by the slave. It should be noted that we did not study the BER and total jitter dependence on temperature, power supply voltage and different loading conditions (i.e., legacy boards, different number and location of the slaves). However, even at 800 MByte/s data rate, in the worst case conditions, we have found an available timing budget larger than 40% of the unit interval. Our results have been obtained with low cost FPGAs without DDR primitives, so we had to manually optimize the layout for the input logic. Newer devices offer DDR I/O resources and remove that need, making the design implementation easier. We conclude that the present technologies (VME64x backplanes, bus drivers, FPGAs) allow reliable 2eSST transfers with speed grades beyond the current limit.

### REFERENCES


Figure 8: Top: D10 BER versus data rate for a fixed 7/8 switching activity data pattern. Bottom: eye diagram for the lowest data rate point.
A multi-channel 24.4 ps bin size Time-to-Digital Converter for HEP applications

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Abstract

A multi-channel time-tagging Time-to-Digital Converter (TDC) ASIC with a resolution of 24.4 ps (bin size) has been implemented and fabricated in a 130 nm CMOS technology. An on-chip PLL is used to generate an internal timing reference from an external 40 MHz clock source. The circuit is based on a 32 element Delay Locked Loop (DLL) which performs the time interpolation. The 32 channel architecture of the TDC is suitable for both triggered and non-triggered applications. The prototype contains test structures such as a substrate noise generator. The paper describes the circuit architecture and its principles of operation.

I. INTRODUCTION

Detectors in HEP applications often require high precision timing measurements. For example the ALICE Time of Flight (TOF) detector, which provides information for particle identification, requires a TDC bin size of 25 ps on 160 704 channels. This leads to an over-all resolution of the full TOF detector of 100 ps. Together with other ALICE subdetectors, the mass of a charged particle can be calculated, allowing to distinguish $\pi$, $K$ and $p$.

The HPTDC, an 8/32 channel high resolution time-to-digital converter that was previously developed at CERN in a 250 nm CMOS technology [1], is now in use in the LHC experiments ALICE [2, 3], ATLAS [4], CMS [5] and LHCb [6]. Its resolution is programmable and can be set to 100 ps or 25 ps (bin size) by trading the number of measurement channels for resolution. To implement the high resolution mode an RC interpolation scheme (fig. 1) that combines four channels into one high-resolution channel has been implemented. The principle of interpolation is to use four channels to perform four conversions with 100 ps resolution but 25 ps delayed from each other, allowing to obtain an effective resolution of 25 ps. This, however, reduces the number of usable channels from 32 per chip to 8 per chip.

Simulations show that in a 130 nm CMOS technology, a basic resolution of 25 ps can be achieved with a non-interpolating architecture, increasing the potential of integrating a higher number of high resolution channels per chip reducing thus the number of chips required for high resolution applications by a factor of at least 4. A new TDC, the TDC130, has been planned to profit from the speed and integration potential of this technology. A prototype chip has been fabricated to evaluate the timing properties of such a TDC.

The paper describes the architecture of the prototype and of the planned TDC, focussing on the time base. A novel interpolation scheme resulting in bin sizes smaller than a logic gate delay is presented.

II. TDC130 ARCHITECTURE

![Diagram of TDC130 prototype architecture](image)

To evaluate the timing precision that can be reached in the 130 nm technology, a prototype (fig. 2) was fabricated. It contains a Phase Locked Loop (PLL), a Delay Locked Loop (DLL), the hit registers of 32 channels and a band-gap voltage reference for biasing. A programmable noise generator with an independent clock input is implemented. This allows for evaluation of the sensitivity of the circuit to substrate and power supply noise, as it will be generated by the final chip’s
synchronous logic.

The core of the planned TDC130 (fig. 3) is a delay locked loop that provides phase interpolation. Its reference signal, a clock with a period of 780 ps, is generated by an on-chip clock multiplying phase-locked loop from an external (LHC-standard) 40 MHz clock source. The 32 element DLL covers one 780 ps clock cycle, leading to a bin size of 25 ps. A counter, clocked by the DLL’s input clock can be used to extend the dynamic range of the TDC according to the requirements of the application. The DLL is the global timing reference for the 32 TDC channels, which therefore have identical timing properties. Sharing the time base reduces the power consumption per channel. The time stamp, the digital representation of the time of the event, is relative to the 40 MHz input clock. In LHC applications it gives the time within a bunch-crossing interval. As both the PLL clock multiplication factor and the number of DLL elements are a power of 2, the bin size is a binary fraction of 25 ns, the input clock period. Encoding of the measurement is thus simplified. As the TDC130 is targeted at High Energy Physics (HEP) applications, it supports high hit rate of measurements (3 MHz per channel). Every channel will have a dedicated level 1 buffer which is fully independent of other channels. Once an event is signalled at the chip’s input, the value of the 32 phase-shifted DLL outputs is stored in a bank of registers, called hit registers. Data from the hit registers can be transferred to the level 1 buffer once per clock cycle. This is contrary to the HPTDC, where a buffer was shared among 8 channels and access subject to arbitration depending on the other channels’ activity. Triggering is a well established technique to reduce the required readout bandwidth: The time stamps for all the events are stored in the level 1 buffer. A trigger processor selects those events which might be interesting and signals them to all detectors. The trigger signal arrives at each TDC with a fixed latency. Only after this latency, data is read out from the level 1 buffers if a trigger has been received, or discarded otherwise. As the level 1 buffers are dedicated to individual channels, data in the buffers are always in perfect time order, simplifying the trigger logic compared to the HPTDC. The data of all channels of a chip is merged by common processing logic and readout circuitry. As the trigger rate is typically much lower than the hit rate, common circuits can run synchronously with the 40 MHz reference clock. In order to enable the use of the TDC130 in a large variety of applications, it can also be configured for non-triggered applications e.g., in mass spectrometer applications, all measurements have to be processed off-chip, and thus read out. Consequently, no data can be discarded on-chip since no trigger signal is available.

III. TIME BASE ARCHITECTURE

The core of the time base is a DLL (fig. 4). It consists of a Voltage Controlled Delay Line (VCDL), composed of 32 differential buffer delay elements. A clock signal is permanently propagating in this line. Its control logic assures that the propagation delay of the complete line is always equal to one clock cycle. A D flip flop serves as a bang-bang phase detector, comparing the VCDL’s input with its output. A charge pump and a filter capacitor convert the digital phase detector output into a control voltage, which changes the bias current of the VCDL’s delay elements and thus their propagation delay. Temperature and voltage variation effects are consequently automatically compensated for. A start-up state machine avoids that the DLL will lock to the wrong delay. Assuming perfect matching of the delay elements, each individual element’s delay is equal to one clock cycle \( T_{\text{clk}} \) divided by the number of elements \( N \). Let the leading edge arrive at the first delay elements input at time \( t_0 \). If at a later time \( t \), the leading edge is at the input of the \( n \)th element, \( t \) is within \( \pm \frac{T_{\text{clk}}}{2N} \) of \( t_0 = t_0 + \frac{T_{\text{clk}}}{4N} \). Fine tuning of the individual delay element’s bias currents is used to reduce the effects of delay cell mismatch. The hit register banks are connected to the VCDL outputs. Once an event is signalled at the hit register input, the state of the DLL is stored and the position of the leading edge can be determined by digital logic at a later stage.

The dynamic range of a DLL is always limited to one clock cycle. Thus, in order to achieve a useful dynamic range, either the delay line must be very long (high number of delay elements), leading to linearity problems due to mismatch, or the input clock frequency must be very low, limiting the resolution. An alternative is to expand the dynamic range using a clock synchronous counter while using a short VCDL with a high clock frequency. This has proven to be a good solution in the past [1].

One specification to the TDC is the use of the LHC standard 40 MHz clock frequency, but as it has been discussed, a high frequency clock is required for high resolution and high

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**Figure 3:** Full TDC130 architecture

**Figure 4:** A phase-interpolating DLL
linearity. A clock multiplying PLL is used to generate the 1.28 GHz DLL clock based on a 40 MHz input clock. The synchronous logic doesn’t need to run at high frequency and uses the 40 MHz clock.

IV. DELAY ELEMENTS

In the asynchronous domain of the TDC, the timing of signals needs to have a precision comparable to a gate delay. The design is very sensitive to parasitics and needs to be very symmetric. As long as related signals are equally delayed, the conversion linearity is not affected. On the other hand, nonlinearities are caused by e.g. unequal propagation delays between the VCDL outputs and the hit registers. Some global process variations affect PMOS and NMOS transistors independently. Therefore, related signals, such as the VCDL tap outputs, have to have the same polarity. This means that the VCDL’s delay elements have to be all non-inverting. To ease data processing, a constraint put on the TDC is that the bin size must be a binary fraction of the 40 MHz LHC reference clock period, 25 ns. Acceptable bin size are either 25 ps or 50 ps. A bin size of 100 ps has already been achieved by the HPTDC in 250 nm and doesn’t justify the use of a 130 nm technology.

A buffer can be used as delay element, while a single inverter cannot. A single-ended buffer consists of two inverters in series, thus two elementary gates. A differential buffer can be realized in one stage. For the 130 nm CMOS technology used, the minimum delay simulated for a single-ended buffer implemented with low $V_t$ transistors is 45 ps. In order to use them in a DLL, their delay must be adjustable, usually employing a current starving technique. This further increases the minimum delay achievable. The nominal operating point must leave a margin both to higher and to lower delays, leading to a nominal delay considerably higher than 45 ps.

![Delay element with inductive peaking including an adjustable bias current source for mismatch compensation](image)

Differential buffers with adjustable delay may consist of a differential pair, a current source and load elements, usually diode connected transistors [7]. The delay of the buffer depends on the current provided by the tap current source. In the DLL, the bias voltage is not constant, but generated by the DLL control logic. Simulations show a delay of about 32 ps under nominal conditions and below 45 ps in worst case. Replacing the diode connected transistor load elements by transistors with series gate resistors (active inductors) (fig. 5) such that they show inductive properties around the operating frequency of the delay element, this delay can be further reduced, reaching a bin size of 25 ps. For such a small buffer delay, mismatch effects can significantly degrade the linearity of the TDC. To compensate for this, the tail current of each VCDL delay element is trimmed by using an additional, individually configurable current source, as shown in fig. 5.

Using differential delay elements implies a conversion from differential to single-ended at some point in the asynchronous domain. Convenient is a conversion either immediately after the VCDL tap outputs or after the hit registers. In the latter case, the differential signals need to be propagated from the VCDL to the hit registers and the hit registers have to be differential. Both single-ended and differential hit registers have been simulated and their performance compared. The simulations were done under the constraint that the differential and single-ended registers would have to have the same recovery time from the metastable state. This leads to a supply current of 1 mA for a differential register, while the single-ended implementation only takes 54 $\mu$A in nominal operating conditions. The noise, i.e. the standard deviation of the supply current, generated by the differential register is lower than that of the single-ended one only in relative terms compared to the average supply current. In absolute terms, the differential register’s noise is slightly higher than the noise generated by the single-ended registers. For these two reasons, lower power consumption and lower supply noise, it has been decided to use single-ended hit registers and perform the conversion immediately after the VCDL.

V. PERFORMANCE ENHANCEMENT

For even higher resolution ($\approx 6$ ps) a novel interpolation scheme (fig. 6) is planned.

The reference clock signal is propagated through a second DLL with an $M$ element VCDL, which, on the contrary to the $N$ element main DLL, does lock to a fraction of the period $m/n$ of the reference clock. The phase detector is connected to the end of the $M$ element DLL and to the input of the $m$th element of the main DLL. The second DLL generates a control voltage $V_{Ctrl2}$ such that its element’s delay $t_M = \frac{m}{F} t_N$. An interpolation factor of $F = 4$ can be reached with $M = 4$ and $m = 5$: $t_M = \frac{5}{4} t_N = \left(1 + \frac{1}{4}\right) t_N$. Note that integer delays of $t_N$ correspond to a shift of the time stamp in the hit register and can therefore be disregarded. If the control voltage $V_{Ctrl2}$ is propagated to other delay elements which are equal to those inside the DLL, their delays are (in first approximation) identical. The incoming hit signals are propagated though a delay line composed of $F - 1 = 3$ elements with a delay $t_M$ with tap outputs before every element and after the last. A bank of hit registers is connected to each tap output. The reference clock signal is propagating though the two DLLs, but the delay lines in the channels carry the hit signals. As a result, an interpolation scheme similar to the RC fine interpolation of the HPTDC can be achieved while taking advantage of the auto-calibration property of DLLs.
Arrays of DLLs [8] can also provide sub-element delays using auto-calibrating DLLs without the need to distribute an analogue control voltage across the channels. Unfortunately, they cannot be built with a number of elements which is a power of 2. In addition, the reference clock signal is permanently propagating though all DLLs, increasing the power consumption. Furthermore, a large number of signals needs to be distributed across the chip, requiring large buffers. Each buffer dissipates roughly as much power as one delay element. The architecture proposed here is thus more efficient from both the area and the power consumption point of view.

VI. POWER CONSUMPTION

The prototype’s power consumption is estimated to be 300 mW. For comparison, the previous HPTDC, including synchronous logic, not present in the TDC130 prototype, consumes 1300 mW in high resolution (100 ps) mode.

VII. SUMMARY

A high resolution TDC in a standard 130 nm technology has been planned and a prototype fabricated to evaluate the resolution of the proposed VCDL circuit. Experimental verification is being prepared. A novel interpolation scheme has been described and will be implemented in a future prototype.

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Skiroc : a Front-end Chip to Read Out the Imaging Silicon-Tungsten Calorimeter for ILC

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Abstract
Integration and low-power consumption of the read-out ASIC for the International Linear Collider (ILC) 82-million-channel W-Si calorimeter must reach an unprecedented level as it will be embedded inside the detector. Uniformity and dynamic range performance has to reach the accuracy to achieve calorimetric measurement. A first step towards this goal has been a 10,000-channel physics prototype of 18*18 cm which was in test beam in Fermilab in summer 2008.

A new version of a full integrated read out chip (SKIROC) has been designed to equip the technologic prototype to be built for 2009. Based on the running physics prototype ASIC (FLC_PHY3), it embeds most of the required features expected for the final detector.

The dynamic range has been improved from 500 to 2000 MIP. An auto-trigger capability has been added allowing built-in zero suppress. The number of channel has been doubled reaching 36 to fit smaller silicon pads and the low-noise charge preamplifier now accepts both AC and DC coupled detectors. After an exhaustive description, the measurement results of that new front-end chip will be presented. The results on the technological R&D conducted on the ultra-thin PCB hosting both the front-end electronic and the silicon detectors will also be described.

I - INTRODUCTION
Integration and low-power consumption of the read-out ASIC for the International Linear Collider (ILC) 82-million-channel W-Si calorimeter must reach an unprecedented level as it will be embedded inside the detector. Uniformity and dynamic range performance has to reach the accuracy to achieve calorimetric measurement. A first step towards this goal has been a 10,000-channel physics prototype of 18*18 cm which is currently in test beam in Fermilab.

A new front-end chip called SKIROC – standing for Silikon Kalorimeter Read-Out Chip – has been designed to read-out the upcoming generation of Si-W calorimeter featuring ILC requirements. The analogue core of SKIROC is based on the front-end electronic designed for that physics prototype. The Maximum input charge has been extended from 500 to 2000 MIP. The number of channel has been doubled – reaching 36 - to fit a pad size reduction in the silicon detector design conducted concurrently. A stand alone working capability comes along with the full power pulsing feature. That means SKIROC does not need any external component such as decoupling capacitance or bias resistor involving a huge room saving. The wake up sequence duration of the power pulsing is around 2µs to ensure a lower than 1% duty cycle in an ILC-like beam structure [1], involving more than two order of magnitude of power saving.

Beyond the analogue core improvement, many features have been implemented in SKIROC. A channel by channel auto-trigger capability has been added allowing a built-in zero suppress. A multi-channel ADC is embedded. The trigger and gain selection threshold is set by an internal dual DAC. Voltage references used in the analogue core use a bandgap reference [2]. A digital core driving all the analogue features and the digital communication with the DAQ has been designed and is implemented in a FPGA to get debugged and improved before being embedded in the next version.

Fig. 1 – ILC beam structure and electronic sequence
That proceeding will describe the SKIROC chip and present results of the first prototype.

II – SKIROC DESCRIPTION

SKIROC is a 36-channel front-end chip designed to read-out silicon PIN diodes for calorimetry application. It has been designed in a general framework ensuring consistent back-end of different front-end ASIC for several calorimeters (HaRDROC to read out the digital RPC HCAL prototype and SPIROC to read out the SiPM and Sci tiles HCAL prototype are the two others chip existing on that framework).

Its main characteristics are the following:

- AMS SiGe 0.35μm technology
- 20mm² (4mm × 5mm) area
- 3.3V power supply
- Package: CQFP240

Each channel is made of a variable-gain low-noise charge preamplifier followed by both a dual shaper – one with a gain 1 and the other with a gain 10 - to filter the charge measurement and a trigger chain composed of a high gain fast shaper and a discriminator. The measured charge is stored in a 5-depth SCA that can be read either in an analogue way or can be connected to a multi-channel 12 bit Wilkinson ADC. Thresholds are set with a 10-bit DAC for trigger level and for automatic gain selection level. A bandgap ensures the stability versus supply voltage and temperature for all the requested reference in the analogue core.

The digital signals requested for digital and analogue block communications are outputted using a dynamic multiplexing to reduce the pin count while emulating the digital core in a FPGA.

III – SKIROC MEASUREMENTS

The analogue core of SKIROC has been extensively measured to validate the performance to achieve calorimetric measurement. The pedestal dispersion on the 36 channels is 1.8mV RMS for gain 1 and 2.1 mV for gain 10. These results fit well the statistic dispersion calculated from technology parameters according to transistor size and architecture. That result shows that the layout is correct and does not add neither additional dispersion nor pedestal pattern over the 36 channel. Results on that measurement are shown on Fig. 5.

The linearity on SKIROC has been measured and fit well the simulation. Due to minor bug in the internal ADC and in the probe bus that allows to check the linearity in an analogue way by probing the output of the slow shaper, it is not possible to extend the measurement to the whole dynamic range. These two bugs are corrected in the next iteration of SKIROC. The linearity is measured ion the two first third of the dynamic range to better than 0.5%. Measurement of that
linearity is shown on Fig. 6 and includes simulation, analogue measurement and digital measurement using the internal 12 bit multichannel Wilkinson ADC.

![SKIROC linearity results](image1)

**Fig 6 – SKIROC Linearity**

The noise and channel dispersion has been measured through the whole acquisition chain including analogue channel, track and hold and internal Wilkinson ADC. These results are shown in Fig. 7 to 9. These results show that the internal does not add significant noise compared to the analogue measurement and validate therefore the use of an internal ADC in terms of noise and digital to analogue coupling.

![Fig 7 – Channel noise, Gain 1](image2)

![Fig 8 – Channel dispersion, Gain 1](image3)

![Fig 9 – Channel noise, Gain 10](image4)

![Fig 10 – Channel dispersion, Gain 10](image5)

The equivalent noise charge of the preamplifier is measured around 2000 electrons. After shaping, the simulated MIP to noise ratio is 16 for the trigger line and 11 for the charge measurement. The measurement done on these points shows some non-expected Gaussian noise on both charge measurement and trigger line. The MIP to noise ratio drops to 8 for the charge measurement while it is not well characterized for the trigger path. Crosstalk is around the per mil level in simulation and in measurement.
The bandgap characterization made on a building block shows a 10ppm/°C drift ensuring the stability of the pedestal with temperature. The stability of the voltage reference with power supply is ensured for supply included within 2.8V to 3.8V for a nominal value of 3.3V. A bug in SKIROC Bandgap power pulsing degrades these performances, it has been corrected for the next iteration.

The DAC performances are within expectation by showing a ‘static ENOB’ of 9.5 bit for a 10 bit DAC. These two internal DAC allows to tune the trigger threshold and the automatic gain selection value.

![Fig 11 – Dual DAC linearity measurement](image)

SKIROC is announced for March 2009 and will embed many of SKIROC1 blocks that has been validated by the above measurements.

**IV – CONCLUSION**

The SKIROC chips will be used to equip the 40,000-channel ECAL foreseen for 2009 that will validate the technological choices for the 82-million-channel final detector. Many of the final detector requested features have been embedded and the performance has been greatly improved compared to the physics prototype front-end chip. The production of that ASIC is foreseen in summer 2008 to be able to take data in 2009, before the engineering design report of the final detector planned for 2010 by the ILC Worldwide Study Bureau.

**V – REFERENCES**

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Testing and calibrating analogue inputs to the ATLAS Level-1 Calorimeter Trigger


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Abstract

The ATLAS Level-1 Calorimeter Trigger is a hardware-based system which aims to identify objects with high transverse momentum within an overall latency of 2.5 $\mu$s. It is composed of a PreProcessor system (PPr) which digitises 7200 analogue input channels, determines the bunch crossing of the interaction, applies a digital noise filter, and provides a fine calibration; and two subsequent digital processors. The PreProcessor system needs various channel dependent parameters to be set in order to provide digital signals which are aligned in time and have proper energy calibration. The different techniques which are used to derive these parameters are described along with the quality tests of the analogue input signals.

I. INTRODUCTION

The enormous rate of proton-proton interactions provided by the LHC machine and the limited readout bandwidth pose strong requirements on the online event selection process. The ATLAS Trigger system is therefore composed of three levels with the first level being entirely realised in programmable hardware. The two subsequent levels are implemented as large computer farms with up to around 2000 nodes divided between the two trigger levels.

The LHC machine collides bunches of protons every 25 ns with about 23 inelastic interactions per bunch crossing at the design luminosity of $10^{34} \, cm^{-2} \, s^{-1}$. The first-level trigger is a rate reduction from the bunch crossing rate of 40 MHz to a maximum of 75 kHz using a strategy based on the search for high $p_T$ objects such as electrons, jets, muons, etc. The calorimeter trigger combined with the muon trigger and the Central Trigger Processor form the first-level trigger of the ATLAS experiment [1]. The calorimeter trigger [1, 2, 3] is itself composed of a PreProcessor system (PPr) which feeds data into two parallel digital processor systems. The PreProcessor system digitises about 7200 analogue calorimeter signals and determines the bunch crossing of the corresponding primary interaction. The Cluster Processor (CP) searches for electron, photon and tau candidates. The Jet/Energy-sum Processor (JEP) searches for jets and determines the missing transverse energy and the total transverse energy. In addition to the main building blocks there are several additional components satisfying various infrastructural purposes which are used in the system for clock distribution, configuration and monitoring etc.

II. PREPROCESSOR SYSTEM

Figure 1: The signal processing chain consists of three steps: digitisation of the analogue signals, determination of the corresponding bunch crossing and finally a fine calibration of the transverse energy measurement.

The main purposes of the PreProcessor system are the digi-
tisation of the analogue input signals, the determination of the bunch crossing of the primary interaction and a precisely calibrated transverse energy measurement. These three logical steps as indicated in figure 1 are the basis for the hardware design of the PreProcessor system. The complete system consists of 124 9U VME boards in 8 crates which cover the full calorimeter area with about 7200 trigger channels. Each PreProcessor Module (PPM) processes 64 channels in parallel. It consists of a main board with a total of 23 daughter boards as can be seen in figure 2. The real-time signal processing is performed entirely on the daughter cards.

The Analogue Input Cards (the four daughter boards seen on the left side of figure 2) condition the signals and pass them to 16 Multi Chip Modules (MCMs) which each process four channels. These MCMs (shown in figure 3) [5] form the core of the PPM processing consisting of digitisation and the subsequent bunch crossing identification using a digital filter. A noise cut and the fine calibration are performed using a programmable look-up table (LUT). The digital signal processing is performed by a custom-designed application-specific integrated circuit (ASIC) which holds additional functionality for debugging and system tests (e.g. monitoring, playback memories, etc.).

After some further processing (e.g. pre-summing of channels for the JEP system which works at lower granularity than the CP system) also performed in the ASIC, the information is serialised and sent using a further daughter card to the Processor Module. Subsequently, the bunch-crossing identification is added mostly cover a region of $5 \times 5 \, \text{m}^2$ in the $\eta - \phi$ space and are called trigger towers. The Calorimeter Trigger processes signals from about 7200 of these trigger towers. Both calorimeters have pulser systems which are able to inject charge into the electronic chain with high signal accuracy and time stability. This is of paramount importance for the timing and energy calibration procedures.

The analogue trigger signals from the calorimeters are routed through $30 - 80 \, \text{m}$ long cables to a separate receiver system [6], situated next to the calorimeter trigger electronics, where they are conditioned. The trigger is designed to process transverse energies; e.m. calorimeter signals arrive in that form, but the gains of hadronic calorimeter signals must be adjusted. The receivers include variable-gain amplifiers that also provide precise gain calibration. A system of patch panels before and after the receiver system provides correct signal distribution to the corresponding PreProcessor Modules.

The differential signals are routed using stiff analogue cables carrying 16 channels each to the front panels of the PPMs. The signals are transformed to single-ended signals and shifted into the appropriate voltage window for the FADC. This processing takes place on Analog Input Cards which handle 16 channels each. Figure 4 shows the two parts of the differential pair for one channel of an LAr calorimeter pulse (double pulse) which was recorded with an oscilloscope at the input to the PPr.

The single-ended signals are then directed to 16 Multi Chip Modules (MCMs) which each process four channels. On the MCMs 10 bit FADCs perform the digitisation using a strobe adjustable in 1 ns steps under control of a special timing chip on the MCM. Subsequently, the bunch-crossing identification is
done using a Finite-Impulse-Response (FIR) filter, and the fine calibration and compensation for possible non-linearities is performed using a look-up table.

The digital processing is entirely done within the custom designed ASIC. After digitisation the data are stored in a pipeline memory from which they can be read out after receipt of an L1 Accept signal from the central trigger processor. Figure 5 shows a complete pipeline readout with signals from the LAr and the Tile calorimeter.

In addition to these timing parameters which influence the real time data path a further important parameter needs to be adjusted, the readout pointer which determines the position in the pipeline memory where data have to be read upon receipt of an L1 Accept signal. The data readout itself is not essential for the trigger functionality. However it is needed for verification of the trigger decision and monitoring its performance. It is in addition involved in various calibration procedures and therefore essential for the operation of the system. In standard running condition for each channel 5 FADC slices are read with the slice corresponding to the bunch crossing in the center together with the final LUT output value.

The ASIC implements a Finite-Impulse-Response (FIR) filter for noise suppression which, together with peak-finding logic, is used to determine the bunch crossing of the interaction. Five consecutive samplings from the FADCs contribute to the input of the filter. The coefficients of the filter, which depend on the pulse shape of the signals from the calorimeter, need to be determined in order to increase the efficiency for detecting low energy objects in particular.

The noise cut needs to be determined and implemented in the look-up table to suppress positive trigger decisions due to statistical fluctuations. The energy calibration can be performed using two systems, the variable gain amplifiers of the receiver system and with somewhat less accuracy the LUT of the Pre-Processor system. The LUT is however able to compensate for possible non-linearities.

The number of parameters fed into the system is quite large, and due to the fact that some are interdependent, a proper strategy needs to be in place in order to determine all parameters. This should be in place prior to colliding beams to guarantee a timely startup and availability of the system. The strategy consists of several steps which sometimes need iterations in or-

Figure 6: Dataflow scheme for the processing on the PPr MCMs. The adjustable timing parameters are indicated. (Sampling timing for the FADC (PPrPhos4), Input timing delay (SyncDelayRaw) and the read-out pointer for the pipeline memory (PipeDelayRaw).)

IV. THE CALIBRATION PARAMETERS AND STRATEGY

A large set of channel dependent and global parameters have to be adjusted in order to align all channels in time at the output stage of the PreProcessor with proper energy calibration. The input timing needs to be adjusted in order to compensate for different signal delays due to different cable lengths from the detector to the PPr. It can be done with steps of 25 ns corresponding to the time between two LHC bunch crossings (BC) by adjusting input pipeline delays as indicated in figure 6. This is important for the overall timing of the trigger and a correct trigger decision since the processors expect the signals which they receive to all belong to the same LHC bunch crossing.
order to check and refine the chosen settings.

- The readout and input timing needs to be determined in a first step in order to align all channels to the same BC and to be able to read out correct data for the further steps of the calibration procedure.

- The fine timing needs to be set correctly before any calibration can be applied in order to avoid a systematic bias from not sampling the pulses at their maximum value.

- The next step consists in a determination of the FIR filter settings to suppress noise.

- After a proper study of the channel dependent noise behaviour a noise cut can be chosen.

- At the last stage the energy calibration constants need to be determined and set at the Receiver level with possible corrections for non-linearities in the LUT.

V. THE TIMING CALIBRATION

A. Readout and Coarse Input Timing

The readout pointer, i.e. the position in the pipeline memory which holds the data for a certain BC corresponding to a L1 Accept signal, can be determined with a pulser run where parts of the system are enabled for triggering. It depends only on the time needed for the processing by the CP and JEP systems, signal transmission to the CTP and the signal transmission of the L1 Accept signal back from the CTP to the PPr. A scan subsequently reads out all parts of the pipeline memory and a fast data analysis determines the exact pulse position which produced the positive trigger decision. The readout timing is independent of the incoming signals and solely depends on the signal propagation downstream from the PPr. It can therefore be determined with a pulser run and keeps its validity also for collision data.

The coarse input timing is meant to compensate for different cable delays from the detector. As for the readout timing it can be determined with a pulser run. In practice all the input delays are set to the same value. A Readout Pointer Scan is performed which results in different readout pointers for different channels. After that all Readout pointers are set to the same value and the input delays are corrected accordingly. In order to minimize the latency of the system, the combination of the global readout pointers and channel dependent input delays is chosen such that the input delay of the channel with the largest cable length is set to zero. This choice determines unambiguously the readout pointer and the input delays of the other channels.

In contrast to the readout pointer, the input delays measured by this method are only approximately valid for collision data since the timing between channels is not necessarily the same for the pulser system and collision data. Therefore small changes of the input timing (about 1 BC for some channels) might be necessary for future collision data.

B. Fine Timing

The goal is to set the proper fine timing with an accuracy of a few ns in order to guarantee a proper energy measurement. Using a pulser run these settings can be found rather easily with a timing scan where all 25 different settings are applied and for each setting a certain number of events are taken. For each step the mean values of the sampled data are then calculated for the 5 FADC slices. This results in a ns accuracy sampling over 125 ns and therefore covers the main part of the pulses. A proper fit to these data determines the position of the maximum of the pulses. An example of such a scan (here with 20 samples read out instead of 5) is shown in the upper left plot of figure 7.

Figure 7: Fine timing studies: upper left - fine timing scan of a pulser run with ns accuracy overlaid with a fit, upper right: 5 FADC samples overlaid with a fit (after pedestal subtraction), lower: correlation of results from a fine timing scan with fits to individual signals.

However this method applies only for pulser runs, while for collision data all pulses have different pulse height which makes it nearly impossible to combine data from different events and to reconstruct the pulse shape. Therefore a method has been developed where single pulses are fitted with the position of the maximum being one of the free parameters of the fit. The upper right plot of figure 7 shows an example of such a fit where the fitted function consists of a gaussian part for the rising edge and a landau function for the falling part of the signal. Both functions are matched at the maximum and the widths of both function has been determined from a fine timing scan performed before thus leading to two free parameters in the fit being the signal height and the position of the maximum.

The lower plot of figure 7 shows the correlation of the fine timing scan and the fitting results of single pulses. Since the correlation is very good this method proves to be a promising technique for analysing collision data. However it involves a detailed understanding of the pulse shapes which is not a priori given for real pulses. However it might be possible to study the pulse shape from large samples of real data. Currently further systematic studies are being performed in order to test the
VI. The Pedestal Calibration and Noise Determination

The first step towards a proper energy calibration consists in the determination of the DAC value which conditions the signals on the AnIn boards by shifting the signal in the appropriate voltage window for the FADC. This effectively determines the pedestal value of the FADC. In order to achieve this a scan of the possible 8-bit DAC values is performed and the output of the FADC is recorded. A fast data analysis determines automatically the DAC value which corresponds to the chosen pedestal value. Currently a pedestal value of 40 is chosen in order to capture the full signal amplitude even with its negative undershoot in case of the bipolar LAr pulses. Figure 8 shows a DAC-scan for a single channel and the corresponding pedestal distribution for a large number of events after adjusting the DAC values based on the scan results. The RMS of the pedestal distribution is used for the determination of the noise cut which is subsequently implemented in the LUT.

VII. The Energy Calibration

A proper energy calibration is needed in order to achieve steep turn-on curves for the trigger items being used. The baseline of our calibration is the energy being measured through the standard calorimeter readout. In the circumstance that various corrections (e.g. dead material, crack losses, etc.) are used the calorimeter calibration, they will directly enter the trigger calibration as well. Currently an electronic calibration is performed which aims to shift the energy measured by the trigger to the values measured by the calorimeter. The left plot in figure 9 shows the FADC distribution for the maximum within a pulse. It should be noted that the width of the distribution is much smaller than for real calorimeter signals since it originates from charge injection into the electronic chain neglecting any calorimeter sampling effects. The right plot compares the energies of the trigger (red) with the calorimeter (black). The essentially uncalibrated trigger agrees already very well with the calorimeter measurement and this is also confirmed by studies using cosmic muons [3]. Before the restart of the LHC in early spring 2009 a detailed analysis of pulser runs will help to achieve further substantial improvements.

Figure 8: left: measured pedestal w.r.t. the DAC value for a single channel, right: pedestal distribution after adjustment of the DAC value with a gaussian fit overlaid.

Figure 9: left: ADC distribution for the maximum of a constant pulse measured in the PPr, right: comparison of measured transverse energies for a collection of channels (red – PPr measurement, black – calorimeter readout)

VIII. Summary

After a successful installation and early commissioning phase of the ATLAS Level-1 Calorimeter trigger, the focus has shifted towards the calibration of the various timing and energy determination settings and a strategy has been set up. The first step consists in the determination of various timing settings, which is largely done using pulser runs and cosmic data taking and only small modifications expected for collision data taking. A study of the fine timing settings based on fitting individual pulses has been performed and seems to be applicable for colliding beam data. Currently detailed studies on energy calibration are being done with the aim to further improve the already reasonable energy calibration.

Acknowledgements

We wish to acknowledge the work of the ATLAS TDAQ community in providing the underlying online software and infrastructure for triggering, read-out and dataflow. We would also like to thank the ATLAS calorimeter communities, in particular those working on the trigger tower builders and receivers, for their efforts to provide genuine input signals to the trigger. Finally the successful installation of the infrastructure and cabling would have been impossible without the careful work of many technicians connected to the institutes involved.

References

Abstract

During the past years our group has built, calibrated, and finally installed all the components of the Muon Barrel Alignment System for the CMS experiment. This paper covers the results of the hardware commissioning, the full system setup and the connection to the CMS Detector Control System (DCS). The step-by-step operation of the system is discussed: from collecting the analog video signals and preprocessing the observed LED images, through controlling the front-end PCs, to forming the measurement results for the CMS DCS. The first measurement results and the initial experiences of the communication with the DCS are also discussed.

I. SYSTEM OVERVIEW

In order to provide reliable muon track parameters and therefore good muon momentum resolution of the CMS experiment, the positions of all 250 Barrel Muon chambers (DT) have to be measured with an accuracy of 150-350 micrometer (depending on their radial distance from the interaction point). Due to the size of the CMS barrel region and the fact that the muon chambers are embedded into the magnet yoke a novel system had to be developed that can cope with both the high magnetic field and the radiation background at a tolerable price.

The CMS Muon Barrel Alignment System, described in more detail in [2], is schematically shown in Fig.1.

According to the concept, about 10000 LED sources are mounted on the 250 DTs. Centroids of these LEDs are then measured by about 600 cameras installed on 36 rigid structures called MABs (Module for Alignment of the Barrel). Furthermore, several MABs hold so called diagonal LEDs and therefore can be observed by the others, while other MABs can observe LEDs mounted directly on the outer shell of the CMS solenoid magnet. This kind of connection between the LEDs, cameras and the MABs therefore forms an opto-mechanical network. The positions of their elements can be reconstructed from the measured data and the calibration constants that have been determined before the full system installation.

II. OPERATION OF THE SYSTEM

Each MAB is equipped with its own intelligent module, that is capable of processing the analog signals of the cameras and is able to control the LEDs mounted on the MAB. The module is also responsible for reading the temperature and relative humidity (RH) sensors of the MAB. This module consists of a PC-104 type PC and a FrameLocker type video image grabber card.

The module is also equipped with a custom designed board (CustomBoard) that is able to multiplex analog video signals, to control LEDs and to read out the temperature/RH sensors. Altogether this module is referred to as BoardPC (Fig.2). The BoardPCs run a customized Linux, which is stored on a central server. On bootup this Linux system is loaded via network using DHCP, TFTP and NFS.

Together with the operating system, two custom built applications are also downloaded. They provide services that are available through TCP/IP protocol. One of them is
As was described before, the LEDs of the System are mechanically connected to the DT chambers. However, they are not directly mounted on these chambers but rather on an opto-mechanical reference body called a Fork (Fig.3). The Forks have been precalibrated and, therefore, the position of every LED is known in the frame of the Fork. During a second calibration phase these Forks were mounted on the chambers and their positions were reconstructed and therefore can be used as a calibration parameter. This object-like approach of the system’s components results in a better overall performance of the alignment system as has been proven by simulations at an early stage of the development. Furthermore, Forks act as driver units for the LEDs since they contain a microcontroller-based intelligent circuit that can be used as a calibration parameter. This object-like approach of the system’s components results in a better overall performance of the alignment system as has been proven by simulations at an early stage of the development. Furthermore, Forks act as driver units for the LEDs since they contain a microcontroller-based intelligent circuit that can be reached via I²C bus. I²C master devices are embedded into each DT chamber’s control and data taking unit, called a MiniCrate. MiniCrates, and hence the Forks, can be reached via a custom protocol through their server machines. If a need for switching on a LED arises, our system sends a command to one of the five MiniCrate servers, where it is then translated to an I²C message that is then sent out to the destination Fork. This scheme prevents the Alignment System from requiring a separate power and data network in parallel to the existing DT readout and power network.

There is a 37th PC called the Measurement Control Machine (MCM). This is a standard rack-mount PC situated in the electronics cavern of the CMS experiment. This machine is equipped with two NICs and therefore acts as an interface machine between the CMS network and the Alignment’s intranet containing all the BoardPCs. Besides acting as a boot server the MCM controls all aspects of the measurement. The measurement control abilities are realised in a Java-based control software: it sends out commands for switching the LEDs on and off and also instructs BoardPCs to measure centroids. The MCM then collects the measured data and, by using predetermined reference values, it eliminates false results due to reflections of the LED’s light (cf. paragraph V).

### III. THE MEASUREMENT CYCLE

The measurement cycle of the system is as follows: capture of images from all the LED light sources by the corresponding video-cameras, calculation of the centroids of the light spots in the images and storage of all the output information. To perform a measurement cycle first all the possible and enabled optical connections have to be recorded in the construction database. To do this all the light sources have to be checked by the corresponding video-cameras and the connections with inadequate image quality (e.g. the light is blocked, distorted or too weak) have to be excluded. This operation of creating the initial set of possible connections was part of the system commissioning procedure and it is not repeated later, unless necessary. After this operation the system is ready to take data. During regular operation the conditions might, of course, change and different quality-check and time-out procedures assure that only good quality images are accepted.

The number of optical connections is very high (equal to the number of LED light sources) and there are several conditions to measure a given connection at a certain moment. These conditions are as follows:

1. The BoardPCs are independent of each other and can work in parallel
2. Only one camera can work on the same MAB at a time (limit of the multiplexing of the video-signal)
3. LEDs observed by the same camera are measured one by one
4. Only a few LEDs can be on at a time on a chamber (current limit)

Only those measurements that do not contravene these conditions at the given moment, can be processed.

The measurement cycle consists of the following steps:

1. The list of connections to be measured is obtained from the construction database.
2. The possibility to execute the measurement of the next connection on the list is checked according to the rules above. If “yes” then the execution command is given and the rule-parameters are set in order to prevent the execution of any interfering measurement. When the measurement is finished then the given connection is marked as “done” and the condition parameters are released.
3. Without waiting for the result of any measurement the next connection not yet measured is checked to ascertain whether the measurement is possible. If “yes” the measurement is executed for the given connection, as in step 2, above. If “no”, the connection is skipped. This allows the parallel operation of all the available MABs and their BoardPCs.
4. Upon reaching the end of the connection list, it is repeated until all the measurements are done, which is the end of the measurement cycle.
This procedure, called “dynamic measurement control” (Fig. 4), turned out to be very efficient and was able to guarantee parallel work of all the MABs. Of course, the sequence of the measurements may vary from cycle to cycle. The most critical limiting factor that determines the duration of the measurement cycle is that only one camera per MAB can work at a time and it is observing one LED at a time. The measurement time for one optical connection (grabbing 20 images, calculating the centroids, and communication between the given BoardPC and the main workstation) is about 20 seconds. As the maximum number of connections which has to be measured by the MABs is 400 (on Wheels +/- 1), the theoretical minimum duration of the full measurement cycle is about 2 hours. This expected duration is verified during the full setup. However, if there is a hardware failure or bad communication to any parts of the system this time can be considerably larger due to the timeout settings. In order to keep the measurement duration low (and therefore maintain the daily measurement frequency at an acceptable level), all the faulty hardware has to be excluded from the measurement.

**IV. THE DATA-FLOW – INTEGRATION INTO THE CMS**

The Measurement Control collects data from the BoardPCs via a custom protocol over TCP/IP. These data are then collected and archived on the CMS online Oracle-based database system (called omds), to which our Measurement Control software connects via the JDBC mechanism. Since omds cannot be reached from outside of the experiment due to safety reasons we had to organise the transport of the measured data to the offline CERN Analysis Facility (CAF). Data from the Alignment System are regarded as an ‘event’ and therefore are transported according to the events’ transport rule. In order to be able to be read by the reconstruction code all measured data have to be written into a ROOT file. This task is performed by a custom ROOT script. Besides reading and saving centroid data of the given run number, it reads and saves data of the temperature/RH sensors as well as the configuration of the measurement itself. As soon as these data are encapsulated into a ROOT file its transfer to the CAF is initiated by a Perl script. During the start-up phase of the experiment the ROOT file generation and the transfer are started manually. During the physics runs, however, this feature will be implemented into the Measurement Control.

Further processing and quality checks are planned on the data delivered to the CAF before they are finally fed into the main reconstruction process. It is also possible, however, to write these data back to an offline database thus allowing statistical analysis of the data from multiple runs. These processes are not yet settled.
In order to deliver online status information, our Measurement Control is connected into the CMS Detector Control System (DCS) which is a standardized approach of the slow control of the detector. It is written in the PVSS industrial process visualising and management software/framework and implements the Finite State Machine (FSM) model.

According to the FSM model our Measurement Control reports its states and receives commands from the upper level in the control hierarchy. Due to the requirements of the DCS and to provide a graphical user interface of the Measurement Control we had to write a control script in PVSS (Fig.5). Connection between this script and the Measurement Control is based on a custom TCP/IP protocol called DIM developed by CERN.

In addition, from this control script all the power modules of the Alignment System can be reached and controlled. From the power and the Measurement Control states this PVSS script creates an overall state of the Barrel Alignment that can be reported upwards.

V. RESULTS OF THE COMMISSIONING

The LEDs are situated inside a rectangular tube called the alignment passage on the DT. Therefore, besides the direct image of a LED its reflected images can also be expected. Since our reconstruction needs only the centroid of the direct image, a filtering of the reflections is inevitable. Due to the tube structure the separation of direct images from the reflections can be made on a simple geometrical basis. For example in Fig.7 a real image can be seen that was taken of forks installed in a chamber. Larger dots belong to the closer fork, while the smaller dots are spots of the farther fork.
Figure 7: Direct and reflected images taken on two forks installed on a chamber. Larger spots belong to the closer fork while smaller spots are of the farther one. Spots inside the red markers are direct images. If reference is suitably defined on a fork, spots closest to this reference can be regarded as direct spots.

The real spots can be seen inside the red markers. All the other spots are reflections. Therefore on each fork the points closest to a suitably defined reference (marked with yellow cross) can be regarded as direct spots, while others can be classified as reflections that are to be rejected. Unfortunately, this process is not automated and therefore it requires a fairly large human effort to check all 600 cameras after installation.

Figure 8: On this real image not every spot of the closer fork can be seen. Discarding un-observable direct spots helps to minimize errors arising from false spot measurements.

However, as it was experienced during the MTCC, the repositioning of a barrel-wheel is so good that it is expected that there would be no need to repeat such a process unless the MAB is taken out for maintenance.

The commissioning phase had another task, also: to discover all the hardware failures and imperfections and provide inputs for the exclusion procedure. During this process our personnel had to check all the possible optical lines. In order to speed up this process they could use the hardware configuration data stored in the omds. This allowed the verification of these data, too. This process is also time-consuming, but could be performed simultaneously with the reflection rejection procedure. In the future, however, our group plans to automate this process.

During the commissioning phase 1744 individual measurements had to be discarded due to either the imperfect geometry of the CMS barrel or various hardware failures. This represents 19.2% of the total 9072 optical lines. It is in good agreement with the expected failure rate as many LEDs were installed to cover a larger range of visibility in case of imperfect positioning of the barrel wheels or the DTs. Therefore this failure is tolerable in such a redundant system. Furthermore, since the discarded measurements are more or less evenly distributed in the full barrel their impact on the precision that can be achieved by the Muon Barrel Alignment system is small.

VI. SUMMARY

In 2007 and early 2008 our group has completed the installation of all the hardware elements of the Muon Barrel Alignment System of the CMS experiment at CERN. During the following commissioning phase we have checked all the hardware elements and determined all the parameters needed for the reliable operation of the system. During this phase we had to exclude 19.2% of the total 9072 optical lines. This is in good accordance with the exclusion rate and therefore tolerable for the full system which is ready to take data.

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VII. REFERENCES

CMS Tracker, ECAL and Pixel Optical Cabling: Installation and Performance Verification

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Abstract

The installation of 52304 optical links for the readout and control of the CMS Tracker, ECAL and Pixel detectors is complete. 768 96-way optical cables were installed and tested using an optical time-domain reflectometer. The testing was followed by connections at high density optical fibre patch-panels. Finally, a further round of testing and troubleshooting following feedback from system commissioning with the Tracker Data Acquisition was carried out. Over 90% of the faults found were recovered, resulting overall in only 0.1% of dead optical link channels in the CMS Tracker.

I. INTRODUCTION

The Compact Muon Solenoid (CMS) [1] is one of two general purpose detectors at the CERN Large Hadron Collider (LHC) that began operation in 2008. The Pixel, Silicon Tracker and ECAL¹ sub-detectors, whose locations within the CMS detector are shown in Fig. 1, all use similar point-to-point optical links [2,3,4,5] for control and readout. These are based on 1310 nm edge-emitting lasers, InGaAs photodiodes and single-mode optical fibre cables. The Tracker uses a total of 39240 optical links, the Pixel 1456, the ECAL Barrel 7272, the ECAL End-Caps 4124 and the Preshower1592.

The optical readout links are either analogue (Tracker and Pixel) or digital (ECAL), while the control links are digital with identical structure in all cases. Lasers and photodiodes are integrated onto opto-hybrids at the front-end and VME (FED/DCC/TCC and FEC/CCS) cards at the back-end as illustrated in Fig. 2.

The final optical cabling, connections and tests took place in 2007 and 2008 as part of the overall CMS integration and services installation project. The Cabling and connection experience, Quality Control (QC) activities and early results on the link performance verification are reported in the following sections.

Figure 1: Exploded view of the CMS detector. Two barrel wheels and three end-cap disks for each side of the central barrel yoke (YB0) are movable along the axial direction. ECAL End-Caps and Preshower are installed on the first end-cap yoke pieces (YE+1 and YE-1).

¹ Electromagnetic CALorimeter.
II. CABLING AND CONNECTIONS

A. Cable-plant layout

Single pigtailed fibres are routed from the front-end optohybrids to a first distributed patch-panel that is embedded within the structure of each sub-detector (Fig. 2). At this patch-panel, groups of 12 individual pigtails are connected to optical fan-outs by means of flat-polished MU-type connectors. The rugged ribbon of the fan-outs crosses the bulkhead of the sub-detector to reach an in-line patch-panel (PP1) where the connection to the Multi-Ribbon (MR) cables is made using angle-polished 12-fibre ribbon connectors. The MR cables (containing 96 fibres made up of 8 12-fibre ribbons) cover the span from the experimental cavern to the racks in the service cavern. Their overall length varies between 50 m and 70 m depending on the sub-detector and the assigned path. The path of cables for the barrel-detectors (pixels, Tracker, ECAL Barrel) is shown in Fig. 3. At the back-end the connection to the VME modules is implemented with angle-polished MPO-type connectors.

Pixel and ECAL End-Caps have a slightly different optical link topology with additional 12-fibre patch-cords inserted between the MR cables and the fan-outs in order to cover the additional length necessary to reach the edge of the sub-detector (Fig. 4). Thus the connection between the patch-cords and the fan-outs takes place at an additional intermediate patch-panel (PP0). For Tracker, Pixel and ECAL Barrel the intermediate connectors are angle-polished (MFS-type) with PP1 and PP0 located inside the solenoid vacuum tank in YB0. In particular the Tracker and Pixel share the same PP1 which results in a very high density of connections.

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B. YB0 cabling

672 pre-connectorized MR cables for Tracker (530), Pixel (34) and ECAL-Barrel (108) were installed in 2007 on the CMS central barrel wheel YB0 during a 6-week cabling campaign that took place just before the Tracker was inserted. The cabling of YE-1 and YE+1 for ECAL End-Caps (72 MR) and Pre-Shower (24 MR) was done after both end-caps had been lowered into the cavern, during the first quarter of 2008.

The YB0 cabling procedure for Tracker, Pixel and ECAL was extensively practiced during the past years [6]. The cables were individually labelled and pre-assigned to a specific path according to their length and the length of the particular route before transportation to P5. Thus the intended connections were already frozen in a cabling map and corresponding database at this stage. Custom mechanical protection elements were added on both ends of each MR cable to protect the naked ribbon portions during handling and installation.

The optical cable installation and test commenced with the first six ECAL Barrel sectors (3 MR cables/sector). The cabling and test crew was then sufficiently trained to start the large installation of Tracker optical cables in parallel with remaining ECAL barrel cables that shared the same cable trays. The Tracker cabling is split into 32 sectors, with 16 PP1s on each side of YB0. Each PP1 houses an optical patch panel with four aluminium cassettes with total dimensions of 60 x 9 x 15 cm$^3$ (l x w x h). Each PP1 houses up to 20 MR cables and associated slack ribbon (up to 50 cm). The cables with their MFS connector blocks are arranged as in Fig. 5.

Figure 3: The CMS central barrel (YB0) is fixed in the middle of the UXC55 cavern. The optical cables for Tracker, Pixel and ECAL Barrel take the shortest path to USC55 crossing the pillar in the two diagonal tunnels.

For ECAL End-Caps and Pre-shower the equivalent of PP1 is placed at the base of YE-1 and YE+1 while PP0 is integrated in the detector bulkhead. Both patch-panels incorporate MPO-type connectors with the patch-cords spanning a length of 18 to 42 m across the End-Cap wheels.

The entire optical cabling system [for both readout and control] of Tracker, Pixel and ECAL comprises 4928 fan-outs, 684 patch-cords and 768 MR trunk-cables. During the cabling at LHC Point 5 (P5) the inner segments of the optical links, including the 52304 pigtails, the distributed patch-panels and part of the fan-outs, were already sealed in the sub-detectors volume and no longer accessible$^2$ (see Fig. 4).

\[\text{Figure 4: Inaccessibility of distributed Patch Panels. PP0 and intermediate patch-cords exist only for Pixel and ECAL End-Caps.}\]
The cabling procedure is described next with the numbers of people involved shown for information in parentheses. To avoid kinks and twists in the cables, which were found previously to lead to losses in the transmitted signals, installation was made one cable at a time. Starting from one of the entrances to the tunnels on UXC55 side of the concrete pillar between the two caverns, the MFS terminated end was threaded along the cable trays (8 people) to the corresponding PP1 cassette where the cable was fixed in a strain relief. After a given cassette was filled (2 people), the MR cables were then bundled and fixed in the cable trays (2 people) at the same time as the next set of cables was being pulled in parallel elsewhere on YB0. Once a bundle was fixed along the entire length within UXC55, the cables were pulled one by one through the tunnel into USC55 (3 people) where they were individually routed (4 people) along the trays beneath the racks (in the 1.8 m tall false floor) to the final destination. The cable was then pulled up to the rack (2 people) and fixed to the corresponding crate. Finally the slack for a given cable was then wound onto a custom figure-8 support located below the rack.

At the peak of the cabling activity, the cabling and test team numbered 25 people and up to 35 cables could be laid per day (in a single 10-hour shift). All the procedural actions were tightly coordinated to fit together, the slowest action being the fixing of the cables in the trays, which required care to follow a precise path in order to fit up to ~200 optical cables into a given tray that often varied in cross-section as it followed the changing contours of YB0.

![Image: A fully occupied Tracker PP1 patch-panel cassette. The MFS ribbon connectors are positioned in the middle. Up to 50cm of slack per ribbon can stored on each cassette. Silicone spiral-wrap was added to organise and protect the bare fibre ribbons.](image)

**C. PP1 and PP0 connections**

ECAL Barrel cables were the first to be connected at PP1 right after the MR cable validation test (see Section III). ECAL Barrel PP1 is made of aluminium boxes mounted on the edge of the sub-detector elements (supermodules) in which the fan-out tails (which were very short, only 10 cm long\(^3\)) and MFS connector blocks are housed. The MR cables were pulled directly to the box and strain relieved. This allowed the rest of the cable length to be laid and fixed all the way to USC55 whilst leaving the connector block temporarily fixed at PP1. The validation test was then carried out (typically in the same day) after which the connection could be done and the patch-panel closed.

Tracker MR connections at PP1 had to wait for Tracker insertion, which took place in December 2007. The ribbon fan-outs, which were already connected to the Tracker distributed patch panels, had been pre-grouped, labelled according to their final PP1 destination and stored on mechanical support frames attached to Tracker bulkheads. The fan-outs were unbundled and carefully laid, sector by sector, PP1 cassette by cassette, in cable channels (3 m long x 30 mm wide x 100 mm deep per sector) going from the Tracker bulkhead up to the PP1 cassettes. Inside the cassettes the fan-outs were laid precisely in parallel layers and taped in place to make best use of the limited space in the channel. The naked portion of the fan-out ribbon at the PP1 end (80 cm long) was arranged in the cassette in the characteristic S-shape shown in Fig. 5, after the connection to the MR. During cabling of the Tracker sub-systems there were some mismatches in length (typically 10cm within a bundle of 4 neighbouring fan-outs) and this difference in length was absorbed in a small volume between the cable channel and the cassette which was reserved for this purpose.

The PP1 fibre connection procedure had been practiced in the previous months on a Tracker PP1/cable channel mock-up at CERN. The effort required to connect 40 fan-outs in a cassette was initially 4 hours (for the first 4 sectors) with a crew of 4 people. After this initial trial the procedure was streamlined, requiring typically only 2 hours and a crew of 2 people per cassette. The Tracker fibre connection activities had, however, to be fully integrated with the rest of the sequence of Tracker connections (including pipe-connections, barrel fibres, pipe insulation, barrel electrical cables, end-cap fibres, end-cap cables). In essence this was achieved by asking the crew to participate in all tasks besides piping which allowed the connections work to be evenly distributed in two daily 8-hour shifts spread out over many sectors in parallel (the maximum occupancy inside YB0 was 2x10 people per side) over a period of 2 months.

The Pixel detector patch-cords were installed and connected at PP1 after the Tracker fan-out installation. In this case the routing was from PP1 to the Tracker bulkhead where the pixel PP0 is located. After insertion of the beam-pipe and the Pixel sub-detector, the patch-cords were connected to the fan-outs at PP0 (August 2008).

The connections at the equivalent PP1 for the ECAL End-Caps and Preshower followed a similar procedure except that the patch-cords mounted on YE+1 and YE-1 were already installed before the CMS end-cap disks were lowered into the cavern. At the end of July 2008 the PP1 connections were completed. In parallel the sub-detector internal cabling was terminated and the various parts lowered. The connections at PP0 were done and tested immediately afterwards.

### III. QUALITY CONTROL

The Quality Control procedures followed in P5 were originally defined for the Tracker and extensively practiced.
during the previous 3 years [6]. A detailed description of the QC programme and the various test tools can be found in [7].

The test system is based around a high-resolution Optical Time Domain Reflectometer (OTDR) which can be combined with an optical switch or a custom-developed optical splitter for testing single fibres (switch) or full ribbons (splitter, 12 fibres at a time). The splitter option reduces the time of testing to one third with respect to testing a single fibre at a time (20 minutes/cable versus 1 hour/cable) and was thus used predominantly in P5.

The main goal of the test was to verify the mechanical integrity of the installed fibres and the good quality of the connections at the patch-panels. We were thus able to quickly give feedback to the cabling crews so that any problems observed could be corrected by planning an appropriate intervention and/or changing the cable-laying/connection procedures. A second objective was to measure the total length of the installed optical links with a precision better than 20 cm (necessary for the synchronization of the Tracker [8] and other sub-detectors). This requirement and the fact that only one end of the optical system was accessible for the measurements led to the choice of using a photon-counting OTDR during the tool selection process.

![Figure 6: Example of the QC scheme followed for the Tracker. Similar procedures were followed for the other systems.](image)

The scheme in Fig. 6 summarizes the Tracker QC procedure adopted in P5. The Pixel and ECAL groups adopted the same procedure. The test crew was typically composed of two experts and two technicians sharing two OTDR test systems (one provided by Tracker, one by ECAL) combined as necessary with either a switch or a splitter, plus two microscopes (600x magnification) for connector inspection. A variety of cleaning tools (5 different types for all kind of installed connectors/adapters), ribbon and single-fibre fault locators and two fusion splicers were also commonly used for troubleshooting interventions.

### A. Test activity

To be efficient in indentifying problems and planning adequate interventions the test activity had to closely follow the installation progress. The test started immediately after the first ECAL Barrel cables were pulled (test of the trunk-cables) using the OTDR combined with the switch to gain a detailed picture of fibre integrity along the cable path. After testing 20% of the cables without observing problems, both the testing and cabling crew were judged to be sufficiently well-trained. This also allowed the test to continue using the splitter configuration and thus speed up the testing by 60%. ECAL Barrel cables were entirely tested from the back-end (their installation in the rack patch-panels followed immediately after routing) and connected at the front-end sector by sector after each test. Afterwards the cables were re-tested again (test of the full-link) and the connectors re-cleaned/re-mated if necessary before final validation and connection at the back-end.

The Tracker and Pixel procedures were similar, with the difference that the connections at PP1 did not immediately follow the cable installation (the Tracker was not inserted yet) and the test of the trunk-cables had to be carried out from the front-end side (from inside YB0) due to the fact that the back-end cable protections were not removed until all cables were installed. After completing 30% of ECAL cabling, the Tracker/Pixel MR cables started to be laid and a second test crew started the test from PP1. The OTDR was equipped at the beginning with the switch (5% of the cables for validating the installation) and then with the splitter. Custom-built patch-cord adapters were used for the connection to the cable MFS blocks. Once the cabling installation was complete, preparation was made for Tracker insertion and the last 20% of cables were tested from the back-end.

After Tracker insertion and its connection at PP1 the testing was done entirely from the back-end with 2 OTDRs and 4 people working in parallel. Two more people focused on the troubleshooting at PP1 based upon feedback from the back-end crew.

For ECAL End-Caps and Pixel the OTDR testing was done in three steps: 100% of the MR cables; 100% of the patch-cords; then a fraction of full-links - those requiring troubleshooting for pixels after feedback from the DAQ system; and 60% of ECAL End-Cap links - only 60% were tested due to the limited time available.

### B. Test results

Table 1 summarizes the test results. For the MR cables (including the extension patch-cords) only 0.27% of the total ribbons were found to be broken and in all cases a repair (splice) or a replacement with an installed spare ribbon was possible. For the full-links it is worth distinguishing between damage along the fan-out tails and problems caused by dirty, scratched or badly mated connectors. In the first case only one Tracker fan-out was so close to the bulkhead that no repair was possible. Hence the corresponding 12 optical channels were lost (0.03% of the total). In the case of problematic connections at PP1/PP0, the re-cleaning/re-mating interventions were highly successful although 25% of the problems required from two to four troubleshooting
interventions. Each intervention lasted in average 2 hours and required gaining access to the related PP1/PP0, removing the fibre protection, extracting of the block of connectors from the cassette (in the Tracker case) and various re-cleaning/re-mating cycles followed by as many OTDR tests as necessary until the problem was fixed or judged unsolvable.

All cases in which the connection could not be fixed were flagged for further investigation by DAQ experts. All those MU connections suspected to contribute to a reduction of the corresponding link gain were also flagged.

**IV. PERFORMANCE VERIFICATION**

As natural extension of the Tracker QC program, the performance verification aims to verify the achievement of the specification targets for the analogue optical links when the system is operational. In the Tracker analogue readout links it is possible to measure different parameters including the laser threshold/bias and the overall link gain at the operating temperature. The initial QC phase started in July 2008 when the cabling functionality was checked by progressively powering up various parts of the detector (checkout). This required some troubleshooting, especially at the back-end where the connections could not be checked with the OTDR. The interventions on the back-end connections were based on a dry cleaning followed by a microscope inspection on both connector sides and additional cleaning cycles if the problem persisted. If necessary an OTDR test was repeated to exclude the presence of new damage that may have occurred along the cable path.

Table 2 summarizes the results of this activity. Those channels for which the connections were not cleaned successfully are flagged as still recoverable with a more aggressive cleaning action or by replacement of the receiver modules. The problems on those channels for which the connections were found to be clean and the OTDR did not reveal anomalies are thought to be due to other causes within the Tracker system. At the end of August 2008 the Tracker was more than 99% functional with only 0.1% of fibre-channels lost. The possibility of recovering a few low gain channels still remains. Fig. 7 shows the measured gain of the links after optimisation to bring the output gain as close to the target value of 0.8 V/V as possible. The noise of the links is under study, as is the laser threshold current. All these parameters are temperature-sensitive and will be tracked by making periodic scans of the optical link characteristics as the Tracker operating temperature is decreased in steps towards the intended operating temperature of -20°C.

**Figure 7: Measured Tracker analogue optical link gains with Tracker coolant circulating at 13°C. The target gain is 0.8 V/V. Front-end AOH gain setting (0, 1, 2 or 3) has been automatically selected to optimise the resulting output. Low gain values can be due to problems not related to the optical links. For more details on switchable gain function and expected distributions, see Ref [9].**

**V. DISCUSSION**

With hindsight and given the very good results of the fibre-optics installation, it is useful to consider whether it was
worth the effort and resources that were devoted to the thorough test and measurement campaign. Developing the custom OTDR test setup (hardware/software), practicing the procedure and training the crew (4 people plus 2 experts) required more than a year of specialized engineering work. In addition a year was then spent testing and troubleshooting.

Considering first the choice to use an OTDR for testing: we recall first of all that this choice was originally also motivated by the wish to measure the full-link lengths with high precision, as required as an input to the Tracker synchronization procedure [8]. This point proved less important than other factors: the first of which is that the optical links are accessible only from the back-end connection, once connected at (PP0 and) PP1 patch-panels. This means an OTDR is the ideal instrument as it works with reflected light signals. In addition, when a fibre is broken it is very important to know which cable section contains the break. For example, in a PP1 the MR cable is relatively easy to remove and repair (in 2 hours of access) but the fan-outs are much more fragile, being densely packed where a repair can require as much as 2 days of uninterrupted access to PP1.

Considering the argument that the small number of eventual problems did not warrant the large effort expended on testing, we note that the success of this activity largely originated from the fact that precise and punctual feedback was available from the test activity. This allowed efficient refinement and evolution of the details of the cabling and connections procedure. This capability provided the confidence to increase the installation rate as needed to minimize the time spent on the ‘critical path’ of CMS installation.

A standalone test-setup was chosen mainly in order to avoid needing to wait a long time for feedback on link performance based on the quality of data coming from Tracker operations. The Tracker, like other CMS systems could not operate and provide feedback until all parts of the system were available such as cooling, power, slow control, safety and DAQ. Due mainly to problems with the Tracker cooling, it was several months after cabling finished before performance data was available, by which time there was no longer access to the PP1s as CMS was closing ready for LHC operation. In addition, the problems found during Tracker operations might have a variety of causes, given the complexity of the system. Having a standalone system meant that all the problems in the fibre system were traced quickly and efficiently, with those originating inside YB0 volume being diagnosed and solved during the relatively brief access period.

VI. CONCLUSION

In 2008 a major milestone was reached with the completion of integration of the CMS experiment. The optical cabling and connections for Tracker, Pixel, ECAL and Preshower went smoothly and was carried out as an integral part of the wider services installation. In this context the detailed planning for fibre installation and test was combined with other neighbouring tasks allowing a smooth and predictable workflow over what proved to be a demanding task.

Rapid feedback on the quality of cabling and connections was provided using a test system based on a high resolution OTDR, which was also later used for further troubleshooting as well as providing the lengths needed for Tracker synchronization.

The quality of the cabling and connection work was excellent. The number of broken/stressed ribbons was well below 0.5% with only one broken ribbon proving to be unrepairable. Also, the troubleshooting capability for the problems discovered at connections in the patch-panels was very high (over 80% success) leaving the Tracker, for example, with only 0.1% of lost fibre channels.

Ultimately the quality of the cabling and connections, as well as the test and measurement programme was built on good preparation, training and an excellent team spirit during 15 months of optical cabling activity in CMS.

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Abstract

We present the proposed Data Acquisition (DAQ) system for KOTO, a $K_L \rightarrow \pi^0 \nu \nu$ experiment at J-Parc, Japan. It comprises two distinctive blocks: a $14(12)$-bit, $125\,(500)$ MHz ADC module for reading the approximately 4000 front-end channels; and a digital Trigger module able to provide a detector-wise synchronous energy sum. A Master Clock and Trigger Supervisor Module, with fans out of control signals to the whole system, completes the DAQ Architecture. The front-end readout board amplifies analog pulses from 16 photomultipliers and passes them through a 10-pole shaper before digitization. Data are then processed locally with field programmable gate arrays (FPGAs) to determine real-time energy values for the system Trigger Supervisor. The ADC module is provided with a pipeline, up to 4us long, which stores the acquisitions, awaiting the system trigger pulse. After a trigger, data are packed and buffered on on-board memories for readout via the VME32/64 backplane. The full design and preliminary test results will be described.

I. SYSTEM ARCHITECTURE

We present the Data Acquisition (DAQ) System for the Step-1 phase of the KOTO experiment [1], a high energy physics kaon experiment at the Japan Particle Accelerator Research Complex (J-PARC). The goal of the experiment is to measure the rate of the rare decay $K_L \rightarrow \pi^0 \nu \nu$. This flavour changing neutral current decay is predicted by the Standard Model (SM) to happen only once every $3.3 \times 10^{11}$ $K_L$ decays. If not observed or observed at a rate very different from the SM predictions, it will shed light on the mechanism responsible for CP in the quark sector.

The DAQ Architecture comprises three functional blocks: front-end modules for the readout and digitization of the ~4000 channels in the KOTO detector; digital trigger modules with a dead timeless two-level design; and control plus fan-out electronics for the orchestration of the entire DAQ and final events readout. Figure 1 contains a block diagram of the DAQ Architecture for the KOTO detector.

The front-end electronics is spread over seventeen (17) 6U VME Crates, and includes three distinctive board flavours:
- Caesium Iodide (CsI) boards, using 14-Bit, 125 MHz ADC modules, each reading out 16 of ~3000 crystals in the KOTO CsI calorimeter.
- Veto Detector boards, using the same custom 14-Bit, 125MHz ADC Modules, fitted with a different firmware, for the readout of ~700 channels.
- Beam Hole Veto boards, using custom 12-Bit, 500MHz ADC Modules, with 4 channels per module, for the readout of up to 100 channels.

The Trigger electronics is designed to provide a dead timeless first level (L1) decision based on the total calorimeter energy and a second level (L2) trigger decision based on clustering and absence of signals in the veto detectors. Events passing the L2 trigger are stored in on-board memories for readout during accelerator spills.

The Trigger modules are housed in 9U VME crates with customized P3 backplane. The Trigger decision is made by the MAster Clock and TRigger Supervisor (MACTRIS) board, which generates and fans out control signals to the whole system, oversees the event readout and communicates with the Event Builder (EVB) and the accelerator.

II. TRIGGER DESIGN

The ADC boards receive the analog outputs of photomultipliers (PMT) attached to the frontend detectors. The analog pulses are shaped by 10-pole Gaussian low pass filters generating fixed-width Gaussian shaped pulses with a FWHM of about 45. By performing a fit to the output shape with a fixed width Gaussian one obtains two key parameters: the height of the Gaussian, which measures the total charge (energy) of the pulse, and the position of the peak, which measures its timing. Figure 2 shows the Gaussian output pulse shape for a sampling rate of 125 MHz.

The shaped pulses are saved inside a 4 us long pipeline where they await for the L1 trigger decision. From the DAQ point of view, an event (i.e. the energy deposited by a single photon in the calorimeter) becomes a set of N consecutive samples centered around the L1 trigger. This is a variable
width signal enveloping the samples with total energy above a predetermined programmable threshold, as illustrated in Figure 2.

![Figure 2: Shaped PMT pulse (black) and DAQ event (light blue) as a set of N consecutive samples around the L1 Trigger (red pulse).](image)

The MACTRIS board aligns the L1 trigger decision with the PMT data as they exit the L1 pipeline and saves the events inside multiple L2 buffers, where each event can be fit to a gaussian template for a precise energy and timing measurement. The L2 trigger decision is done asynchronously with the sampling clock but sequentially over each L2 buffer. The L2 trigger is based on clustering of adjacent CsI crystals to count photons in the calorimeter and on rejecting events with in-time activity in the veto counters.

![Figure 3: Cartoon view of the two-level Trigger for KOTO.](image)

The two-level trigger allows a further reduction of readout rate to a manageable level. Events passing the L2 trigger are sent to an on-board VME Memory for readout via VME backplane. Figure 3 shows a cartoon of the two-level trigger design for KOTO.

### III. FRONT-END MODULES

There are two different custom ADC Modules used in this experiment:

- 16-Channel, 14-BIT, 125MHz ADC Boards - for the CsI DAQ, and for the Veto Detector (with different firmware);
- 4-Channel, 12-BIT, 500MHz FADC Boards – for the Beam Hole Veto.

The ADC Boards are distributed over 17 VME Crates (6U). Each board connects directly to the Trigger Electronics via two Optical Links and one CAT5 cable.

Figure 4 presents the block diagram of one 14BIT, 125MHz 16-Channel ADC Board. The Boards are located 16 per one 6U VME Crate, and receive analog pulses directly from the PMTs. The Trigger Electronics connections are as follows:

- The CAT5 connection is used for the System Clock, and Trigger/Control Pulses.
- The Board Total Energy, is sent to the Trigger Modules via a 2.5Gbps Optical Link.
- The 2nd 2.5Gbps Optical Link is used for data readout upon a L1 Trigger pulse.

![Figure 4: Block diagram of the 14-BIT, 125 MHz ADC Module.](image)

In the CsI Calorimeter, every analog pulse generated by the photomultiplier tube is amplified and passed through a 10-pole filter/shaper with a cut-off frequency of about 10 MHz, which converts the fast PMT pulse into a Gaussian form, while keeping the total energy information constant. The filter/shaper was calculated for optimal Full Width Half-Height (FWHH) of the resulting pulse with respect to fitting and timing. Scope plots of the input and output signals are presented in Figure 5.

![Figure 5: Scope plots of input and output signals through the shaper used in the KOTO CsI DAQ.](image)

After shaping, each pulse is applied to a sample-and-hold ADC chip (AD9254).
Digitized data are processed locally with Field Programmable Gate Arrays (FPGAs), Altera EP2S60F1020C5 chips from the STRATIX II family [2] that perform the board total energy calculation and determine real-time board energy related values. These values are passed via 2.5Gbps Optical Links directly to the Trigger Electronics, for final decision, and eventual trigger pulse generation.

Each ADC module is provided with a pipeline, up to 4us (500 samples) long, which stores the acquisitions while awaiting the system trigger pulse. After a trigger, data are packed and buffered for readout. Data readout is performed via the 2nd front panel Optical Link.

A prototype 16-Channel, 14BIT, 125MHz ADC Board was built, and is presented in Figure 6. Preliminary tests showed an SNR of about 74dB.

The 4-Channel, 12-Bit, 500MHz Module, used in the Beam Hole Veto, has the block diagram presented in Figure 7. The functionality is similar to that of the 16-Channel CsI ADC Module. The FADC chips send LVDS signals to the FPGA, where a customized deserializer block reduces the bus frequency by a factor of four. Overall this 500MHz Module will process, and transmit the same volume of data as the 125MHZ Board used for the CsI.

IV. CONCLUSIONS

We presented the design of the DAQ for the K0TO detector at JPARC. The proposed architecture has three distinct functional blocks, one for the frontend readout, one for the trigger and one for DAQ controls.

The frontend electronics combines energy and time measurement in a single digitization step thanks to a new technique of waveform shaping. Its design is quite advanced and has already been tested in a 16 channel testbeam.

The digital trigger is designed to provide a deatimeless first level decision based on the total deposited energy and an asynchronous second level decision based on energy clustering and in-time veto signal rejection.

A commissioning run is scheduled for end of 2009, with Phase-1 data taking starting in winter 2010. The modularity in the K0TO DAQ design should provide enough flexibility to be able to cope with the increase in event rates expected for Phase-2 of the experiment.

V. REFERENCES

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Noise Analysis of Radiation Detector Charge Sensitive Amplifier Architectures

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Abstract

In this work, a detailed comparison of four equivalent charge-sensitive, folded-cascode amplifiers in terms of noise performance is presented. A couple of complementary structures, one with a noise-optimised input nMOSFET and the other with a noise-optimised input pMOSFET were designed in 0.35 μm CMOS process by Austria MicroSystems (AMS). Another couple of complementary structures consisting of a noise-optimised input npn with a pMOSFET cascode, and the respective structure having a pMOS as input device, were developed in a 0.35 μm SiGe BiCMOS process (AMS). The structures’ comparison is performed through simulation, after careful selection of the parameters that remain constant in all four variations.

I. INTRODUCTION

High Energy Physics Experiments (HEPE) have given a great boost to the analogue VLSI for front-end devices applied to Solid State Detectors, the main reason being the large number of channels required for such experiments. The charge generated by the X-rays – Sensors interaction is very small and has to be amplified in a low noise circuit before any further signal processing. The growing number of channels, more in multi-detector systems, sets different problems. Regarding the power dissipation-noise limitations, it is better to put the detector and the front-end amplifier as close as possible. However the heat transferred from the amplifier to the detector can create problems of drift and make its resolution worse. Concerning the active occupied area the segmentation of the multi-detector systems is mainly limited by the preamplifier size and finally regarding the total cost, the price of a preamplifier depends on the technology involved. A VLSI preamplifier costs much less than a hybrid one or a preamplifier unit.

While literature is available on the noise behaviour of the front end stages [1]-[2], contrary few studies have been performed regarding the used process configuring the radiation detection ASIC and the related trade offs. The main problem in the design of nuclear spectroscopy VLSI readout front ends is the implementation of low noise – low power Charge Sensitive Amplifier (CSA) – Shaper systems (figure 1) and the selection of the process (CMOS or BiCMOS) determines the total performance and generally the noise related design methodology. Non extended research has been performed comparing the use of a MOSFET or a bipolar device as the input device of the pre-amplification cell in terms of the total noise contribution setting strict comparison constraints.

II. PREAMPLIFICATION STAGE ANALYSIS – NOISE OPTIMIZATION METHODOLOGIES

A detector readout system’s noise performance is expressed as the equivalent noise charge (enc) (ratio of the total rms noise at the output of the pulse shaper to the signal amplitude due to one electron charge). The noise contribution of the amplification stage is the dominant source that determines the overall system noise and is therefore, optimized. The main pre-amplification stage noise contributor is the CSA input device. The noise optimisation methodologies regarding CMOS and BiCMOS CSA implementations are provided below.

A.CMOS Implementations

The main noise contributor is the CSA input MOSFET and the noise types associated with this device are 1/f and channel thermal noise. The respective en<sub>c</sub> are given by [1]-[5]:

\[
enc_{\text{in}} = \frac{1}{g_m} \left( \frac{n^2 \sigma_{\text{n}}}{n^2} \right) B(\frac{1}{2}, n - \frac{1}{2}) \sqrt{\pi} \tau \quad C_i^2 \quad (1)
\]

\[
enc_{1/f} = \frac{K_f}{C_{\text{in}}WL} \left( \frac{n^2 \sigma_{\text{n}}}{n^2} \right) \frac{1}{q^2} \frac{1}{2n} \quad C_i^2 \quad (2)
\]
where $B$ is the euler beta function, $q$ is the electronic charge, $\tau_e$ is the peaking time of the shaper and $n$ is the order of the semi Gaussian shaper. Capacitances $C_{d}$, $C_{p}$, $C_{GS}$ and $C_{GD}$ are capacitances of detector, feedback, gate-source and gate-drain of the input MOSFET respectively, and $C_{p}$ is the parasitic capacitance of the interconnection between the detector and the amplifier input, which is generally considered negligible. $k$ is the Boltzmann constant, $T$ is the temperature, $g_{m}$ is the transconductance, $K_{f}$ is the flicker noise constant depended on device characteristics and able to vary widely for different devices in the same process, variables $W$, $L$ and $C_{ox}$ represent the transistor’s width, length and gate capacitance per unit area respectively.

The total input stage capacitance is given by [1]-[5]:

$$C_{i} = C_{\text{total, in}} = C_{d} + C_{p} + C_{f} + C_{GS} + C_{GD} \quad (3)$$

Optimum gatewidths exist for which the respective thermal and flicker $enc$s are minimal. These optimum dimensions are extracted by minimizing the respective $enc$s.

$$\frac{\partial enc_{th}}{\partial W} = 0 \Rightarrow W_{th} = \frac{C_{d} + C_{f}}{2C_{th} \alpha L} \quad (4)$$

$$\frac{\partial enc_{f}}{\partial W} = 0 \Rightarrow W_{f} = 3W_{th} \quad (5)$$

where $\alpha$ is defined as $\alpha = 1 + \frac{9X_{j}}{4L}$ and $X_{j}$ is the metallurgical junction depth. Equations (4) and (5) are valid when capacitance $C_{d}$ is in the range of picofarad. When the dominant noise component is determined, the CSA input transistor type and its optimum dimensions are selected, considering that typically P-MOSFETs have less $1/f$ noise than their n-channel counterparts

**B. SiGe BiCMOS Implementations**

Normally, the Equivalent Noise Charge for a bipolar transistor as an input device is determined by the parallel noise and series noise contributions. For an optimized preamplifier design, these two contributions, mainly characterized by the base and collector current shot noise and the base spreading resistance $R_{sh}$, are given by an equivalent input noise voltage source and a current source with noise spectral densities [6]:

$$S_{N_{in}} = 4kT(R_{sh} + \frac{1}{2g_{m}}) \quad (6)$$

$$S_{I_{in}} = 2qI_{b} \quad (7)$$

The series noise voltage is built up from two components, the base spreading resistance $R_{sh}$ and the transconductance of the input transistor. In order to minimize the spreading resistance which is scaled inversely by the emitter area, a large emitter area should be chosen. As mentioned above, the main radiation effect observed in bipolar transistors is the degradation of the current gain $\beta$. This effect is inversely proportional to the current density in the base area and from this point of view a small emitter device is preferable. In order to keep the lowest base spreading resistance, multiple base contacts should have been used and the width of the emitter region is set to minimum that gives a minimal distance between the base contacts and the emitter. From Equations an important fact can be found that there is an optimum collector current $I_{c}$ where the total noise contribution is minimum. With a CR-RC type of shaper, the approximate expression for $enc$ referred to the input is given below:

$$enc = \sqrt{\frac{3.67(\frac{kT}{q})^{2} \left(\frac{R_{sh} + \frac{kT}{2qI_{c}}}{qI_{c}}\right) + 1.83\frac{\tau_{e}I_{c}}{q\beta}}{(1)}} \quad (8)$$

where $\tau_{e}$ is the shaping time and $C_{th} = C_{d} + C_{f} + C_{GS} + C_{GD}$, $C_{f}$, the detector capacitance, $C_{th}$ the feedback capacitor and $C_{sh}$ the input capacitance of the input bipolar transistor of the CSA. It can be observed that noise performance of an electronic front-end depends on the shaping time of the preamplifier-shaper and the capacitor $C_{th}$. For a given shaping time, the detector capacitance and current gain, an optimum collector current which gives minimum noise can be obtained:

$$I_{opt} = \sqrt{\beta} \frac{C_{th}V_{th}}{\tau_{e}} \quad (9)$$

where $V_{th} = \frac{kT}{q} \quad (10)$

In contrast to the CMOS case where optimum noise performance is achieved by choosing the dimension of the input transistor for a given detector capacitance, in bipolar devices, the optimum noise matching can be achieved by adjusting the collector current of the input transistor for any detector capacitance.

**III. Folded Cascode Amplifier Topologies**

**Design - Comparison**

Four equivalent folded cascode amplifying topologies were designed. Our primary concern was the examination of noise contribution of the devices pair, firstly the input transistor and secondary, the cascoded one. The four structures were: a) nMOS as the input and pMOS as cascode, b) pMOS as input, nMOS as cascode, c) npn BJT as input, pMOS as cascode and d) pMOS as input and nMOS as cascode. To further isolate these noise contributors, ideal bias current sources and output buffer were used, in all four designs. Feedback was implemented using a capacitance in parallel with a large reset resistor. The structures were designed in two respective processes commercially available by Austria Mikro Systeme (AMS), the 0.35µm CMOS process (2P/3M 3.3/5V) and the 0.35µm SiGe BiCMOS process (2P/3M 3.3/5V). All four folded cascode topologies are depicted in figure 2.

In order to achieve a fair comparison, the bias current of the input branch was selected by applying noise-optimisation theory on the input npn available transistor (equation 9). This bias was then kept constant for the rest implementations, where noise-optimization methodology was applied regarding the input MOS type to set its dimensions. This bias current selection, in addition to constant total power (current) consumption, leads to a constrained bias current for the cascode. This, in the case of the BJT cascode, results to a
specific transconductance value, constraining the cascode MOS dimensions in the rest cascode structures.

A table containing the comparison specifications – design characteristics is depicted below (table 1). In all these configurations the noise contributors are the input device, the cascode one and the feedback resistor.

<table>
<thead>
<tr>
<th>Application Specifications</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Detector Capacitance</td>
<td>2 – 20 pF</td>
</tr>
<tr>
<td>Temperature</td>
<td>27°C</td>
</tr>
<tr>
<td>Peaking time</td>
<td>100 ns</td>
</tr>
</tbody>
</table>

| Comparison Specifications – Design characteristics |
|---------------------------|--|
| Ibias 1                   | 15 μA |
| Ibias 2                   | 7.6 μA |
| Vdd = - Vss               | 1.65 V |

The optimum collector current was found equal to 7.4 μA. Regarding the optimum dimensions of the input MOS device, in the case of an NMOS the dimensions were equal to (W/L) = (476μm/0.35μm) and in the case of a PMOS device (W/L) = (1428μm/0.35μm). The AC response of the four configurations is depicted in figure 3. All the topologies provide an operating bandwidth of 107 kHz and an output gain of 130 dB. Regarding the total power dissipation, in all the topologies 36.95 μW are consumed. The cascode parasitic transconductance is also equal for all four structures.

Regarding the output noise performance, the output noise spectral density is given in figure 4. As it is obvious the higher noise performance is observed in the SiGe BiCMOS while the lower is observed in the architectures with the
PMOS input device. The respective rms noise values at the CSA topologies output is depicted below. An overall table regarding the output noise dependence in the detector capacitance value is also provided (table 2). While the implementation with the BJT input device appears to provide the higher output noise, it also provided the lower slope regarding the increment of the rms noise in relation to the detector capacitance indicating as suitable for large detector capacitance applications, as shown in fig. 5.

<table>
<thead>
<tr>
<th>Table 2 : RMS Output Noise Vs Detector Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Noise Vs Detector Capacitance</td>
</tr>
<tr>
<td>NMOS input – PMOS cascode</td>
</tr>
<tr>
<td>PMOS input – NMOS cascode</td>
</tr>
<tr>
<td>PMOS input – BJT cascode</td>
</tr>
<tr>
<td>BJT input – PMOS cascode</td>
</tr>
</tbody>
</table>

![Figure 5: Output Noise vs detector capacitance](image)

**IV. CONCLUSION AND DISCUSSION**

In this work a comparison of four folded cascode preamplifier topologies is presented, in order to find out the preferred topology in terms of noise performance, respecting to the technology and design specifications. PMOS input-NMOS cascode, NMOS input-Pmos cascode, PMOS input-npn BJT cascode and npn BJT input-PMOS cascode and CMOS 0.35μm and SiGe BiCMOS 0.35μm were used. In all the topologies consumption was kept constant while the only noisy devices were the input transistor, the cascode transistor and the feedback element. Also the capacitance seen by the input transistor was also calculated to be equal in all the implementations. Simulation results demonstrate the superiority of the PMOS transistor as input device for small or medium size of detector capacitance , while the BJT transistor could be a good candidate in case of large detector capacitance.

Regarding the future work, extra analysis should be performed regarding the noise contribution of the feedback elements and the optimum selection in terms of the related design specifications.

References


The CMS Detector Power System

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Abstract

The power system for the on-detector electronics of the CMS Experiment comprises approximately 12000 low voltage channels, with a total power requirement of 1.1 MVA.

The radiation environment inside the CMS experimental cavern combined with an ambient magnetic field (reaching up to 1.3 kGauss at the detector periphery) severely limit the available choices of low voltage supplies, effectively ruling out the use of commercial off-the-shelf DC power supplies.

Typical current requirements at the CMS detector front end range from 1A-30A per channel at voltages ranging between 1.25V and 8V. This requires in turn that the final stage of the low voltage power supply be located on the detector periphery.

Power to the CMS front-end electronics is stabilized by a 2 MVA uninterruptible power supply (UPS) located in a CMS surface building. This UPS isolates the CMS detector from disturbances on the local power grid and provides for 2 minutes of autonomy following a power failure, allowing for an orderly shutdown of detector electronics and controls.

This paper describes the design of the CMS Detector Power System, reviews the process of its installation and commissioning, and discusses issues of power distribution common to current-generation collider detectors.

I. OVERVIEW OF THE CMS DETECTOR

CMS is a general-purpose detector at the LHC accelerator at the CERN laboratory in Geneva, Switzerland. A description of this detector is beyond the scope of this paper, but may be found in reference [1].

A. Requirements of CMS Detector

The front-end electronics of the CMS detector has 12090 low-voltage channels, requiring 1182 KVA of power. The steel yoke structure of the CMS detector serves as a flux return for the 4-Tesla solenoid inside the detector structure. Since the magnetic field of the solenoid is large enough to drive sections of this steel yoke into saturation there is an ambient magnetic field that can reach up to 1.3 KG outside detector in the regions where low voltage power supplies are mounted. Typical commercial low-voltage power supplies are not designed for operation in a magnetic field and many have been noted to fail destructively at fields above 150 Gauss. In addition, the high radiation environment inside the CMS experimental cavern imposes constraints on the design of low voltage supplies from the standpoint of semiconductor displacement damage and single-event effects. Together, these constraints rule out the use of general-purpose commercial power supplies.

Typical front-end current requirements are 1 to 30A per channel, at voltages from 1.25 to 8.0V. Since cable power dissipation must be kept within reasonable limits, the placement of the final power supply stage is constrained to be within ~10m of the front-end electronics, that is, on the detector periphery.

B. CMS power distribution requirements

The power cable paths between CMS on-detector systems and the power distribution area in the adjacent equipment cavern are typically 100 to 140m in length. Power to the detector is supplied at 380 and 230 VAC (three-phase) and at 385 VDC. No neutral is distributed.

The CMS detector power system serves all of the low voltage power needs on the detector from a single distribution network. Although there are other power distribution networks at the CMS site, there are no persistent connections between the CMS detector and any of these other networks. This single-source powering scheme enables a unified earthing structure for the CMS detector and simplifies considerations of detector response to disturbances in power distribution.

C. CMS power distribution system architecture

The detector power system is powered by a 2 MVA uninterruptible power supply (UPS) installed on the surface. The UPS provides for at least 2 minutes autonomy in the event of a power failure. This length of time is sufficient to provide for an orderly shutdown of subdetector power systems.

The UPS powers a bank of 6 isolation transformers located underground in one of the CMS caverns. The transformers are apportioned by subdetector and geographical detector region. Each transformer feeds one or more power distribution cabinets containing circuit breakers, monitoring equipment and programmable logic controllers. Power from an individual circuit breaker channel can be turned on and off via a remote control system, but in the event of a fault condition the circuit breaker must be reset manually. This is a deliberate design choice to prevent casual responses to fault conditions.

The isolation transformers consist of four 230V and two 380V three-phase units, each containing an interwinding electrostatic screen. Static compensators are connected to selected distribution cabinets in order to provide power factor correction (PFC) for certain subdetectors (Fig 1.)
D. CMS power supply architectures

Power from the distribution cabinets is in turn fed to power supplies located in the two CMS underground areas. CMS uses power supplies from two manufacturers. One is the Wiener MARATON series from Plein & Baus GmbH [3]. The second is EASY (3000 & 4000) Series from CAEN S.p.A. [2]. Each company has its own approach to meeting the radiation and magnetic-field tolerance requirements of CMS.

Each system spans two zones, referred to as the Safe and Hostile Areas. The magnetic field and radiation environment of the safe area is assumed to be compatible with conventional commercial electronics. The hostile area, on the other hand, is a special environment requiring electronics with enhanced radiation and magnetic-field tolerance.

The first stage of the Wiener power supply system consists of a bank of rectifier/power factor correction units located in the safe area which are powered via single-phase 230V inputs and which in turn supply 385VDC to MARATON supplies located in the hostile area, on the detector periphery. The input power is supplied by a phase-to-phase connection from one of three 230V three-phase isolation transformers shown in Figure 1. Since the rectifier units contain their own internal power factor correction circuitry, no additional static compensators are required at the level of the power distribution cabinets.

The MARATON supplies located in the hostile area contain up to 12 programmable output channels capable of supplying output voltages between 2 and 8V with a total unit power of 3.6 KW.

Control and monitoring of the MARATON supplies is accomplished via a CANBus readout chain that runs serially between some number of MARATONs on the detector. The CANBus readout chain is fed by a CANBus interface board mounted in a PC in the safe area. This PC is connected to the local network, through which the PC is connected to the CMS Detector Control System (DCS). The detector control system spans all subdetector systems on CMS. An overview of the Wiener power supply architecture is shown in Figure 2.

For the CAEN-based systems, on the other hand, three-phase power is fed directly to the hostile area, where it powers AC-DC converters which in turn supply 48VDC to modular crates containing DC-DC converter units that provide 1.25-8V to the CMS front-end electronics.

Control and monitoring of both the AC-DC converters and the DC-DC converter crates is accomplished via a serial readout chain using a proprietary protocol. Each chain controls up to 6 DC-DC crates and 6 AC-DC converters. The readout chains are driven from branch driver modules (CAEN A1676) located in readout crates (CAEN SY1527) located in the safe area. Each crate is connected to the local network, from which it is controlled by the CMS detector control system.

Each AC-DC converter and DC-DC converter module contains a communication board that interfaces with the control readout chain. This board requires 48VDC, which is supplied via a separate channel referred to as service power. Service power for the AC-DC converters is supplied via a dedicated channel in the branch controllers in the safe area, as illustrated in figure 2.

Only the AC-DC converters receive service power from the safe area, a consequence of limitations on the power available from the branch drivers. Service power to the DC-DC converters is derived from the outputs of the AC-DC converters once they are powered. This results in a two-step turn-on sequence. The power requirements of the DC-DC converter boards are significant (53KW vs. 9KW for the AC-DC converters alone,) making the supply of global service power from the safe area impractical as a result of cable voltage drop considerations.

II. OVERVIEW OF PHYSICAL INSTALLATION

The CMS detector is located in one of two adjacent underground caverns. The experimental cavern contains the detector itself, along with support infrastructure such as cooling equipment. Access to the experimental cavern is only possible when the LHC beam is not present. The detector is segmented longitudinally into 13 sections. The central section is fixed to the cavern floor. The other sections are movable in order to allow access to detector elements, and are capable of up to 10m of free travel in the direction of the beam axis.
All connections to the movable detector elements (such as cabling and cooling pipes) must be capable of accommodating this movement without the need for disconnection. All such connections are routed through flexible articulated cable chains laid in trenches under the detector.

A. Underground layout

The second cavern contains electronics racks for readout and triggering of the detector, the first layer of computing for the data acquisition system and infrastructure for providing services such as cooling and power. This cavern is referred to as the service cavern and is the “safe zone” mentioned earlier. Access to the service cavern is possible during the operation of the LHC. The two caverns are shown in figure 3.

B. Power distribution area

The power distribution area in the service cavern contains 6 isolation transformers, 6 power distribution cabinets containing circuit breakers and programmable logic controllers, 10 electronics racks and a bank of static compensators. The racks contain banks of rectifier/power factor corrector units for the Wiener MARATON power supplies, control crates for the CAEN power supplies and additional power supplies for heating tape associated with the cooling system of the CMS tracker detector. The layout of the power distribution area is shown in figure 4.

C. Power cabling

Typical cable paths between the power distribution area and the CMS detector range between 100 and 140m. There are three types of cables: primary power, service power and control cables.

The primary and service power cables are screened 7x6mm² cables. These can be organized as two tripsets for three-phase operation or as three pairs for 385VDC or service power. The 6mm cross-section was chosen to minimize the resistive voltage drop. The control cables are screened 25 twisted-pair cables for the CAEN power supplies or dual twisted pair for the CANBus cables used by the Weiner systems.

D. Patch panels

The CMS detector was assembled on the surface and lowered into the experimental cavern in sections. This strategy allowed for the assembly of the detector in parallel with excavation of the caverns and installation of service infrastructure. One consequence of such a design is the need for an interface connection for cabling and services in order to connect preinstalled infrastructure cabling to preinstalled on-detector cabling once the detector sections are lowered into the experimental cavern.

For the detector power system, this interface connection consists of a metallic enclosure mounted at the base of the equipment towers on each side of a detector section. These enclosures, or patch panels, are straight-through devices, but have provisions for splitting out service power and DCS connections. The patch panels also provide a low-inductance ground connection point for cable shields.

E. On-detector power distribution

The shields of the 7x6mm² cable segments are grounded at the end closest to detector, that is, for the segments between the patch panels and the power distribution area in the service cavern, the shields are grounded at the patch panel. The option for grounding the other end of shield at a later date may be exercised depending on operational experience with the CMS detector.

At the on-detector racks, the power cables must be broken out to the power supplies, in a way that is uniform for all the subdetectors. This is done using metallic rack-mounted distribution boxes, 2U high, which can accept up to two power cables, each of which can be broken out up to three ways. These distribution boxes can be mounted at the front or rear of the rack and may be located inside or outside the rack volume. The output connectors are keyed according to output power type to prevent application of the wrong voltage. The distribution chassis also serves as a low-inductance tie point for the cable shields. At this point, connections are made to the CAEN AC-DC converters and to the MARATON supplies.

III. POWER UTILIZATION IN CMS

The CMS power utilization has been calculated taking into account known efficiencies and cabling power losses.
A. Power utilization by subdetector

Broken down by subdetector, as shown in figure 5, the CMS electromagnetic calorimeter (ECAL) has the largest power requirements (38%) followed by the tracker detector (21%). It is interesting to note that the on-detector turbines are a significant part of CMS power requirements (11%). The power figures shown here represent the total power drawn at the level of the UPS by a given subdetector, and so include all power supply inefficiencies and cabling losses, as well as the front-end power required by the subdetector.

<table>
<thead>
<tr>
<th>System</th>
<th>Power Req. (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECAL</td>
<td>38</td>
</tr>
<tr>
<td>Tracker</td>
<td>21</td>
</tr>
<tr>
<td>Calorimeter</td>
<td>11</td>
</tr>
<tr>
<td>Pixel</td>
<td>10</td>
</tr>
<tr>
<td>Endcap RPC</td>
<td>5</td>
</tr>
<tr>
<td>Endcap Muon</td>
<td>3</td>
</tr>
<tr>
<td>Turbines</td>
<td>2.5</td>
</tr>
</tbody>
</table>

Figure 5: Power by CMS subdetector

B. Power utilization by distribution stage

An examination of the losses incurred at different stages of the power distribution system is shown in figure 6. It is immediately obvious that the global efficiency of the distribution system is very low. The power used by the front-end electronics is only 34% of the total power. The rest is lost to heat, either as power supply inefficiency or dissipation in the cables. These losses represent a significant load on the detector cooling system.

The losses are split roughly evenly between power supply inefficiencies and cabling losses. The bulk of the cabling losses (15% of total dissipation) occur in the last 10m to the front-end electronics.

The low efficiency for power distribution is common to all detectors of this type and is caused by the combination of large detector size, low front-end voltages and hostile operating environment.

IV. SUMMARY

The particularities of current collider detectors place special demands on their low voltage power distribution systems. Front-end voltage requirements are low (1-5V), requiring the final stage power supplies to be located close to (~10m) the front-end electronics. As a result, these power supplies must operate in a hostile area.

The commercial market for suitable power supplies is sparse. Even commercial power supplies developed for HEP sometimes need to be adapted to a particular experiment, resulting in a dependence on a single source.

EMI/EMC issues need to be addressed in the design of the distribution system. In many ways this is a question of mechanical engineering as much as electrical design. Long cable runs require attention to shielding and the means of grounding the shields. The meaning of detector “ground” for a metallic object 15m in diameter and 30m in length is not obvious.

The efficiency of current detector power distribution systems is low. Power losses are dominated by cable dissipation and power supply inefficiencies. These issues will need to be addressed in the designs for the next generation of detectors.

V. REFERENCES

[2] CAEN (Costruzione Apparecchiature Elettroniche Nucleari,) 11 Via Vetraia, 55049, Viareggio, Italy
[3] WIENER, Plein & Baus GmbH, Mullersbaum 20, D-51399 Burscheid, Germany
A Radiation Hard Current Reference Circuit in a Standard 0.13µm CMOS Technology.

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Abstract.

A CMOS bandgap current reference circuit has been developed in a 0.13 um CMOS technology. The circuit exhibits low sensitivity to temperature- and power supply variations. The combination of the natural properties of thin gate oxide MOS transistors with a gate-all-around layout approach makes stable operation in harsh radiation environment possible. In the present design we utilize only MOS structures and poly-silicon resistors. The output current varies in the range 0.9 % when the circuit is being irradiated up to a 200 Mrad.

I. Introduction.

Integrated circuits generating reference currents with low sensitivity to temperature variation and power supply variations are commonly used in analog blocks such as current comparators, A/D and D/A converters, and bias circuits. In high-energy physics experiments there is an additional requirement; that is to deliver a stable current during operation in ionizing radiation environments.

With ongoing CMOS evolution, the gate-oxide thickness steadily decreases, resulting in an increased radiation tolerance of MOS transistors. This, in combination with special layout techniques, yields to circuits with a high inherent robustness against X-rays and other ionizing radiation. In bandgap current references, the dominant radiation susceptibility is, then, no longer associated with the MOS transistors, but is dominated by the diodes.

For this reason in the present design we excluded diodes and used alternative structures called dynamic-threshold MOS transistors (DTMOST) instead. The DTMOST is made of a standard p-channel MOST by means of tying the gate terminal to the drain and bulk terminals. The source terminal is left open. This two-terminal device demonstrates an exponential (diode-like) current-to-voltage characteristic when the voltage is lower than 250mV. This feature enables us to consider the DTMOST as a “low-voltage diode” and to use it instead of an ordinary diode in standard bandgap circuits (see Figure1) [1].

II. Characterisation of the Dynamic-Threshold MOS Transistor (DTMOST).

In 1999 Anne-Johan Annema proposed to use DTMOST structure in CMOS technologies [2]. It is in fact a p-channel MOS (PMOST) transistor with gate, drain and substrate contacts connected together. In a limited region this device behaves similar to a conventional diode with exception: it needs far lower bias voltage to operate (see Fig.2).

The exponential behaviour of the voltage-to-current characteristic is of primary importance because it enables us to construct a current source, which delivers a current that is proportional to the absolute temperature (PTAT). This can be used to implement a mechanism of temperature compensation in a bandgap reference circuit. A conventional diode has an exponential voltage-to-current relationship above 650mV while the DTMOST device is exponential within a region from 100mV to 250mV (see Fig.2).
III. Current reference circuit.

The complete current bandgap reference circuit consists of DTMOST devices, a pair of cascoded current sources and a two-stage operational amplifier (see Fig.3). The voltage across the DTMOST is Conversely Proportional to Absolute Temperature (CTAT) and therefore also the current (I1) through resistor R2. On the other hand, the current (I2) through the DTMOST (T1) is directly Proportional to Absolute Temperature (PTAT) [3]. After an appropriate adjustment, superposition of the PTAT and the CTAT currents results in a temperature independent reference current.

IV. Experimental results.

A. Temperature dependence of the reference current.

Eight test chips were at our disposal. In order to vary the value of the PTAT resistor R1 (see Fig.2) was divided in sections, which can be externally bypassed. In this way the slope of the PTAT current could be trimmed to the slope of the CTAT current in order to achieve the minimum temperature coefficient of the reference current. Under that condition, the current to temperature relation is a parabolic function with a maximum deviation of less than 0.2μA (0.5%) in the range from 0°C up to 50°C (see Fig.4). When untrimmed the temperature coefficient of the reference current takes a turn to the worse and comes to the value of 0.06%/ºC.

B. Fluctuation of the reference current caused by irradiation.

We used the Nikhef’s in-house ⁹⁰Sr source for the irradiation of the chips. The effect caused by irradiation consists in the shift of the reference current while the circuit remains fully operational. As depicted in Fig.5 the reference current shifts in the range ±0.4μA (0.9%) after it has been irradiated with dose as high as 200Mrad.
C. Chip-to-chip spread of the reference current.

In some applications not only the stability of the reference current is important but also its absolute value. The absolute value differs from chip to chip. It is caused by the process variation. Based on measurements on a small number of (unselected) samples, the quadratic mean value of statistical spread of the reference current has been estimated as low as 0.6% (see Fig.6).

The present circuit has four outputs delivering different currents (see Fig.3). This topology makes it possible to construct a 4-bit DAC and adjust the value of output current.

![Figure 6: Chip-to-chip spread of the value of the reference current.](image)

- Variation of the output current caused by ionizing radiation up to dose of 200 Mrad is +0.9%.

VI. References.


Grounding, Shielding and Cooling Issues on LHCb Electronics at the LHC pit 8

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Abstract

The grounding, shielding and cooling issues are important factors in the design, the operation and the maintenance of all the electronics systems. Noise sources in High Energy Physics Experiments are specially taken into account. Inadequate grounding, shielding or cooling leads to unreliable operation of the particle detectors because most of them work with very low signal levels. After a brief review of the major environmental constraints, this paper provides an overview on the LHCb strategy and achievements in the field of the grounding, shielding and cooling for its electronics equipment at the LHC pit 8.

I. INTRODUCTION

The LHCb detector is designed to search for New Physics through the study of the CP violation in the B decays with the precise determination of the CKM parameters at the LHC collider [1]. The installation of the experiment started in 2002 was completed, except the muon station 1, in June 2008. The global commissioning is progressing well and the experiment is ready for data taking from August as scheduled. The experimental cavern (ex-DELPHI at LEP), 100 m underground at pit 8 is divided in two main areas. The layout of the experimental area (UX85 cavern) is shown in Figure 1.

II. ENVIRONMENTAL CONSTRAINTS

The various locations of the LHCb electronics are schematically shown in Figure 1 (areas noted 1, 2, 3, 4 & 5). The ECS crates nearby the sub-detectors are located at the balcony (VELO), at the “bunker” (OT, IT, RICHs, M1), at the top the calorimeters and inside the muon towers. These places were specified as the best compromise for LHCb. But, the large radiation shielding wall is a real barrier for all services (power, readout, control) which have to pass across via narrow chicanes in order to reach the protected area (UXA). The temperature and humidity in the UX85 cavern (UXA & UXB areas) are rather stable parameters, 20°C (+/- 1.5°C), 45% respectively. However, on the detector side, there is two major constraints, magnetic field and radiation.

A. Magnetic Field

The magnetic field generated by the large dipole magnet (3.6 Tm, 4.5 MVA, 6.6 kA, 1800 t) was simulated using VF OPERA-3d code [7]. The top view of the magnetic field map around the LHCb detector in the plan of the LHC beams is shown in figure 2. The electronics which were specified to be placed closest to the sub-detectors are located in areas below 5 mT in order to avoid the potential problems such as air cooling fans in the racks.

The detector area (UXB) is separated from the protected area (UXA) by a large radiation shielding wall [2] [3] of 3200 tons of concrete [4] [5]. The UXA area is essentially dedicated to the non-radiation tolerant electronics, such as the DAQ interface electronics and the PC farm of about 2000 computing nodes in its final configuration. The UXA area is always accessible when the LHC operates. The specification of the best compromise for the location of the electronics and the cabling lengths [6] was a real challenge at the LHC pit 8.

Figure 1: Top view of the LHCb experimental cavern

Figure 2: Magnetic field map in the LHC beam plane
B. Radiation

Radiation simulations using FLUKA code were performed [8] [9] for the large shielding wall. The ambient-dose-equivalent studies were essentially achieved for two cases: a) an accident scenario which consists of the full beam-loss, one proton beam at 7 TeV/c at the worst location of the LHCb Spectrometer and b) normal operation. The minimum shielding requirements for the concrete wall were specified to 3 m thick for the lower part and 2 m thick for the upper part of the wall protecting the counting house. The worst locations (7.2 mSv in the case of the beam-loss scenario) are just behind the chicanes dedicated to the cabling and services at the level of the second floor of the counting house. A radiation map in the vertical plan at the centre of the cavern is shown in Figure 3. The average value for the front part of the counting is about 4 mSv. For the normal operation the average value is about 5.6 10^{-2} µSv only. In fact, for the modular construction using an assembly of CERN standard concrete blocks (2400x1600x800 mm³; 7.5 t), the thickness of the concrete wall is about 3.2 m up to 4 m for the lower part and 2.4 m for the upper part providing the radiation protection expected. The holes such as the chicanes devoted to the long distance cabling and services are permanently supervised using six radiation monitors type IG5-H2O hydrogen filled ionization chambers.

Figure 3: Radiation map showing the counting house area protected against radiation in the case of the beam-loss scenario (one beam at 7 TeV/c). Limits (4.7 x 10^{14} protons): blue arrow = 20 mSv; red arrow = 50 mSv.

III. GROUNDING

The first purpose of the grounding is safety. But in addition, in order to reduce the impedances between the sub-detectors and the counting house (80-100 m far away), a high mesh earth network connecting all the metallic structures and all the electrical equipments is adopted for LHCb [11]. The safety earth cable interconnects all the metallic structures and the electrical equipments to the secondary star points of the main transformers and to the earth cables running both sides the UX85 cavern. The safety earth cables are also connected to the underground LHC machine earth with a connection to the surface where earth electrodes in the ground are available.

In order to increase the high meshed grounding network, all metallic structures such as cranes, rails, supports, platforms are interconnected both sides of the cavern in the UXA and the UXB areas at various locations. In addition, a grounding cable (120 mm²) is installed every 4 cable trays along the walls of the UX85. The cable trays are connected to this additional grounding cable every 5 meters.

At the 3 levels of the counting house (UXA zone), the beams supporting racks are interconnected to the copper grounding bars and the cooling pipelines. The copper ground bars interconnect all the electronics racks. The ground structure in the counting house is connected to the general grounding network in the cavern via the ground conductors, metallic structures and cable trays [12].

IV. SHIELDING

The shielding of electronic components is needed in order to get maximum immunity against external electromagnetic fields. In fact, there are three basic reasons for using shields: against capacitive coupling, against inductive coupling and radio-frequency (RF) environment.

The usual way to stop the capacitive coupling is to enclose the circuits or conductors to be protected in a metal shielding box (Faraday shield). The physical mechanism of the inductive coupling is magnetic flux lines from external interference sources, via current loops in the victim circuit, which generates a low voltage component (Lenz’ law). The potential sources in the UX85 area are the dipole magnet, transformers, power supply lines, electric motors and coils for the light tubes. A ground cable is placed inside every cable tray in order to minimize the pickup loop between the cable shields and the ground.

Changing electrical and magnetic fields may also generate RF interference problems. All signal wires are potential antennas for the reception and/or the transmission of RF noise. The general idea behind RF shielding is that varying fields induce currents into the shielding material. The induced currents dissipate heat from resistive losses or are re-radiated as RF reflections. The efficiency of a RF shielding is strongly dependent on the frequency, permeability and conductivity of the material used [6].
V. COOLING

All the racks located in the counting are directly cooled with mixed water (17°C). The muon, calorimeter electronic racks, IT & TT services boxes are also cooled with mixed water. The IT, TT, RICHs, VELO and OT have their own cooling system using specific coolants such as C6F14. These cooling units are installed in the accessible area (UXA). The specific coolants are supplied to the sub-detectors via transfer lines.

As an example the LHCb electronic racks located under the “bunker” is shown Figure 4.

![Figure 4: Electronics under the “bunker”](image)

VI. CONCLUDING REMARKS

The sub-detectors are controlled by the Detector Control System (DCS). In addition, in case of the DCS failures the Detector Safety System (DSS) prevents all possible damages of the equipment [14]. The DSS, based on redundant PLC, is a robust and reliable system, permanently working including when the power and/or network cuts occurred. Suitable sensors for all the sub-detectors and associated infrastructure are installed in order to protect the whole equipment and in particular electronics by switching off electric power. The DSS assures the following tasks [15]:

- Protection of the front-end-electronics (FEE) by measuring temperature (nearby voltage regulators) and action using thermo-switches.
- Supervision of the various cooling systems (e.g. measures of temperature and flux of mixed water for the MARATHON power supplies).
- Protection of the crates inside the racks by measuring the temperature and detecting smoke from the ventilation air.
- Triggering an extinguishing CO2 system for rapidly fighting fire in the racks.
- Protection against water leaks (e.g. water leak sensors dedicated to the Trigger Tracker (TT) services boxes.

- Switching off the high voltages in case gas problems in the sub-detectors (e.g. muon chambers).

DSS checks also the temperature, the humidity of the ambient air of the cavern, the counting house and the gas room, in order to avoid possible problems with the air conditioning units. In addition, the system provides information about the presence of smokes everywhere in the cavern through the independent fire detection system.

VII. REFERENCES

Radiation damage of SiGe HBT Technologies at different bias configurations

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Abstract

SiGe BiCMOS technologies are being proposed for the Front-end readout of the detectors in the middle region of the ATLAS-Upgrade. The radiation hardness of the SiGe bipolar transistors is being assessed for this application through irradiations with different particles. Biasing conditions during irradiation of bipolar transistors or circuits have an influence on the damage and there is a risk of erroneous results. We have performed several irradiation experiments of SiGe devices from IHP in different bias conditions. We have observed a systematic trend in gamma irradiations, showing a smaller damage in transistors irradiated biased compared to shorted or floating terminals.

I. INTRODUCTION

The LHC at CERN is expected to start taking data during next year. In the meantime, a new project has started to try and extract more physics benefits after its expected life span of 10 years. The plan is to upgrade the accelerator in order to increase its luminosity in around one order of magnitude, it is called the Super-LHC. It has been shown that this will force the modification of the different experiments installed in the accelerator. In particular, all the inner detector of the ATLAS detector will have to be upgraded. Some of the microelectronics technologies proposed for the front-end readout of the detectors in the middle region of the upgraded inner detector are the SiGe BiCMOS technologies. These technologies should provide better performances in terms of power consumption, signal to noise, and processing speed, but they have to be evaluated in terms of radiation hardness.

In order to perform this evaluation, the devices should be submitted to different irradiation experiments, and then measure their performance after irradiation. These experiments are usually performed in complex irradiation facilities with difficult access to the irradiation area. This complicates the irradiation setup, in particular, biasing the devices during irradiation in order to mimic the real conditions is very difficult, and often impossible. This work studies the results of radiation damage in the SiGe HBT transistors when submitted to irradiations in various bias configurations, in order to verify the validity of irradiation experiments carried out at bias conditions different from the real case.

We have performed irradiations of SiGe HBT transistors with Co60 gamma particles in three different bias configurations: biased in forward active region (in similar conditions as they will be working in the real experiment); with all their terminals short-circuited; and with all their terminals floating. Differences in radiation damage have been observed for SiGe transistors submitted to gamma irradiations in biased configuration with respect to shorted and floating configurations. Biased transistors suffer less current gain degradations than shorted transistors, and these suffer less degradations than floating transistors.

The variation of radiation damage in time after irradiation (annealing) has also been studied in order to discard differences in radiation degradation coming only from different degree of annealing of the damage due to their different biases during irradiation. Transistors have been measured right after irradiation, and then left for some time in the same bias conditions and at room-temperature, then re-measured. Less annealing has been observed for gamma irradiations in the biased transistors indicating that some of the damage differences observed actually come from different annealing levels, nevertheless some differences in damage remain after the full annealing process.

II. MOTIVATION

In our radiation hardness studies of bipolar technologies previous to the present work, in the framework of the radiation hardness tests of the front-end electronics of the ATLAS-SCT detector [1], we had performed several experiments irradiating bipolar transistors with gamma rays in different bias configurations. Our results from those experiments (unpublished) always indicated that ionizing radiation effects in devices with floating terminals were more intense than those on devices whose terminals are wire bonded and biased, regardless of dose rate, temperature, or device type (NPN, PNP). An example of this can be seen in Figure 1, which shows the excess base current density, defined as the base current density increase after irradiation ($\Delta I_B = I_B - I_B^0$) at $V_{BE} = 0.7$ V, of transistors from the MAXIM’s CB2 bipolar technology (well described in [2]), gamma-irradiated at a wide range of total doses from 100 krads(Si) to 10 Mrads(Si). In that figure, filled points represent single-transistor results, and empty symbols correspond to the calculated averages for all transistors irradiated at the same total dose and bias configuration. As it can be seen, there is a clear increase in radiation damage on devices irradiated with terminals floating compared to those irradiated in biased configurations for the whole range of doses.

One can deduce from these results, that there is a risk of largely overestimating the damage that bipolar transistors will receive in the real experiment when performing experiments in unrealistic bias conditions. Therefore, one could decide to reject some technologies or designs (ICs) as candidates for the experiment under wrong assumptions. In the light of these
results, we decided to perform a systematic study on the effects of the bias configuration during irradiation (bias effects) on the radiation degradation of bipolar transistors for high energy physics applications.

III. EXPERIMENTAL DETAILS

In order to perform a systematic study of the bias effects under ionizing radiation, we irradiated several bipolar devices, in three different bias configurations:

(a) All terminals floating.
(b) All terminals shorted together.
(c) Transistor biased in forward active region with $V_{BE} \approx 0.7$ V and $V_{CB} = 0$ V.

The transistors used for the study are included in test chips fabricated on a SiGe:C HBT technology from Innovation for High Performance Microelectronics (IHP) [3]. The technology, called SGB25VD, presents the following key characteristics: $f_T = 75$ GHz, $BV_{CEO} = 2.4$ V, $\beta = 190$. An schematic cross-section of the NPN transistor of this technology can be seen in Figure 2. This is one of the technologies being studied as candidates for its use in the front-end electronics of the ATLAS Upgrade for the Super-LHC at CERN [4].

All transistors were irradiated with gamma particles in the same conditions other than the bias configuration. The total dose reached was 5 Mrad(Si), at a dose rate of 342 rad(Si)/s. The irradiations were carried out in the Nayade facility at CIEMAT (Madrid, Spain), a water well Co60 irradiator. The dosimetry was performed by means of a Fricke system [5]. All irradiations were performed using a PbAl shielding box to avoid dose enhancement effects due to secondary photons and to reach charged particle equilibrium at the samples, according to irradiation standards [6]. The devices remained close to room temperature during irradiation. The temperature of the samples during irradiation was obtained via PT100 sensors.

![Figure 2: Cross sections of the NPN SiGe:C heterojunction bipolar transistors (HBT) used. The devices stem from IHP’s BiCMOS technology SGB25VD.](image)

Before irradiation the devices were measured first on wafer. Then, the wafers were cut and the selected test chips were wire bonded to the biasing boards, except for the ones that were to be irradiated in floating configuration which remained with their terminals pads floating during the whole experiment (obviously, except for the short testing cycles). Devices were then, re-measured to make sure that their characteristics had not changed or that they had not died during the bonding process. After irradiation, all devices were kept at low temperature ($< 0$ °C) in order to avoid annealing until they were measured. Then they were left for annealing at room temperature with their terminals shorted together and grounded, except for the devices irradiated in floating configuration which were left also floating for the whole annealing process. Several measurements were later performed at consecutive time periods, systematically observing a beneficial annealing of the damage. Beneficial annealing proceeds for around two weeks until it reaches a saturation. The final stable value after saturation of the annealing was taken as the final result of the irradiation.

The measurements were performed with a Keithley 4200 Semiconductor Characterization System and the use of a manual probe station and microprobes. The environmental temperature of the laboratory was measured during the tests process. This temperature remains in the range of $25 \pm 2$ °C. Nevertheless, a commonly used correction for small temperature differences has been used for the base current by applying a factor to the post irradiation value which is equal to the ratio between the pre- and post- irradiation value of the collector current (which is known not to be affected by gamma radiation) [7]. Forward Gummel plots of the transistors were obtained, and the following figures-of-merit for the radiation damage were extracted from them: $\text{Final Current Gain} (\beta_F)$; defined as the post-irradiation common emitter current gain of the transistors at $V_{BE} = 0.7$ V; $\text{Normalized Current Gain} (\beta_N)$; defined as the ratio between post- and pre-irradiation common emitter current gain ($\beta_F/\beta_0$) at $V_{BE} = 0.7$ V; and $\text{Excess Base Current Density} (\Delta J_B)$; defined as the difference between post- and pre-irradiation base current density at $V_{BE} = 0.7$ V.
IV. RESULTS

The radiation damage suffered by transistors submitted to gamma irradiations in different bias configurations is shown in Figure 3 in terms of the Excess Base Current Density \( (\Delta J_B) \) after annealing. As it can be seen, less damage is obtained for transistors irradiated in biased configuration than for the transistors with their terminals shorted or floating. Also, floating transistors suffer the most damage among all cases. Overall, the damage differences observed are small at the dose reached of 5 Mrads(Si), but higher differences can be expected at radiation doses where the devices are closer to the edge of their usability. This has been observed in previous results as the ones presented in Section II, and other irradiations that we have performed. Quantitative differences with other cases are related to technological diversity which make some devices relatively more immune to ionization damage (quality of spacer oxide, size, etc).

As it has been mentioned above, the results presented correspond to measurements of devices after annealing has taken place. During the annealing process, the damage produced by radiation is reversed in some amount, in a process called “beneficial annealing”. This process continues for a few days (5-10), at room temperature, until it reaches a saturation point after which the damage level of the transistors remains stable. This is the reason why this saturation point is usually taken as the final value of the ionization damage in bipolar transistors. We have monitored the annealing of the devices, taking intermediate measurements for several days along the whole process. Figure 4 shows the post-irradiation current gain \( (\beta_F) \) of the irradiated transistors throughout the whole annealing process until it reaches a saturation, for all the transistors irradiated in the different bias configurations. The saturation in the annealing can be easily seen after about 5 to 10 days at room temperature.

This annealing behavior of the irradiation damage in bipolar transistors, could raise some doubts about the possibility that the differences in radiation damage observed for the different bias configurations could be only related to differences in annealing for the different transistors, and not to actual irradiation bias effects. In order to address this question we have compared the annealing of the devices, along the whole process.

Figure 5 shows the total beneficial annealing occurred for the transistors irradiated at different bias configurations. Annealing is shown in terms of the excess base current density as the difference between the final stable value after the annealing process has taken place, and the initial value obtained in measurements taken right after irradiation. As it can be seen, no significative differences are observed in the annealing of the transistors for the different bias cases. Therefore, it can be concluded that the differences observed in radiation damage of devices irradiated at different bias configurations is an effect related with these bias configurations and not with annealing differences.
V. CONCLUSIONS

Systematic less damage is observed for bipolar devices irradiated in biased configuration with respect to shorted or floating terminals configurations. Floating devices appear to suffer the highest damages of all the cases. Grounded configuration appears as a "worst-case" configuration in the sense that irradiations performed in these conditions will overestimate the damage in small amounts. Annealing differences are not responsible of the differences observed in the damage for the different configurations.

At the view of these results some practical recommendations can be made when performing irradiation experiments of bipolar technologies for high energy physics applications, where devices are usually biased when they are exposed to radiation in the real life. Special care should be used when trying floating configuration as there is the risk of largely overestimating the damage produced on the transistors. Shorting all the terminals together can be a good practice when biasing the devices can be too difficult or even impossible in the radiations sources used. Quantitative differences seem to be important among technologies, therefore studies of this kind should be performed when considering experiments in bias configurations different from the real-life.

VI. ACKNOWLEDGEMENTS

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VII. REFERENCES

PMm2 ASIC: PARISROC

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Abstract

PARISROC is a complete read out chip in AMS SiGe 0.35µm technology for photomultipliers array. It is made to allow triggerless acquisition for next generation neutrino experiments. The ASIC integrates 16 independent channels with variable gain and provides charge and time measurement with a 12-bit ADC and a 24-bits Counter.

I. INTRODUCTION

The PMm2 project [1] proposes an innovative electronics for array of photodetectors used in High Energy Physics and Astroparticle. The goal is to develop a macro pixel made of 16 small photomultiplier tubes connected to an autonomous front-end electronics, as shown in Figure 1, in order to segment very large surface of photo-detection.

This R&D [2] involves three French laboratories (LAL Orsay, LAPP Annecy, IPN Orsay) and PHOTONIS company, the French photomultiplier tube maker as shown in figure 2. It is funded for three years by the French National Agency for Research (ANR) under the reference ANR-06-BLAN-0186.

The micro-electronics group (OMEGA) from the LAL at Orsay is in charge of the front-end electronics and develops an ASIC called PARISROC (Photomultiplier ARray Integrated in Sige ReadOut Chip) described below.

II. ASIC ARCHITECTURE

A. Requirements

The Electronics must be autonomous, triggerless and with 16 independent channels. It must provide charge and time measurements. The charge measurement has to be efficient for 1 photo-electron and with a good linearity on a dynamic range up to 300 photo-electrons. The time measurement is done in two steps: a coarse measure with a 24 bit counter at 10MHz and a fine measure on a 100 ns ramp to achieve a resolution of 1ns. Because of the common high voltage supply, the preamplifier gain must be adjustable channel by channel in order to compensate the photomultiplier tube gain variation. Output data are serialized to be sent by only one communication wire.

B. Global architecture

The global architecture of the ASIC is shown in figure 3. It is composed of 16 analogue channels managed by a common digital part.

A bandgap bloc provides the common voltage references for fast and slow shapers. The threshold of the discriminators is common for the sixteen channels and given by a 10 bit DAC. The ramps for ADC and TDC are common for all the channels.

C. One channel detail

The detail of one analogue channel is given in figure 4. Each channel is composed by a low noise preamplifier with...
variable and adjustable gain. The variable gain is common for all channels and can change from 8 to 1 on 4 bits. The gain is also adjustable channel by channel by a factor 4 on 8 bits.

![Figure 4: One channel schematic](image)

The preamplifier is followed by a slow channel for the charge measurement in parallel with a fast channel for the trigger output. The slow channel is made by a slow shaper followed by an analogue memory with depth of 2 to provide a linear charge measurement up to 50pC; this charge is converted by a 12 bit Wilkinson ADC. The fast channel is composed of a fast shaper (15ns) followed by 2 low offset discriminators to auto-trig down to 10fC. The thresholds are loaded by 2 internal 10-bit DACs common for the 16 channels plus a 4bit DAC per channel for one discriminator. The 2 discriminator outputs are multiplexed to provide only 16 trigger outputs.

The fine time measurement is made by an analogue memory with depth of 2 which sample a 12 bit ramp as the same time of the charge. This time is then converted by a 12 bit Wilkinson ADC.

D. Digital part

On overview of the digital part is given in figure 5. The digital bloc manages the track and hold system like a FIFO and starts and stops all the counters [3]. All the data are serialized to be sent out.

![Figure 5: Digital part overview](image)

There are two clocks: one at 40 MHz for the analogue to digital conversion and for the track and hold management, the second at 10MHz for timestamp and readout.

The readout format is 52 bits: 4bits for channel number + 24 bits for timestamp + 12 bits for charge conversion + 12 bits for fine time conversion. The readout is selective: only the hit channels are read; so the maximum readout time will be 100µs if all channels are hit.

E. PARISROC layout

Figure 6 presents the PARISROC layout. The circuit has been designed in AMS SiGe 0.35µm technology [4]. The die has a surface of 17 mm² (5mm X 3.4mm) and will be package in CQFP160 case.

![Figure 6: PARISROC layout](image)

PARISROC was sent in foundry on June and the dies are expected for the end of September 2008.

III. ANALOGUE CHANNEL SIMULATIONS

A. Preamplifier

1) Input signal

For all the simulations, except for the photomultiplier gain adjustment, we use a triangle as input signal to simulate the photomultiplier signal. It is a 4.5ns rise and fall time with a 1ns duration current signal as shown in figure 7. This current signal is sent on an external resistor (50 Ohms) and varies from 0 to 10mA in order to simulate a PMT charge from 0 to 50pC which represents 0 to 300 photo-electrons when the PM gain is $10^6$.

![Figure 7: Input signal used for simulation](image)
2) **Preamplifier response**

The preamplifier gain is given by the ratio between the input capacitance ($C_{in}$) and the feedback capacitance ($C_f$). This gain can vary from 8 to 1 by changing $C_{in}$ on 4 bits for the sixteen channels together.

The figure 8 gives the preamplifier response at gain 4 for an input charge from 0 to 50pC.

![Figure 8: Preamplifier response at gain 4 with input charge from 0 to 300 photo-electrons](image)

3) **Photomultiplier gain adjustment**

On the preamplifier the feedback capacitance ($C_f$) value could be changed to adjust the photomultiplier plus preamplifier gain channel by channel. The typical value of $C_f$ is 0.5pF and can be changed by a factor four on 8 bits (from 125fF to 2pF by step of 17fF). The figure 9 shows the preamplifier output for the same input charge (a square pulse with 1ns rise and fall time and 9ns duration) when the feedback capacitance varies.

![Figure 9: Preamplifier output for various $C_f$ (a: from 1pF to 2 pF, b: from 0.25pF to 1pF)](image)

### B. Slow shaper

1) **Response at 1 photo-electron**

The shaping time constant can be chosen between 50ns, 100ns or 200ns but it is common for all channels. The slow shaper response at one photo-electron for the various time constant is shown in figure 10 and the main characteristics (gain, peaking time, noise and signal over noise) of these signals are listed in Table 1.

![Figure 10: Slow shaper response at 1 p.e. for various shaping time](image)

<table>
<thead>
<tr>
<th>Time constant</th>
<th>$V_{out}$ @ $T_p$</th>
<th>RMS noise</th>
<th>S/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>50ns</td>
<td>19mV @ 37ns</td>
<td>1.6mV</td>
<td>11</td>
</tr>
<tr>
<td>100ns</td>
<td>10mV @ 75ns</td>
<td>1.2mV</td>
<td>8</td>
</tr>
<tr>
<td>200ns</td>
<td>5mV @ 122ns</td>
<td>95µV</td>
<td>5</td>
</tr>
</tbody>
</table>

2) **Linearity**

Figure 11 gives the simulation of the linearity for preamplifier gain 8 and 4. For the preamplifier gain 4, the non-linearity is very good (less than 0.5%) for an input charge until 330 photo-electrons. Of course when the gain doubles the input dynamic range is divided by two for the same non-linearity.

![Figure 11: Slow shaper linearity and residuals for gains 4 and 8](image)

3) **Slow shaper response**

The slow shaper is a CRRC2 with variable time constant. The figure 12 shows the slow shaper response with an input charge from 0 to 2pC. The gain of the preamplifier is 4 and the time constant of the shaper is 200ns.

![Figure 12: Slow shaper response with an input charge from 0 to 2pC](image)
C. Fast shaper

The fast shaper is a CRRC with a time constant of 15ns and with high gain to send high signal to discriminator. The goal is to trigger easily on the third of photo-electron. The figure 13 shows the fast shaper response for an input charge from 0 to 2pC.

The fast shaper response at one photo-electron is a signal of 65mV at a peaking time of 7ns. The RMS noise is around 2.3mV which gives a signal over noise ratio of 28.

D. Discriminator

The discriminator is only a simple low offset comparator. The threshold is common on the 16 channels and provided by a 10 bit DAC. The threshold can be set at one third of the photo-electron. The output duration depends on the input signal amplitude as shown in figure 14. Figure 15 is an enlargement of the discriminator rise time in order to see the time walk of around 4 ns.

IV. CONCLUSION

PARISROC is a dedicated circuit to readout the photomultiplier array. It was designed in AMS SiGe 0.35µm and sent in fabrication in June 2008. The circuits are expected for end of September. The test board is now in layout and will be available in end of October. The first measurement results will arrive at the end of the year.

V. REFERENCES

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Radiation Resistant DC-DC Power Conversion with Voltage Ratios > 10 Capable of Operating in High Magnetic Field for LHC Upgrade Detectors

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Abstract

Commercial power converters that have voltage ratios greater than ten and are capable of running near the LHC collision region would increase the efficiency of the power distribution system of the ATLAS Silicon Tracker high luminosity upgrade. The devices must operate in a high magnetic field (2 T) and be radiation hard to \(2 \times 10^{15}\) Neq/cm\(^2\) and \(50-100\) Mrad. These converters are to be mounted on the same multi-chip modules as the ASIC readout chips or in close vicinity without introducing any additional readout noise due to the high switching frequencies. Such devices will permit higher voltage power delivery to the tracker and thus increase overall power efficiency by limiting the ohmic losses in the stretch of cable (about 100 meters) between the tracker and the power sources.

I. Introduction

There is a clear need for a new system of power delivery for the upgraded Atlas Silicon Tracker for the SLHC. With the planned changes the existing powering scheme will have an estimated efficiency of about 10% if the existing cables are reused. Due to space and mass constraints these cables would be difficult to change or made larger. A system featuring DC-DC converters with a voltage ratio of ten would result in an estimated efficiency on the order of 70-80% using the existing cables.

One approach to DC-DC conversion utilizes the buck regulator architecture. DC-DC buck converters with our electrical requirements are commonly used in the commercial market. We have been surveying and testing currently available devices to understand the present state of the art.

The challenging environment and the limited volume impose formidable technical requirements. Foremost in unique requirements is operation in a high magnetic field. This necessitates the use of an air core inductor, requiring high switching frequencies that lie in the bandwidth of the readout ASIC. Because of this, switching noise introduced by the converter into the data is a serious concern. In addition, the radiation hardness of the devices, and the relatively high voltage ratios needed are also of primary concern.

In 2007, we had tested a number of devices that, although lacking the high voltage ratios required, enabled us to learn a number of lessons. For example, one device that we irradiated with gammas up to 100 Mrad showed no change in performance. This proved that at least one commercial device was inherently radiation hard. Also, we conducted noise tests with our own custom module utilizing current Atlas ABCD Asics connected to a large silicon strip detector and mounted with a daughter buck regulator board. There was no noise increase due to switching noise on the power and ground. However, magnetic/electrical pickup on the 8 cm silicon strips from the air-core inductor required shielding to reduce the noise to a satisfactory level.

Commercial requirements are now driving the development of a new generation of converters with voltage ratios greater than 10. Following are the results of the irradiation of some of these new converters. Additionally, we have fabricated and tested several small \(\mu\)H inductors with the results reported below.

![Figure 1: Power Distribution Schemes, Efficiencies and Air Coils.](image-url)
II. Need for New Methods of Power Distribution

The LHC inner detector electronics currently use low voltage DC power supplies located a long distance away (30 m for CMS and 140 m for ATLAS detector). Here we examine a power supply solution for the upgraded silicon tracker which would use 10 times more detecting elements for a future SLHC that would be designed to deliver 10 times higher luminosity. The Power Delivery plot in Figure 1 illustrates the problem. At present 10.25 V power is delivered by 4088 power cables each with a resistance of 4.5 Ω. The 10 chip ASIC readout it supplies needs 1.5 amps @ 3.5 Volts. This results in a power delivery efficiency of ~33% as shown in the bar graph. In an upgraded ASIC design with finer lithography and x2 more chips, the voltage required is estimated to drop to 1.3 V. Using the same power delivery scheme and the same cables would decrease the power delivery efficiency to 10%. By placing a DC-DC converter with a voltage ratio, \( V_{\text{in}}/V_{\text{out}} = 10 \) on the 20 chip hybrid Kapton PCB would provide an efficiency of 70 - 80%. However, unlike the existing scheme, this places the converter down in the harsh environment of the silicon tracker.

Some of the requirements for a buck converter used in the upgraded Silicon Tracker would be:

- High radiation tolerance ~ 100 Mrad, \( 10^{15} \text{n}_{\text{eq}}/\text{cm}^2 \)
- Magnetic field immunity to 2 Tesla or higher.
- Construction from nonmagnetic materials
- High efficiency
- Air core Inductors – Solenoid, Toroid, Spirals etched on Kapton

As stated in the introduction this study began in 2007 with some of the newer COTS (Commercial off the Shelf) commercially available power converters to determine whether any were inherently radiation hard. The very first selected chip (EN5360) survived 100 Mrad of \(^{60}\text{Co}\) exposure without any noticeable damage. This was followed by studying noise issues since these chips switch in the low MHz range. These results were reported at the TWEPP 2007 in Prague [1].

III. Selected Commercial Devices and Performance

The focus for the past year has been to evaluate additional commercial converters that may provide higher input to output voltage ratios and to test a few devices with \(^{60}\text{Co}\) radiation. Table 1 lists a few commercial devices selected on the basis of the following criteria:

1. New products/designs.
2. Finer lithography, preferably 0.25 µm CMOS.
3. Higher input/output voltage ratio.
4. Single die fabrication (exception, the Maxim device that has 3 chips including 2 external FET Switches.

5. Additional products from Enpirion. The EN5360 had previously survived 100 Mrad of \(^{60}\text{Co}\). EN5382 is a similar chip made by the same company.
6. Availability of PC Evaluation Boards to speed up the evaluation process and allow standardized testing.

Semiconductor companies are working on Buck converters designed to meet the needs of the embedded industrial and blade computing applications, where 12 Volts is distributed to local PC boards with multiple buck converters to generate multiple voltages for microprocessors, IO, FPGAs etc. For these applications, vendors are working to achieve higher values of \( V_{\text{in}}/V_{\text{out}} \) by using higher frequencies to decrease the size of inductors and capacitors.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Evaluation Board @ Yale</th>
<th>Device Type</th>
<th>( V_{\text{in}}/V_{\text{out}} )</th>
<th>Technology</th>
<th>Frequency MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST</td>
<td>Yes</td>
<td>ST1S10</td>
<td>10</td>
<td>BCD</td>
<td>0.9</td>
</tr>
<tr>
<td>TI</td>
<td>Yes</td>
<td>TPS62110</td>
<td>10</td>
<td>BCD 0.25 µm</td>
<td>1</td>
</tr>
<tr>
<td>IR</td>
<td>Yes</td>
<td>IRDC 3322</td>
<td>10</td>
<td>BCD 0.25 µm</td>
<td>1</td>
</tr>
<tr>
<td>Maxim</td>
<td>Yes</td>
<td>MAX 8654</td>
<td>10</td>
<td>BCD 0.25 µm</td>
<td>1</td>
</tr>
<tr>
<td>Intoric</td>
<td>Yes</td>
<td>IL6652</td>
<td>10</td>
<td>BCD 0.25 µm</td>
<td>1</td>
</tr>
<tr>
<td>Analog Devices</td>
<td>Yes</td>
<td>AS2100</td>
<td>2:1</td>
<td>MIX 0.25 µm</td>
<td>1</td>
</tr>
<tr>
<td>Enpirion</td>
<td>Yes</td>
<td>EN5360</td>
<td>10</td>
<td>BCD 0.25 µm</td>
<td>1</td>
</tr>
<tr>
<td>Enpirion</td>
<td>Yes</td>
<td>EDO 5360</td>
<td>10</td>
<td>BCD 0.25 µm</td>
<td>1</td>
</tr>
</tbody>
</table>

Most of the selected devices can run at higher voltage ratios. However, this is at a cost of lower efficiencies due to high rms current losses. This is shown in Figure 2 for ST1S10.

Generally, the chips are designed for lower switching losses in the top MOSFET [1] while the bottom MOSFET is designed for lower ohmic resistance. This is because the top MOSFET is on for a much smaller period of time than the bottom MOSFET with the switching losses being a much larger fraction of the total power in the top device. As an example, for a 10:1 voltage ratio the top MOSFET switch is on for 10% of the time while the bottom MOSFET is on 90% of the time.

In addition, these converters specify minimum turn on times of about 100 ns. This then limits the maximum operating frequency to about 1 MHz for a 10:1 \( V_{\text{in}}/V_{\text{out}} \). The chip itself may be able to operate at a much higher frequencies.
IV. Air Core Coils and AC Resistance Effects

This year we have explored coil designs and commercial converter chips. The solenoids and toroids tested last year were thicker components and were difficult to flatten. It may be possible to wind a toroid with specially shaped and laser cut copper foil [2].

Figure 3 shows the power conversion efficiency versus output current and compares the factory mounted ferrite inductor provided on the evaluation PCB and an air core solenoid of lower inductance. The efficiency gap between the two inductors is greatest at lower currents.

The skin effect forces the current to be carried near the surface of the conductor. To analyze this note that the coil designs in Figure 1 use two ounces of Copper/ft² for the coil traces. At a switching frequency of 1 MHz, the skin depth in copper is 66 µm while the thickness of the 2 oz copper trace on the PCB is 70 µm. Hence, at 1 MHz, there is no appreciable change in the AC resistance with respect to the DC case caused by the skin effect.

The proximity effect [3-5] significantly increases the AC resistance of an adjacent conductor. A changing magnetic field will influence the distribution of an electric current flowing within an adjacent conductor due to induced eddy currents thus reducing the cross section for the current flow.

The additional resistance increases electrical losses which, in turn, reduce efficiency and complicate the cooling of the coils. We investigated connecting multiple spiral coils in series and close proximity to increase inductance as this may be necessary to achieve the inductance necessary for a high $V_{in}/V_{out}$ ratio.

Measurements were made with two of the large coils of Figure 1 connected in series. The increase in inductance and resistance was measured versus coil spacing at frequencies of 100 kHz and 1 MHz. The resistance increase is x16 when the coils are pressed together and a factor of 3 to 4 when close but still separated. See table 2.

<table>
<thead>
<tr>
<th>Coil Spacing</th>
<th>100 KHz</th>
<th>1 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wide</td>
<td>L 1.21 µH, 1.16 µH</td>
<td>R 0.098 Ω, 0.094 Ω</td>
</tr>
<tr>
<td>Near but not touching</td>
<td>L 1.80 µH, 1.70 µH</td>
<td>R 0.098 Ω, 0.300 Ω</td>
</tr>
<tr>
<td>Pressed Together</td>
<td>L 2.37 µH, 1.93 µH</td>
<td>R 0.080 Ω, 1.300 Ω</td>
</tr>
</tbody>
</table>

To further illustrate this effect, 3 medium coils from Figure 1 were connected in series and placed parallel to each other with spacers in between them. Figure 4 shows the results of the efficiency change with different Mylar spacers and copper clad boards on the outside.
V. Radiation Testing

Manufacturer designed evaluation boards (Figure 5) were used for all converter device testing. The same connector is used on each board for interchangeability.

The boards were irradiated at the BNL Gamma Irradiation Facility which contains a 2500 Curie 60Co source. Generally a converter was biased at the maximum input operating voltage and an output load of about 1 amp. The dose rate for all converters was 200 krad/hour. The input and output currents and voltages were monitored and periodically recorded by a scanning DVM before, during and after irradiation. During irradiation most of the devices developed problems and the exposure was stopped. Only the EN5360 continued to function properly as noted in Table 3.

Table 3 also includes the observed damage modes for the devices tested.

VI. Enpirion Devices

In radiation testing in 2007 the Enpirion device EN5360 exhibited little radiation damage while in 2008 all tested irradiated devices from all manufacturers showed significant damage at doses less than 200 krad including another Enpirion chip EN5382. This motivated us to retest the EN5360 chip in 2008 to confirm the 2007 results.
Figure 6 Efficiency change during irradiation at a constant output current of 1 Amp for an EN5360 DC-DC Converter

This behavior continued during the remainder of the irradiation with some recovery occurring during periods when the irradiation was halted. By the time 48 Mrad was reached the efficiency was about 76%. Shown in Figure 7 below are the before and after irradiation efficiency measurements made at Yale on the same device which confirm the observations during irradiation.

Figure 7: Efficiency Enhancement caused by Gamma Radiation: Verifying the unradiated eval board behaved the same in the testing setup reaffirmed that the changed bias current caused the efficiency to shift. Comparing data and calculating values showed this to be true

The EN5360 was produced by IHP Microelectronics foundry in Germany while successor devices which show radiation damage at much lower doses are fabricated by Dongbu HiTek semiconductor in South Korea. Both use a 0.25 μm CMOS process, but some differences in the foundry processes and/or in the device circuit design make the EN5360 radiation hard.

Recently Los Alamos National Laboratory irradiated an EN5360 and its successor EN5365 with heavy ions and protons for space satellite qualification [6]. They concluded that while both are suitable for their purposes, the EN5360 showed no effect well beyond their proton dosage limit while EN5365 exceeded their proton dosage limits. Hence for the lower orbit space applications both of these devices are suitable.

VII. Conclusion / Future Work

Enpirion EN5360 demonstrates that a commercial COTS device can be radiation hard. While we have reason to expect some next generation high voltage ratio 0.25 μm devices might similarly prove rad-hard, all of the devices we tested showed radiation damage at doses less than 200 krad. We are attempting to understand differences in the IHP fabrication process that lead to a successful device. Additionally, as next generation devices come on the market we will use the infrastructure we developed to quickly evaluate these devices.

VIII. References

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2. M. Nigam & C. Sullivan, Multi-Layer Folded High-Frequency Toroidal Inductor Windings, IEEE APEC Conference, February 24-28, 2008, Austin, TX, USA
6. Matthew Stettler & Mike Pigue, Los Alamos National Laboratory, NM, USA , Private communication
Abstract

The hadronic Tile Calorimeter (TileCal) of the ATLAS detector at LHC has a digitization, pipeline and readout system composed of nearly 2000 boards [1][2], developed and maintained by Stockholm University. Prior to now a rather complex test system been used to verify the functionality of the boards. However this system was developed nearly 10 years ago and now difficult to maintain due to several already obsolete components. A new, simpler, more reliable, and portable test system was therefore initiated. Its components have been chosen to reduce problems with obsolescence, and to allow easy migration to new platforms over the lifetime of the digitizer system.

I. LEGACY SYSTEM

The original system for testing digitizer boards during development and manufacturing (Figure 1) is now over 10 year old. It contains several key components that would be difficult to replace in case of failure. The VME computer that controls the TTC system, for instance, has an obsolete architecture and operating system. The PMC optical receiver board that it hosts cannot be installed on many new systems. And if it can, there is still the problem of finding suitable drivers and subroutine packages. The aging hardware is causing increased instabilities. The documentation does not answer all questions. And perhaps most importantly, most of the persons that were involved in the development of the system over a long period are no longer available.

The legacy test system was intended for in-house testing and debugging of digitizer hardware in Stockholm. Ideally we want a more modern, practical test system that can even test the digitizer system in situ.

II. NEW SYSTEM

The new test system is based on commercially available components, for easy upgrade and service. It consists of a Xilinx development board (ML506) [3] (Figure 2), equipped with a Small Form-factor Pluggable (SFP) module for optical transmission and reception, and an optional laptop PC. The system communicates with the digitizers by transmitting TTC signals and receiving high-speed (G-Link) readout signals through the same SFP module, utilising a single gigabit transceiver on the Virtex-V FPGA (Figure 3). The FPGA can easily be reconfigured for future upgrades and improvements, such as hardware acceleration for different high-speed tests. It also contains an embedded CPU system running test software on Linux [4]. Hence we have replaced the previous crate system with a single board.

The board communicates with a host computer over Ethernet, allowing the debug software to be run remotely. The main debug software runs in a virtual environment for easy maintenance and compatibility.

Figure 2: Xilinx ML506 development board (left) and full test system, including a complete set of drawer electronics (right)

Figure 3: Diagram of the new test system.

Figure 1: The legacy test system: complex and obsolete.
III. DESIGN CHALLENGES AND SOLUTIONS

To create this system several design challenges had to be solved, including FPGA emulation of the TTC system and the Agilent G-link receiver.

A. Generation of the TTC signal

All configuration and command signals are transmitted to the digitizer system via the TTC system [5]. Therefore the TTC system needed to be emulated inside the FPGA. Currently the system uses a 100 MHz crystal oscillator to generate the 40 MHz clock on the receiver side, but the board could be equipped with an extra crystal oscillator to generate the 40.08 MHz clock too.

B. Receiving the G-Link signals

The digitizers transmit data to a link card, which in turn transmits them to the readout system over a high-speed Agilent G-Link [6] communication link. Therefore a G-Link receiver emulator was developed for FPGA as well, using one of the multi-gigabit transceiver GTPs included in the Virtex-V. Since the G-Link protocol is different from other common protocols on the market, some tricks with the GTP were needed: A Clock Data Recovery unit (CDR) is used to lock the receiver to the source frequency and the G-Link idle pattern is used as a comma character, to make the receiver align to the right bit pattern. The G-Link decoding is then implemented in normal logic cells. However, since the board has only one SFP module, both TTC and the G-Link needed to share the same GTP resource.

C. TTC and G-Link through the same SFP module

Transmitting TTC and receiving G-Link through the same SFP module is not supported by the module vendors, since the TTC is using 1300 nm wavelength and the G-Link is using 850 nm. Usually one SFP module supports only the same wavelength on both transmitting and receiving side. However, due to the good quality of optical transceivers on both sides the communication is very stable in both directions, even though they are used outside their specifications.

D. Embedded system running Linux

To control the TTC transmitter, the G-Link receiver and the network communication, an embedded CPU system running a variant of Linux was implemented to expedite porting of the legacy controlling software.

E. Porting the control software to the embedded Linux

Porting the control software to the embedded Linux was perhaps the most time consuming part of the work. In the new system the CPU has direct access to both the TTC transmitter and G-Link receiver. That means that transferring instructions and data between the debug software and the TTC transmitter and G-Link receiver should be quite simple. However, since the old hardware was much distributed, the controlling software was far more complex. Removing unnecessary parts from the legacy software thus became the major task. The fact that many collaborators added redundant features to the old software in various places over a long period made porting more complex than necessary. Incomplete documentation also made the process more difficult.

IV. LONG TERM MAINTENANCE

The digitizer system will potentially need to function and be maintained for up to 15 years, so the test system and must be reliable and robust. The ML506 development board could potentially break down at some point during this period. However, the board is commercially available and could easily be replaced with a new one without significant testing and debugging. If the board becomes unavailable after some years it could be replaced with a newer generation, since the necessary portion of the design is written in VHDL and could easily be implemented on a new FPGA. It is expected that the essential functionality (such as high speed links and fiber optics) will still be available. Generating a new embedded system and a Linux system will almost certainly be easier than for the current system.

The PC, of course, cannot be expected to be in use for 15 years. However, running the debug software in a virtual operating system makes it independent from the hardware and the operating system. (Figure 4) Virtualization technology will be maintained in the future by software developers and will almost certainly remain freely available. This eliminates the need for software maintenance from our side, by allowing us to retain the old operating system on any new hardware.

![Debug software running in a virtual environment.](image)

V. SUMMARY

The system is ready and more robust then the legacy system ever was. Important issues about future maintenance have been addressed and solutions found. Design challenges have been solved, although some developments took longer than expected.

Such a test system could be adapted for use in other systems, requiring only some amount of additional software development for the board. Even the hardware could be modified if communication links other than TTC and G-Link were desired.
VI. REFERENCES

[6] Part #: HDMP-1032/1034  (can be found via Google)
The ALICE Level 0 Pixel Trigger Driver Layer

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Abstract

The ALICE[1] Silicon Pixel Detector (SPD) [2] includes 120 detector modules each containing 10 pixel chips. Each pixel chip is capable of generating a FastOR signal indicating the presence of at least one pixel hit in the corresponding 8192 pixel matrix.

The Pixel Trigger (PIT) [3] [4] System has been implemented to process the 1200 Fast-Or signals from the SPD and to provide an input signal to the ALICE Central Trigger Processor (CTP)[5] for the fastest (Level 0) trigger decision within a latency of 800 ns.

Working as a decision criteria for ALICE, the data flow need to be monitored carefully and status information needs to be made available. Therefore the PIT control system required an accurate design of hardware and software solutions to implement a coordinated operation of the PIT and the ALICE systems to which it interfaces.

A driver layer was developed under stringent requirements of robustness and reusability. It qualifies as a general purpose hardware driver for electronic systems. It uses the ALICE Digital Data Link (DDL) [6] front end board (SIU) to communicate with the PIT hardware.

We present here the design, and the implementation of the Pixel Trigger Front End Device (FED) Server [7].

I. The Pixel Trigger Control Hardware

The pixel trigger hardware is composed of a main processing board where 10 mezzanine cards (Optin boards) are plugged. The Optin boards are capable of reading the output of 12 SPD detector modules (Optical Links).

A PCI inspired control bus with transaction acknowledgement and late parity check is used to communicate between all on-board instances.

A DDL was included as the communication medium for the control interface. Commands are received and status information is read back via a bridge between this device and the internal control bus.

A second FPGA on the processing board is dedicated to the slow control, to the system interfaces and to the reconfiguration of the main processing FPGA. Status monitoring and control is implemented via registers in all the programmable devices available in the hardware. Remote programming of the processing FPGA is foreseen: the programming file for a given processing algorithm will be downloaded via the DDL link and the control FPGA to a local SRAM memory and then transferred to the Flash PROM connected to the processing FPGA.

II. The PIT Control System

The Pixel Trigger control system was designed to operate and control the pixel trigger hardware. It takes appropriate corrective actions to maintain the triggering stability and ensure the data quality.

It is composed of two computers: a Linux PC to act as the driver layer of the system using the ALICE Data Acquisition (DAQ) standard hardware equipped with a SIU/DDL module to interface with the PIT electronics, a Windows PC which is the supervision layer of the system running CERN’s standard Supervisory Control and Data Acquisition (SCADA) framework, PVSS II [8].

The PIT control system is part of the ALICE Detector Control System (DCS) [9]. The architecture of the ALICE on-line software is strictly hierarchical. The main systems: DCS, DAQ, CTP and High Level Trigger (HLT) work as autonomous applications. At the highest level of this hierarchy is the Experimental Control System (ECS) [10], which controls all on-line applications.

The global ALICE DCS is partitioned in sub-detectors that are seen as independent control systems integrated in a hierarchical Finite State Machine (FSM) [11].

III. The PIT FED Server

The Pixel trigger FED Server is a software developed to act as the driver layer of the system. It uses a SIU/DDL to
interface with the PIT electronics and it is capable of publishing status information and receiving commands from several computers over the network.

It was developed in C++ to provide an interface to all hardware features and to be the first layer of control of the system displaying the overall trigger status. It can freely access the 19 bit register address space in the hardware monitoring the status registers of the 120 optical links and 1200 FastOR counts and publishes them as DIM services for the supervision PVSS layer and Finite State Machine (FSM) for trigger quality calculation and FastOR tuning.

In addiction it publishes status services for alarm conditions, provides hardware debugging tools and automatic tests on the system ensuring the data quality.

A. Main Libraries Used

![Library Organization Diagram]

The PIT FED server was developed on top of CERN standard libraries using:

**DIM** [12]: Developed at CERN stands for Distributed Information Management System. It provides a network transparent inter-process communication layer. It is used by the PIT FED to publish status information and to receive commands from other computers through the network.

**OCCI** [13]: Oracle C++ Call Interface (OCCI) is a high-performance and comprehensive object-oriented API to access the Oracle databases. It is used by the FED to access the DCS configuration database.

**Log4cpp** [14]: Is a library of C++ classes for flexible logging to files, syslog, IDSA and other destinations. It is modelled after the Log4j Java library, profiting of their API as much as possible. It is used for the extensive logging that exists in all operations of the FED.

**Fec2Rorc** [15]: Developed at CERN, part of the standard ALICE Data Acquisition and Test Environment (DATE) distribution, is a thin wrapper over the RORC driver libraries and is used by the lower level of the software to access the hardware using the DDL/SIU interface.

Figure 2 shows the library organization.

IV. The FED Server Command Structure

The PIT FED server has to work also as one information hub of several ALICE sub-systems. There are 3 instances currently sending commands to the PIT FED server and relying on its status information: the PIT supervision layer for the control and operation of the system, the SPD FED server [16] in order to read status information for FastOR DAC calibration scans and the CTP in order to configure the PIT outputs (TINDET partition [17]). It can perform a wide range of operations: the execution status of these commands have to be available to all of the instances it interfaces with.

So for the PIT FED a command structure was devised to be flexible, capable of receiving a variable number of arguments, to accurately display the status of the execution of all commands and to be capable of dealing with the fact that several instances can send commands at the same time.

A command channel in the PIT FED is composed of a DIM command and 4 status informations brought through DIM services:

- **Command:** DIM command which is a white space separated string containing the command to be executed followed by all its parameters “command arg1 arg2..argN” ex: “write_register 0x18000 0xDEADBEEF”
- **Command Status:** DIM service with a string publishing the execution status of the command, possible values are: “FINISHED”, “EXECUTING”, “FAILED”
- **Command Return:** DIM service, an integer containing the return value of the command if any. If the command would be reading a register this service would contain, after finishing the command, the actual register value.
- **Command ID:** DIM service integer containing an unique id for the current command being executed, useful if several instances send commands at the same time.

V. List Of Published Services

Connecting the PIT hardware to the rest of the world the PIT FED server has to work also as one information hub of the system.

Counters and status registers that are written by the PIT hardware are made available by issuing commands to the PIT FED but data that are relevant to the trigger quality and overall stability of the system need to be constantly monitored and to be forwarded through DIM services as PVSS datapoints that will be used by the supervision layer Finite State Machine (FSM). This is done by monitoring 2 sets of data: status of the links and status of the outputs.

A. Status of the links

There are 3 DIM services per optical link (link required, link status, link locked), making a total of 360 services. The data of these services are refreshed continuously from two set of registers in the Optin Board address space: the link status registers and the link settings register. There is one settings and one status register per optical link (120) in the system.
They are contained inside the Optin board address space. Registers 21 to 32 contain the link status registers and 33 to 44 the settings registers of the 12 optical links of the corresponding Optin board. Figure 3 and 4 show the format of these registers.

Link Required: integer service, 10 bits used for displaying which of the 10 FastOR channels from a link are being used in the trigger logic. It is read from the 10 least significant bits of the settings register, the mask bits, bits 0 to 9, one per FastOR chip. If one bit is enabled it means that the corresponding pixel chip will be excluded from the trigger logic. If all pixel chips are disabled the link is not required.

Link Locked: determines if the internal optical receiver is locked and getting a valid input data stream. It is read from the least significant bit, from the link status register that is forwarded by the deserializer device connected to the optical link receiver in the hardware. If a link is required by the trigger logic and there is no valid input data stream the data taking is stopped.

Link Error: determines if the rates of the FastOR of this channel are within the correct thresholds. In the hardware there are of 40 read/write registers where the maximum and minimum FastOR rates can be set: 20 for the maximum and minimum rates for pixels chips belonging to the inner layer of the SPD and 20 for the maximum and minimum rates for chips belonging to the outer layer. The Optin Board will then automatically count the incoming FastOR signals for a default period of one second and if at least one of the 10 FastOR channels of one link gets out of the thresholds the bit number 2 of the status register will be enabled stating that there is a configuration problem in this SPD halfstave (noise or inefficiency).

B. Status of the outputs

The same logic is applied to the outputs of the system. Status registers and counters of the outputs are read from the processing FPGA address space to the higher level supervision layer in order to detect problems and stop the run if required.

There are 10 services indicating the output mode to the CTP visualized as strings ("normal", "random", "toggle" or "signature"). The different modes are used for debugging of the CTP: normal is the normal triggering mode, in random mode the corresponding output will send a random bit pattern, in toggle mode the output will switch polarity on every trigger and in signature mode the output will send a pre-defined pattern on every trigger. During run mode all outputs have to be in "normal" mode.

10 integer services indicating the current trigger rate of the outputs are foreseen, this will be forwarded to the supervision layer in order to detect abnormalities in the trigger algorithms.

C. FastOR Counters

One big service displays the FastOR count of all chips in the system (1200). Used by the SPD FED and refreshed on demand during FastOR Optimization DAC scans. This service is published due to constraints in performance during FastOR calibration scans. The SPD FED will loop over pixel chip FastOR DACS, set test pulse matrices, send triggers and measure the FastOR rates. Due to the large number of possible steps of this scan (minimum of 4*8 bit DACs, 3 test pulse matrices : \(3*256 = 12.9*10^9\)). The SPD FED will send a command to start the measurements on the PIT FED and retrieve the data in one big array instead of issuing several read counters commands.

VI. Command Line Interface

Using the high level architecture of the FED server allows sending commands directly through a command line interface. This feature is managed by the pit_keyboard class. It uses the “termios.h” and “poll.h” unix C libraries to scan from the keyboard input without stopping the execution loop of the FED server. It is able to perform normal tasks and commands from other sources at the same time while the operator types commands in the PIT FED console.

The command structure is the same as for the DIM commands, feedback of the execution status is available by following one of the log channels of the FED.

The command line interface was extremely useful during the early commissioning phase for testing the hardware features and to perform bit error rate measurements on the system.

VII. The PIT FED Server Implementation

In order to address problems like the long term maintenance, robustness and scalability for the PIT FED server a pure C++ object-oriented paradigm modelling parts of the hardware was chosen. There was a heavy investment in encapsulation where classes provide interfaces hiding hardware related data while providing high level functionalities. C++ exceptions for error management and the Standard Template Library (STL) [18] whenever possible was used. This proved to be an effective way of managing complexity increasing code robustness without hindering performance.
A. Main Classes Developed

1. PIT Communication Class

The pit_comm class is positioned at the lower level of the class architecture. It is used to manage the communication through the DDL. It is a singleton [19] meaning that there is only one instance of the class in the project and its used by almost all other classes in this architecture. It is an object oriented wrapper around Fec2Rorc functions. Status bits are read automatically in all transactions. All data sent to the hardware are read back and verified. Exceptions are thrown if any error is detected.

The PIT communication class summary:
- manages the communication with the hardware
- a wrapper around the Fec2Rorc functions
- checks status bits automatically
- write followed by a read for verification
- one instance used by all hardware classes (singleton)
- throws exceptions on error detection

2. PIT Configuration Class

The pit_configuration class is designed to supply configuration data to all other classes. It manages the access to the oracle database or to configuration files. It is also a singleton having only one instance of this classe in the project supplying services to several other instances/classes.

The PIT configuration class summary:
- manages access to database or to configuration files
- one instance used by all classes (singleton)

3. PIT Driver Top Level Class

The pit_driver class is the higher level instance of all hardware related classes and contains collections of all other driver classes (processing FPGA, control FPGA, Optin boards etc.). It is capable of parsing the commands received from the DIM or from the command line interface and forwards them to the correct instances. This includes bit error rate tests, measurement and realignment of all phases, finding noisy FastOR channels and management of all global operations of the software.

The PIT Driver top level class summary:
- higher instance of the driver class
- has collections of all other driver classes (processing FPGA, control FPGA, Optin boards classes)
- manages commands coming from the different instances
- performs global operations in the system

4. Hardware modelling classes

The pit_driver_ProcFPGA, pit_driver_ControlFpga, pit_driver_OptinBoard, pit_driver_Optical_link and pit_driver_FoChannel are classes that were designed to model the existing hardware devices with the same name. They provide high level methods to access functionalities of the devices they represent hiding the hardware related implementation. They are self contained: they include inside them the means for communicating with the hardware and all memory addresses and information needed to keep track of the status of the device. They can publish status information via DIM services if needed. They are safe, they verify the data and throw exceptions if needed.

For instance the pit_driver_ProcFPGA class offers methods to fully configure the output algorithms of the system, the pit_driver_Optical_link class displays when a link is locked, is required or if it is in error.

PIT driver hardware classes summary:
- they model existing hardware devices with the same name
- they provide high level functionalities hiding memory addresses, registers and hardware related issues
- they are self contained
- they are included inside the pit_driver class
- they are safe: they verify the data and throw exceptions

B. Extension of Existing Frameworks

There was an extension of existing frameworks namely in Log4Cpp::DimAppender and run_time_error::pit_comm_error classes.

In the Log4Cpp framework a logger class can have several appenders and in this way it can write logging information to several destinations: log files, databases or even system specific logs ex: windows event log.

Log4Cpp::DimAppender is an extension of the generic Log4cpp::Appender. It was created through inheritance from the Log4cpp::FormattedAppender class. It publishes logging information to the higher instances that connect to the driver layer through DIM. This framework provides several priority levels for each log message (fatal, error, warning, info, debug etc.) and each appender can be configured to write messages only above a certain level. In that way the driver layer can be configured to be in debug level for the FileAppender object. Then all log messages are written to file, or to be in warning
level for the DimAppender object, displaying only warnings or errors to the operator in the supervision layer.

C. Command Parsing

The pit_driver class was designed to have a common path for the parsing of all commands from any source: the command line interface, DIM commands from the SPD FED server, DIM commands from the supervision layer etc. Like that a standard way of managing all commands with logging information and error handling can be created.

It uses only C++ formatted data input/output mechanisms relying in the istream and ostream inherited classes operators “>>” and “<<” so there is no possibility of buffer overruns while using sscanf or sprintf, increasing the stability and safety of the system.

The commands are seen as “white space” separated strings with a command name and a variable number or arguments. Furthermore the way of identifying instances in the hardware is done only by SPD coordinates: sector, side, channel and not by hardware coordinates, Optin number, channel. This makes the commands more easy to remember and more user friendly.

D. Error Handling

The error handling is a critical part of the development of any project. This software makes an extensive use of C++ exceptions for error handling. A special pit_comm_error class which is an extension of the run_time_error exception was developed. It is used by the system for special error handling of communication errors through the DDL. It allows to automatically reset the SIU on certain types of errors. The verification of the data and the throwing of exceptions in case of errors was left to the lower level classes.

This increases:

- encapsulation: permits a bigger level of abstraction, the higher level instances classes do not need to be aware of the low level implementation of the system
- software flexibility: is easier to replace the lower level classes by other classes
- software scalability: is easy to add new kinds of errors after the initial design of the system
- safety: all errors will be reported and saved the same way. Even some lower level system errors included automatically by the compiler can be caught this way

E. Documentation Generating Tools

During the development of this software an automatic documentation generating tool called Doxygen [20] was used.

Doxygen is a documentation system for several languages including: C++, C, PVSS control scripts, VHDL, Python, Ruby and many more. It is used by a large number of projects, it can easily be integrated in many Integrated Development Environments (IDE) for instance eclipse. It can generate online documentation in HTML, MS-Word rich text format documents, Latex, compressed HTML, PostScript, PDF and Unix man pages. The documentation is extracted directly from the source files through specially defined comments and also by the code structure displaying the relationship between the various elements, dependency graphs, inheritance diagrams and collaboration diagrams which are all generated automatically.

This proved to be very useful to quickly find the way in large source distributions and increased good practices in commenting code and consistence in documentation.

VIII. Conclusions

The PIT FED server was integrated into ALICE DCS and is in stable production phase. It has been running stably without any crash for several months and it performs already many of the high level functions required. In particular the bit error rate measurements on the hardware and the automatic finding of noisy FastOR channels were extremely useful during the early commissioning phase as well as the command line interface.

The highly modular high level class structure proved to increase scalability and robustness, to reduce maintenance issues and does not hinder the performance of the system.

Automatic documentation tools and modern integrated development environments were used during the development phase.

The PIT FED successfully maps all PIT hardware features while publishing the status information for FastOR tuning. It calculates the trigger quality and provides the higher level FSM information to recognize errors conditions.

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Power Distribution in a CMS Tracker for the SLHC

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Abstract

An upgraded tracker for CMS will need a new architecture for powering to keep the power dissipated in the power cables to acceptable levels. Inductor topologies to reduce the stray magnetic field are discussed together with measurements of the magnetic field produced by prototype inductors. A transformer based DC-DC converter has the potential to produce a high step-down ratio whilst producing a low stray field and retaining high efficiency. The relative merits of buck configuration and transformer based DC-DC converters are discussed.

I. INTRODUCTION

A tracker for use in CMS with an upgraded LHC (SLHC) will need finer granularity whilst having the same, or less, dead material[1]. This will imply either the same or less power consumption. This can be achieved by using readout chips with a smaller feature size: the current rises with the increased number of channels but the power consumption stays the same due to the reduced supply voltage. In the current tracker the power dissipated in the low voltage supply cables in comparable with the power dissipated by the active electronics. If the same architecture is retained for an upgraded tracker the dead material will rise significantly, either in terms of thicker cabling or cooling pipes to remove the increased power dissipated in the cabling. A new system architecture is required. The two currently proposed involved the use of serial powering and/or DC-DC converters[2]. Aspects of DC-DC converters using magnetic fields as an energy storage/transfer mechanism are discussed here.

The baseline configuration for a DC-DC converter based scheme is the buck converter. Energy is repeatedly drawn from the input supply stored in the magnetic field generated by an inductor and then liberated to the output. A description of the buck converter and a discussion of the challenges involved in its use in the high radiation, high magnetic field environment of a CMS or Atlas tracker are described elsewhere[3]. Buck converters have the advantage of simplicity and compactness. To be competitive in terms of system efficiency with serial powering approach a DC-DC converter based scheme needs to achieve a step-down ratio between the input and output voltages in the region of ten. To achieve this ratio whilst retaining a high conversion efficiency is challenging in a buck converter where a high step-down ratio implies a high mark-space ratio for the switches. An additional challenge for a DC-DC converter based on magnetic components is electro-magnetic interference (EMI) with the readout chips caused by the time-varying magnetic field generated by the converter.

The EMI produced by a DC-DC converter can be reduced by using an inductor which produces smaller stray field, using a configuration - such as a transformer based design - that produces less stray field, or shielding the magnetic field. The use of a toroidal inductor, a planar transformer and shielding are discussed.

II. TOROIDAL INDUCTOR FABRICATED IN PCB

A toroidal inductor has lower external field than a solenoid of equivalent inductance. It is possible to fabricate a rectangular section toroid in a printed circuit board, following the example of fabricating a toroid in CMOS technology[4]. The inductance of a rectangular toroid of \( N \) turns with inner and outer diameters \( d_i \), \( d_o \) and height \( h \) is approximately \( L \approx (N^2 \mu_0/2\pi) \log(d_o/d_i) \). An inductor with inner and outer radius of 12mm and 28mm respectively was constructed in a standard PCB process of 1.6mm height. Figure 1 shows a photograph of the test inductor. The 30 turn inductor is predicted to have an inductance of 244\( \mu \)H. The measured impedance, at 100kHz was 240 ± 20n\( \Omega \). The DC resistance was measured as 205 ± 20m\( \Omega \). From this it can be seen that constructing an inductor suitable for use in a 1-Amp DC-DC buck converter would be challenging. For such a device an inductance in the region of 500\( n \)H with a DC resistance of much less than 100m\( \Omega \) is needed[5]. By using multiple layers and filled vias an inductor with suitable characteristics could probably be fabricated, but the extra cost and complexity would negate the benefit of the increased integration allowed by building magnetic components into the PCB of the DC-DC converter. However, it would be possible to construct an inductor of lower inductance suitable for use as part of an output filter for a transformer-based design.

Even an ideal toroid produces some external magnetic field. If the the current input and output in the same position it can been seen that in addition to the many turns around the core of the toroid the current undergoes a single turn around the axis perpendicular to the plane of the core. This field can be reduced by either fabricating two toroids on top of each other connected in series to as to cancel the external field or by using a conductive shield. Since the inductor will be fabricated in a board with power and ground planes the latter solution will be implemented in any case.
III. MEASUREMENT OF MAGNETIC FIELD

A variety of inductors were connected to the tracking generator output of a Hewlett Packard HP8560A spectrum analyser and the magnetic field measured using a Hameg HZ530 “near field probe”. The inductor and the field probe were held in a non-conducting support separated by $100 \pm 5\text{mm}$ aligned along the axial direction to within $5^\circ$. Figure 2 shows the arrangement (but not the supports). The field probe has no absolute calibration, but its response is linear and enables comparative measurements to be made.

Figure 3 shows the relative magnetic field as a function of frequency with a variety of inductors. The inductors are driven with a fixed voltage and the sensitivity of the field probe varies strongly with frequency, hence it is not straightforward to calculate the magnetic field as a function of drive current and frequency. However, some conclusions can be drawn. Table 1 gives the measured field strength for three different arrangements of air-core inductor together with the inductance measured by using an inductance bridge. The inductors are Coilcraft 132-19 solenoidal inductors, with nominal inductance 470$nH$. The magnetic field for a single inductor and two inductors mounted side by side with the magnetic field in their core oriented in the same direction are almost the same. This is because the magnetic field per unit current is approximately twice as large as for one coil, but the inductance approximately doubles so the current drops by a factor of two. For two inductors mounted so the the magnetic field from each coil are in opposite direction the magnetic field is a factor of $20dB$ lower, whilst the inductances for the two arrangements are within measurement errors. This indicates that the electromagnetic interference from radiated magnetic fields in a DC-DC converter can be greatly reduced by careful choice of inductor geometry.

Table 1: Inductance and relative magnetic field of air-core solenoids

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Inductance/nH ±10%</th>
<th>Magnetic Field at 20MHz (arb. units)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Coilcraft 132-19</td>
<td>477</td>
<td>-75dB</td>
</tr>
<tr>
<td>Two 132-19, parallel field</td>
<td>940</td>
<td>-75dB</td>
</tr>
<tr>
<td>Two 132-19, anti-parallel field</td>
<td>915</td>
<td>-94dB</td>
</tr>
</tbody>
</table>

IV. TRANSFORMER BASED DC-DC CONVERTER

At high step-down ratios a transformer based DC-DC converter is preferable to a buck configuration. The step down ratio is largely determined by the ratio of the number of turns between the primary and secondary windings. Regulation of the output voltage can be achieved by altering the mark-to-space ratio of the switches driving the primary winding. For resonant converter voltage regulation can be achieved by changing the drive frequency. To increase the degree of integration the transformer can be constructed inside the printed circuit board. It has been
pointed out[6] that an advantage of a transformer based converter is that almost all the magnetic field generated by the primary winding is cancelled out by the secondary. The low external field also implies that the transformer can be screened without significantly affecting its operation. A schematic showing a transformer based DC-DC converter is shown in 4. In practice the rectifying diodes would be replaced by a synchronous rectifier. The schematic is taken from the data sheet of a commercial component[7] intended to enable the construction of low-noise DC-DC converters. A differential output noise of less than $10\mu$V RMS is claimed for the example circuit.

The characteristics of a planar transformer were simulated and a prototype constructed. With the Figure 5 shows the prototype transformer constructed. The transformer has a 4:1 windings ratio and is constructed as an eight layer printed circuit board with $30\mu$m copper foil separated by $50\mu$m dielectric. The outer diameter is $28\text{mm}$. The magnetic field produced was simulated under a variety of different conditions. Figure 6 shows the field lines when the primary coil was energized with $0.25A$ and the secondary coil left open. Figure 7 shows the field lines with the primary energized with $0.25A$ and the secondary with $1A$. It can be seen that the external field is greatly reduced. Figure 8 shows the field density for a transformer with the primary and secondary energized and shielded with $35\mu$m of copper foil at a distance of $200\mu$m from the outer windings. The field is reduced still further. Table 2 lists the magnetic field predicted at $10\text{cm}$ in an axial direction from the centre of the transformer. Even with copper shielding foils only $200\mu$m from the outer layers of the transformer the power dissipated in the shield is predicted to be only $2.8\text{mW}$ with $250mA/1A$ in the primary/secondary windings.

![Figure 4: Sketch of transformer based DC-DC converter](image)

![Figure 5: Photograph of prototype planar transformer](image)

![Figure 6: Magnetic field lines from a planar transformer with only primary energized](image)

![Figure 7: Magnetic field lines from planar transformer with both primary and secondary energized](image)

![Figure 8: Magnetic field density from planar transformer with primary and secondary energized with 0.25A, 1A. Shielded at a distance of 200µm.](image)

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Magnetic Field at 10cm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary energized with 250mA</td>
<td>$28\text{nT}$</td>
</tr>
<tr>
<td>Primary/secondary energized with 250mA/ -1A</td>
<td>$12\text{nT}$</td>
</tr>
<tr>
<td>Primary/secondary energized with 250mA/-1A, Screened at 200µm</td>
<td>$60\text{pT}$</td>
</tr>
</tbody>
</table>

Table 2: Magnetic field produced by planar transformer

V. Module Test Stand

A test-stand based in the ARC test-system[8] for tracker modules is being constructed in order to test experimentally noise pick-up in a tracker module. In addition a system for measuring the common and differential mode conducted electrical noise, similar to those set up in CERN and Aachen[9] is being set up. This will allow the noise produced by a prototype DC-DC converter to be measured and also its effect on a CMS tracker module. The physical arrangement of the module test-stand is shown in figure 9.
VI. DISCUSSION

Powering a CMS tracker at the SLHC will require a powering scheme that can supply electrical power at a higher voltage and hence lower current than the supply for the front-end electrical circuitry. The relative merits of a system based on serial powering or DC-DC converters are discussed elsewhere[2]. Within the family of DC-DC converters based on magnetic fields for energy transfer, transformer-based converters have the possibility for a higher step-down ratio and lower EMI than a buck configuration. However, system issues such as simplicity and compactness may override these factors.

VII. ACKNOWLEDGEMENTS

The authors would like to thank Brian Hawes for providing us with planar transformer prototypes and simulations. We are also grateful to the University of California Santa Barbara for providing us with the components needed to construct a module test-stand.

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FPGA Implementation of Optimal Filtering Algorithm for TileCal ROD System

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Abstract

Traditionally, Optimal Filtering Algorithm has been implemented using general purpose programmable DSP chips. Alternatively, new FPGAs provide a highly adaptable and flexible system to develop this algorithm. TileCal ROD is a multi-channel system, where similar data arrives at very high sampling rates and is subject to simultaneous tasks. It include different FPGAs with high I/O and with parallel structures that provide a benefit at a data analysis.

The Optical Multiplexer Board is one of the elements presents in TileCal ROD System. It has FPGAs devices that present an ideal platform for implementing Optimal Filtering Algorithm. Actually this algorithm is performing in the DSPs included at ROD Motherboard. This work presents an alternative to implement Optimal Filtering Algorithm.

I. INTRODUCTION

TileCal [1] is the hadronic tile calorimeter of the ATLAS-LHC [2] experiment and consists in terms of electronic readout of roughly 10000 channels read each 25 ns. Data gathered from these channels are digitized and transmitted to the Data Acquisition System (DAQ) following a three level trigger system.

The main component of the back-end electronics of the TileCal sub-detector is the Read-Out Driver (ROD) [3], which is placed between the first and the second level trigger. The ROD has to pre-process and gather data coming from the Front End Boards (FEB) and send these data to the Read-Out Buffers (ROB) in the second level trigger.

II. OPTIMAL FILTERING ALGORITHM

The Optimal Filtering (OF) algorithm reconstructs the amplitude and phase of a digitized signal by a linear combination of its digitized samples, pedestal subtracted.

\[ A = \sum_{i=1}^{n} a_i (S_i - p) \]  

\[ \tau = \frac{1}{A} \sum_{i=1}^{n} b_i (S_i - p) \]  

\[ \chi = \frac{1}{A} \sum_{i=1}^{n} |(S_i - p) - A g_i| \]  

where \( S_i \) represents the digital sample \( i \) and \( n \) is the total number of samples. The number of samples is 7 for physics and 9 for calibration runs [5]. We define the pedestal, \( p \), as the baseline of the signal. The amplitude, \( A \), is the height of the signal measured from the pedestal, \( \tau \), is the phase and it is defined as the time between the central sample and the peak of the pulse (Fig. 3).
The weights, $a_i$ and $b_i$, are obtained from the pulse shape of the photomultipliers and the noise autocorrelation matrix, $g_i$. Determine correctly weights minimize the effect of the noise in the amplitude and phase reconstruction [6].

DSP has to compute energy, phase and Quality Factor (QF) for all the channels in less than 10 us at the ATLAS maximum rate and send the reconstructed data to the second trigger level.

III. OPTIMAL FILTERING DEVELOPMENT

Traditionally, digital signal processing (DSP) algorithms are implemented using general-purpose (programmable) DSP chips for low-rate applications, or special-purpose (fixed function) DSP chip-sets and application-specific integrated circuits (ASICs) for higher rates.

Advancements in Field Programmable Gate Arrays (FPGAs) provide new options for DSP design engineers. The FPGA maintains the advantages of custom functionality like an ASIC while avoiding the high development costs and the inability to make design modifications after production. The FPGA also adds design flexibility and adaptability with optimal device utilization while conserving both board space and system power, which is often not the case with DSP chips.

In some high-performance signal processing applications, FPGAs have several significant advantages over high-end DSP processors. FPGAs can take advantage of their highly parallel architectures and offer much higher throughput than DSPs. As a result, FPGAs overall energy consumpation may be significantly lower than that of DSP processors.

This paper presents a comparative between OF in DSP and OF in FPGAs.

A. OF in DSPs

Processing Units of the TileCal ROD have two Texas Instruments TMS320C6414 DSPs which provide an instruction cycle frequency of 720 MHz, 1024KB of user memory and an interrupt latency of 900ns. Each ROD DSP has to compute the data coming from two TileCal modules, i.e. two times 48 channels.

The Energy, Phase and Quality Factor is computed sequentially and the ROD DSP takes 8us to compute these three magnitudes for 96 channels. In addition, the DSP has to synchronize and to format the data.

The DSP performance was also tested at high event rate during the production tests [7]. The maximum Level 1 event rate can not be achieved in copy mode due to the ROD output data bandwidth limitations and in OF mode due to the OF algorithm processing time, which is 23 µs is the current DSP version. It is expect to reduce the processing time to under 10 µs by using OF without iterations and an optimized programming of the reconstruction algorithms in assembler.
B. OF in FPGAs

Another performance improvement is the ability to separate the data stream into multiple parallel blocks of data which have limited interdependence. Each data block can then be operated on independently, and the results combined, resulting in higher relative performance. Taking advantage of any architectural opportunity for maximizing the number or speed of operations is essential to maximizing the performance achievable within an FPGA [8].

In FPGAs we can generate OF Algorithm by using two methods, VHDL Blocks and Embedded DSPs. VHDL method uses separate multiplier and accumulator.

![Figure 7: OF in FPGAs with VHDL Blocks.](image)

Embedded DSP method uses hardware blocks incluyes in FPGA.

![Figure 8: OF in FPGAs with Embedded DSP Blocks.](image)

With VHDL Method we need 81 Slices and a maximum frequency of 116 MHz. With Embedded DSPs we need 25 Slices and 168 MHz. Optimal Filtering in FPGA is faster than DSPs.

IV. CONCLUSION

The work presented has been developed as a technology comparison between Digital Signal Processor used in TileCal RODs and new low cost FPGAs for signal processing application. The results show FPGA signal processing 100 times faster than DSPs. These results might be used in the TileCal Optical Multiplexer Boards mezzanine Processing Units if a more precise or complex reconstruction algorithm is required during the TileCal life.

V. REFERENCES

An Optical Demo-Link for ATLAS Inner Detector Readout Upgrade

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Abstract

The GOL ASIC is a serializer chip developed by CERN based on a 0.25 μm CMOS technology [1]. The GOL operates with two data rates: 800 Mbps and 1.6 Gbps. This ASIC has been evaluated with radiation tolerance requirement for the ATLAS Inner Detector upgrade for the SLHC1. A demo-link has been designed and constructed to read out silicon detectors in the test staves through fiber optics. Through this demo-link we plan to study system issues in a giga-bit optical link. This concept will be extended to future serializer ASICs like the GBTx and the LOC when they become available. Experience gained from these demo-links will help us design and build a reliable optical readout system for new ATLAS Inner Detector readout.

I. INTRODUCTION

R&D activities for ATLAS Inner Detector upgrade, especially its B-layer replacement, have taken place for several years. On the detector side, a stave concept has taken shape. A stave is a mechanical structure on which the silicon sensors and front-end readout ASICs (called the hybrid module) are placed. The stave provides support to services like power supplies and cooling tubes. The stave also is a natural unit to gather data from the hybrid modules, process and serialize them and send the data off the detector to the back-end electronics through optical fibers.

Together with the development of new silicon sensors for the upgrade, new front-end readout ASICs are being developed with newer technologies to meet new requirements. With these developments, a new front-end readout system is in discussion. In this system an optical link with a data rate at multi-giga-bit per second is proposed to meet new demands. All developments for the front-end readout electronics need to meet the radiation tolerance requirements for the ATLAS Inner Detector at the SLHC. This includes the transmitting part of the optical links.

Giga-bit range serial data transmission has its own specific issues. Many of these issues were discovered and addressed in the present optical links like the one for ATLAS Liquid Argon calorimeter front-end readout. Lessons have been learned from those exercises and are documented [2]. In the new optical readout for the Inner Detector upgrade, we propose the demo-link concept to develop the optical link together with not only the ASICs (GBTx, LOC) and subsystems (the Versatile Link) for the optical link itself, but also the detector’s other front-end readout ASICs. This way we can understand issues in the link, in integration, installation and system reliability at early stages so that actions can be taken to address them. With this, we hope to have a high quality, reliable optical link for the ATLAS Inner Detector upgrade.

There are two ASIC developments (GBTx and LOC) to meet the new data rate and radiation tolerance requirements for the upgrade. These ASICs are not yet available for system development. The presently available ASIC in giga-bit data rate range is the GOL chip which has been verified for applications in LHC. We verified it to the SLHC radiation tolerance requirements and started the first demo-link with this ASIC. We are prepared to move to the GBTx and LOC ASICs when they become available.

In this note, we report the irradiation test results on the GOL ASIC in section II. In section III the GOL based demo-link is described. The integration of this demo-link with stave-06 is reported. In section IV, we outline the design consideration for the GBTx and LOC based demo-link. It will be this demo-link that will lead to the baseline design of the optical link for the ATLAS Inner Detector readout upgrade. Conclusions and acknowledgements are in section V.

II. IRRADIATION TESTS ON THE GOL ASIC

The GOL ASIC has been qualified for applications in the LHC radiation environment [3]. We irradiated two of the GOL chips with a 230 MeV proton beam and find that this chip may be used in the SLHC radiation environment. Detailed test results have been reported elsewhere [4]. Here we summarize the characteristics of the GOL chip before and after the irradiation (total ionization dose effect) and the single event effect measurement results.

A. The total ionization dose effect

The eye diagrams of the serial output of the GOL before and after the irradiation are shown in Figure 1. There is no change in rise/fall times of the waveforms. The amplitude decreases from 350 mV to 300 mV. The eye opening easily pass 1.6Gbps eye mask test adopted from the Gigabit Ethernet standard.

1 The work reported in this note is supported by the US-ATLAS for the high luminosity upgrade of the LHC.
Jitter measurements were performed before and after the irradiation and are summarised in Table 1. The radiation effect on the jitter components is minimal.

Table 1: Measurement on the GOL jitter components before and after the irradiation

<table>
<thead>
<tr>
<th>Jitter Component</th>
<th>Clock (ps)</th>
<th>Before (ps)</th>
<th>After (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Random (RMS)</td>
<td>8.6</td>
<td>8.8</td>
<td>9.9</td>
</tr>
<tr>
<td>Deterministic (pk-pk)</td>
<td>10.8</td>
<td>112.5</td>
<td>96.6</td>
</tr>
<tr>
<td>Total at BER &lt; 1E-12</td>
<td>127.7</td>
<td>208.6</td>
<td>205.2</td>
</tr>
</tbody>
</table>

Jitter transfer function of the GOL chip is shown in Figure 2. After the irradiation, low frequency jitter is more suppressed, while jitter frequency at around 1 MHz is slightly enhanced.

B. Single event effect

Two types of single event effects were measured during the irradiation with 230 MeV protons: data bit corruption that does not bring down the link synchronization and the event that cause the link to lose synchronization hence a re-synch was needed to establish the serial data transmission.

Table 2: Single event effect measurement a GOL-TLK link system with the GOL under proton irradiation.

<table>
<thead>
<tr>
<th>SEE Type</th>
<th>Cross Section (cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Loss of synch</td>
<td>&lt; (2.5±0.6)×10⁻¹³</td>
</tr>
<tr>
<td>Bit corruption</td>
<td>&lt; (5.3±2.6)×10⁻¹⁴</td>
</tr>
</tbody>
</table>

In conclusion, the GOL ASIC is suitable for optical link system development for applications in the SLHC.

III. THE GOL BASED DEMO-LINK

Since the GOL is the only serializer chip that has been evaluated and verified to be radiation tolerant for applications in SLHC, we decided to start our demo-link with this ASIC. In this section we report on this demo-link and its integration with the stave-06 at the LBNL.

A. The demo-link design and test

Shown in Figure 4 is the block diagram of the GOL based demo-link. We employ a four board system so that the two interface boards are simple and can be easily re-designed and constructed to meet the requirements of different stave configurations. As a matter of matter, we are designing new interface boards to read out the stave-07.
New front-end electronics systems for the SLHC must
withstand higher radiations. The data transmission must meet
with higher data rate requirements. New radiation tolerant
ASICs are being development to meet the new demands.
There are two ASIC developments for optical links: the GBT
and the LOC. Please see reports on the GBT in TWEPP
2007, LOT in this conference. The ser-des part of the GBT is
called the GBTx. The LOC is only a serializer chip. Both
ASICs couple to the Versatile Link, and operates at a serial
data rate around 5 Gbps. The block diagram of the GBTx and
LOC based demo-link is shown in Figure 7. In this design,
we make use of the Reference Link project [?] which is
currently under development as a common project between
ATLAS and CMS for the SLHC upgrade. The Reference
Link is FPGA based, with the ser-des function realized with
the embedded ser-des in the FPGAs. By the time when the
GBTx and the LOC are available, we anticipate that prices
for the ser-des embedded FPGAs would fall into reach in one
year’s time.

The choice of the TLK2500 as the deserializer is based on
past experience with this commercially available chip, and
for economical reasons. TLK2500 is a serializer-deserializer
(ser-des) chip produced by Texas Instrument. This ser-des
has a data rate up to 2.5 Gbps, matches perfectly with the
GOL. Embedded ser-des in FPGAs are much more expensive
than TLK2500 and are reserved for the GBTx and LOC
based demo-links that operate at higher speeds. Shown in
Figure 5 is a picture of the GOL based demo-link. The optical
interface is chosen to be SFP+ format. This is the standard
chosen by the Versatile Link project. Please see reports on
the Versatile Link in the joint ATLAS-CMS opto-electronics
working group session in this conference. Shown in Figure 6
is the optical eye diagram.
GOL

Interface

SFP+/VL

Signal
from
stave

fibe

SFP+/VL

Signal
to test
station

fibe

TLK

Detector
Stave +
FE ASICs

Interface to
Front-end
ASICs

GBTx or
LOC + V.L.

Interface

Figure 5: Picture of the GOL-TLK demo-link.

V.L. +
Ref.Link

Interface to
Back-end
electronics

Back-end
Electronics

Demo-link
Figure 7: The GBTx or LOC demo-link block diagram. In this
design, common projects such as the Versatile Link and the
Reference Link are incorporated to minimize the R&D efforts.

V. CONCLUSIONS AND AKNOWLEDEMENTS

Figure 6: Optical eye diagram of measured from the GOL-TLK
demo-link.

The GOL based demo-link has been constructed and
system level studies are being carried out with silicon
detector and its front-end readout ASICs (the stave). The next
generation of the demo-links will be based on the GBTx and
the LOC, both currently under development. In this new
demo-links, developments from common projects such as the
Versatile Link and the Reference Link will be incorporated to
minimized R&D efforts.

Bit error rate of this demo-link was measured in lab to be
better than 1E-14 before we carried out the integration test
with the stave-6.

B. The integration with the stave-06
The stave -06 is a prototype stave with 6 hybrid modules.
The present ATLAS Inner Detector front-end readout ASICs
are used to readout the silicon sensors. The GOL based
demo-link was successfully integrated between the stave-06
and its readout test stand (functions as the back-end
electronics). Although digital data was transmitted correctly,
we discovered noise issues due to the introduction of this
high speed serial data link. This issue has been investigated
and will be corrected in the new interface board for the stave07. This illustrates the importance of the demo-link. More
system tests are in line with this demo-link until the faster
GBTx and LOC based demo-links are available.

We would like to thank the US-ATLAS program which
provides funds for this R&D effort. We also would like to
thank many of our colleges who have been helping us in
defining, designing, construction and testing of this demolink. Particularly we would like to thank Vataliy Fadeyev and
Jason Nelson from SCIPP, Carl Habor from LBNL, P.K.Teng
and Suen Hou from IPAS in helping us in the demo-link
efforts. We would like to thank Jim Kierstead at BNL and
Ethan Cascio at MGH’s NPTC for their help in irradiation
tests.

VI. REFERENCES
IV. DESIGN CONSIDERATIONS FOR GBTX AND LOC
BASED DEMO-LINK

Marchioro and J. Christiansen, "G-Link and Gigabit
Ethernet compliant serializer for LHC data transmission,

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Detector noise susceptibility issues for the future generation of High Energy Physics Experiments

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Abstract
The front-end electronics (FEE) noise characterization to electromagnetic interference and the compatibility of the different subsystems are important topics to consider for the LHC calorimeter upgrades. A new power distribution scheme based on switching power converters is under study and will define a noticeable noise source very close to the detector’s FEE. Knowledge and experience with both FEE noise and electromagnetic compatibility (EMC) issues from previous detectors are important conditions to guarantee the design goals and the good functionality of the upgraded LHC detectors. This paper shows an overview of the noise susceptibility studies performed in different CMS sub-detectors. The impact of different FEE topologies in the final susceptibility to electromagnetic interference of the subsystem is analyzed and design recommendations are presented to increase the EMC of the detectors to the future challenging power distribution topologies.

I. INTRODUCTION

Electromagnetic interference (EMI) has been a major concern [1] during the integration of the CMS experiments. Grounding and shielding problems and electromagnetic compatibility (EMC) issues have arisen during the integration of the LHC calorimeters in different sub-detectors requiring time and important number of tests and studies to solve them. The efforts to find both the root cause and the solution to these problems can be minimized, if no eliminated, performing noise susceptibility studies during the design and the prototype stage of the FEE.

In general, almost all the EMC problems with HEP detectors are associated with interference generated by the power supplies and auxiliary equipment and coupled to the detector through the power distribution and slow control cables, respectively. Interference and noise currents penetrating the detector system propagates through the distribution cables and boards within the detector, interfering through conductive or near-field coupling with the sensitive areas of the FEE reducing its signal-to-noise ratio. Although a big effort is put to reduce the noise emission in switching power converters, the levels achieved have to be directly compatible with the noise levels defined by signal-to-noise in the HEP detectors [2]. The intrinsic FEE topology and the detector integration set the final noise level compatible with the signal to be processed by the system.

The noise sensitivity of the front-end electronics to EMI can be either evaluated earlier during the design via modelling and simulation [3] of the system or measured on prototypes [4]. In the first case, corrective actions can be taken during the design stage, whereas in the second case, it is possible to identify critical elements and inappropriate layouts in prototypes that are responsible for the performance degradation of the FEE. To define the immunity level of the FEE to conductive disturbances, several tests [5] are conducted by injecting currents through the FEE input power terminals and slow control cables. The goal of these tests is two-fold: firstly, the test will characterize the immunity of the system to RF perturbations defining weak points in the design and second, it will provide data to define the emission level to be imposed to the switching power supply and auxiliary equipment connected to them.

This paper presents the characterization of the FEE sensitivity of different CMS subsystems to common mode currents flowing through the power distribution and slow control cables. Based on the results of studies and tests conducted on different CMS subsystems, the impact of the front-end electronics topology, the detector-FEE connection, the power distribution board design, CM filtering and the FEE grounding connection on the FEE susceptibility to interferences is presented. Noise immunity tests and numerical simulations have been used to evaluate the FEE susceptibility to define the weakest areas in the design and to quantify the effect of external EMI in the system. Based on these analysis and measurements, design recommendations are presented to increase the robustness of the system to EMI in view of the future challenging power distribution topologies proposed for the LHC detector upgrades.

II. IMPACT OF ELECTROMAGNETIC INTERFERENCE ON FEE

The design of Application Specific Integrated Circuits (ASIC) to process the signal generated by the detectors allows more specific functions being integrated and located near the detector. It simplifies the front-end electronic design reducing the connection path between the detector and the electronics input, digitizing the signal at the front-end and transmitting the pre-processed data to the counting room via optical fibre. It allowed, for the LHC CMS calorimeter, processing signals with a bandwidth of 40MHz and transmitting the data from the detector to the counting room, located 120m away. Based
on that topology, the front-end electronics can be considered as an isolated system with the only galvanic connection to the external part of the calorimeter through the power distribution and slow control network.

The minimum signal that the front-end electronics can process is determined by the noise level coupled to the system. In addition to the intrinsic thermal noise perturbing the input stages of the FEE, electromagnetic interferences degrade the noise performance of the system. Fig.1 shows the coupling paths for both conductive noise and EMI perturbing a generic part of the calorimeter. Electromagnetic Interference and noise currents generated by power supplies and auxiliary equipment flow into the FEE-Detector unit through the power and slow control cables. Within the FEE-Detector unit, the external perturbing currents couple the EMI to the FEE via conductive and near-field paths. These mechanisms are dominant in the noise coupling because of the bandwidth associated with the front-end electronics and the dimensions of the sensitive processing areas of the detector.

The total noise defines the minimum level for the signal that can be processed by the FEE. The FEE-Detector design goal focuses on minimizing the thermal noise and characterizing and reducing the effects of the EMI contributions. Assuming independence in the perturbations and using $\|n\|_2$ to quantify the overall noise contribution, a criterion usually followed in HEP designs to define the magnitude of the minimum signal processed $\min(s_{\text{sp}})$ is:

$$\min(s_{\text{sp}}) = \min(s_{\text{sp}}) \gg 1,$$

forcing in the design $\|n_{\text{F-D}}\|_2^2 \|n_{\text{F-E}}\|_2^2 \ll \|n_{\text{TH}}\|_2^2$.

This relationship has to be enforced and tested during the front-end electronic design and the integration of the FEE-Detector unit to ensure the good performance of the system. It involves not only the careful design of the coupling between the Detector and the FEE, to minimize $n_{\text{F-D}}(t)$, but also the proper design of the power distribution and slow control cables and shielding to reduce $n_{\text{F-E}}(t)$.

### III. EM CHARACTERIZATION OF THE FEE

The goal of the EM noise characterization of the FEE is to quantify the terms $n_{\text{F-D}}(t)$ and $n_{\text{F-E}}(t)$, and systematically define critical elements in the design that can help to minimize those terms. This characterization of the FEE can be achieved via immunity tests on prototypes or via numerical simulations. The main objective of these EMC tests is to define the immunity of the FEE to electromagnetic interferences.

- Immunity tests consist on injecting a perturbing sine-wave signal $i_{\text{pert}}(t)$ to the front-end electronics at different amplitude and frequency and measuring the output signal $v_{\text{out}}(t)$ of the FEE by its own acquisition system to evaluate the performance of the FEE.
- Numerical simulations using mathematical models of the FEE-Detector have been carried out during the design stage of several subsystems. EMI coupling to critical parts of the FEE have been modelled using Multi-conductor Transmission line Theory (MTL).

$$i_{\text{pert}}(t) \rightarrow \text{FEE} \rightarrow V_{\text{out}}(t)$$

The immunity tests and numerical simulation results may be used to characterize:

1. Noise distribution among channels in the FEE
2. Frequency response of the FEE to EM noise.
   - Estimate the transfer function $TF(\omega)$ between the interference $I_{\text{pert}}(\omega)$ and the FEE output voltage $V_{\text{out}}(\omega)$.
   - Define the coupling mechanism between the electromagnetic interference and the FEE.
   - Define the level of output noise emission of power supplies compatible with the FEE.
The analysis of the FEE immunity corresponding to different CMS front-end electronics respect to the grounding connection, filter implementation, cable and shield connections, FEE-Detector connections and PCB designs are analyzed.

IV. FEE-DETECTOR CONNECTION

This section analyses the sensitivity of the FEE-Detector connection due to common mode (CM) currents flowing through the power cable of the CMS HCAL & Pre-shower front-end electronics. For that purpose a noise injection test is carried out. The idea of the test is to inject a sinusoidal CM current to the FEE through the power supply cables and evaluate the FEE performance using their own acquisition system. The frequency of the perturbing signal is changed to analyze the sensitivity at different frequencies and the amplitude of the signal is set just that the total noise is slightly higher than the thermal noise. The responses of different channels of the front-end electronics are depicted in Fig. 3 for the CMS HCAL prototype and in Fig. 4 for the CMS FEE Pre-shower prototype. The first figure depicts the digitised RMS value of the QIE amplifier output voltages for 12 channels when perturbing currents of 6 mA RMS at 5 MHz and 10 MHz are injected. Fig. 4 shows the digitised RMS value of the amplifier output voltages for all channels when a perturbing current of 9 mA RMS at 8 MHz is injected. In both cases, these values are compared with the output voltage noise of each channel when no perturbation is injected (Reference).

The main result of this test is that the injected perturbation does not distribute equally across all channels. For both the HCAL and Pre-shower prototypes, the non uniformity of noise is generated by slight differences in the connection between the input amplifier and the detector. For future designs, special attention should be paid in planning the FEE-Detector connection with similar common signal paths to equally distribute the noise current to all the FEE channels, avoiding ‘critical paths’ or ‘sensitive channels’

V. FEE RESPONSE: FREQUENCY-GAIN

Other important aspect that has big impact in the performance of the experiment is the frequency response of the FEE to electromagnetic interferences. This response can be obtained from the transfer function measured by the noise injection test and define the susceptibility of the FEE to noise currents. Figs. 5 and 6 show the measured and estimated transfer functions for End-Cap Tracker (TEC) and Pre-shower FEE when CM currents are injected through the power cables. Fig. 5 shows TEC TF for the two operation modes of the APV (PK & DEC) [6] and Fig. 6 the Pre-shower TF for two different gains of the PACE chip (LG & HG). From these pictures, the FEE is more sensitive to high frequency noise than to low frequency noise due to coupling network. This coupling network is defined mainly by parasitic impedances linking the power cables and the FEE-Detector connections.
Additionally, it is important to remark that the sensitivity of the FEE is different for the two operation modes of the chip.

VI. GROUNDING CONNECTIONS EFFECTS

The grounding of the FEE is important to ensure the correct performance of the FEE. The grounding has to be designed to:

1. To minimize capacitive coupling between the structure and the sensitive areas of the FEE $(n_F, D_i(t))$.

2. To create low impedance at the input of the power connector (in DM and CM) to avoid the external current interference flowing inside FEE electronics.

The implementation of these concepts and the way that they are implemented have important implications in the FEE immunity. As example, to show the effect of the FEE GND connection in the sensitivity of the FEE to CM currents, this section studies different methods of implementing the ground connection of the HCAL input power filter. The effects of the length and routing of the ground connection has been evaluated via CM current injection test. Fig. 7 shows the connection under study.

During the test, the strap connection between the filter box and the read-out box (RBX), holding the HCAL electronics, is changed to study their influence on the FEE performance. This connection is made with a 15 cm long copper strap. The length and the routing of the strap connection to the RBX are changed. This modification produces a variation on the inductance of the ground connection. The results of three different layouts are presented.

• GND 1: The ground connection is done with a long strap. It is routed to the connection point as far as possible from the metallic structure of the RBX.

• GND 2: The second layout, the strap is routed to the connection point as close as possible to the metallic structure of the RBX following the shortest path to that point.

• GND 3: The third layout is similar to the second one, but a copper tape is used to fix the strap to the RBX (Fig. 7). This layout decreases the length of the strap to a minimum.

Figure 8 depicts the transfer function for the three configurations that have been studied. Results show the FEE susceptibility to CM currents for three different types of ground connections. Based on these curves, the third layout (GND 3) is the best configuration to make the ground connection of the shield. Essentially this connection is characterized by the shortest and less inductive strap and produces the lowest value of ground impedance connection for the frequency range of interest. The system presents a higher rejection to shield currents because most of these currents can be by-passed from the RBX and hence they do not pass through the sensitive part of the FEE.

For future designs, it is important to consider that the ground connection plays an important role in the FEE immunity. It defines the impedance between the FEE and the ground, setting the level of noise current that is capable of flowing inside the FEE metallic box. Based on this study, it is possible to define the main characteristics that should be followed for the ground connections:

• They should be short and flat.

• Routing path should be as close as possible to the metallic box.

VII. FEE TOPOLOGY - UNBALANCES

The front-end electronics of the HCAL Forward Calorimeter (HF) is composed by photo-multipliers (PMT) located about 4 mts. from the sensitive amplifiers. This section studies the signal connection between each PMT and the respective amplifier to provide enough common mode rejection to avoid amplification of spurious signal due to the remote connection between grounds. The wide-band amplifiers used in the detector (QIE [7]) are very sensitive and the noise tolerated in the detector is just above the intrinsic thermal noise of the amplifier. The common mode rejection of the differential topology has been studied considering the circuit depicted in Fig. 9. The study is based on numerical simulation and the signal cables are modelled using Multi-conductor Transmission Line theory (MTL).

The influence of unbalances generated by the connection between the photodiodes and the FEE located 4 meters away is studied. Fig. 10 shows the common mode rejection to radiation noise of the HF FEE. It shows the performance of the HCAL FEE is decreased more by the different position of the cables on the cable tray than the capacitance unbalance of the photodiodes when the system is affected by electromagnetic radiated noise.
It is important to consider for future designs that unbalances in the input signal circuit strongly increase the FEE noise susceptibility to EMI. The selection of specific components and the topology help to decrease unbalance effects. In this particular case, the HF immunity was improved by selecting a double twisted pair cable with a single braided shield.

VIII. FILTER IMPLEMENTATIONS

The noise emissions in HEP experiments are mainly dominated by the CM currents generated by switching DC-DC converters or by the radiated noise coupled to power cables. The CM current spectrum contains large amount of harmonic components from a few kHz up to hundreds of MHz. In general, this noise is difficult to cancel and may decrease signal-to-noise ratio of the FEE. The noise performance of the experiment can be improved either decreasing the impact of the environment noise (reducing the noise emitted by power supplies by installing filters at the output of the units or using shielded power cables) or increasing the FEE immunity by installing CM filters at the input power terminals of the FEE. CM filters protect the FEE from CM currents flowing through the power cables. A set of immunity tests have been carried out in CMS Tracker and HCAL FEE to evaluate the performance of CM filters installed at the input power terminals of the FEE.

Figure 11 depicts the sensitivity function of the HCAL FEE to common mode current flowing through the power cables, while Fig. 12 depicts the same function for the End-Cap Tracker (TEC). Those plots compare the immunity in case the FEE includes or not a CM filter at its input power terminals. The HCAL FEE without CM filter is about 14dB more sensitive than the FEE with filter and for TEC the results depicted in Fig. 11 shows a general improvement between 12-30 dB, when a filter is installed at the input power terminals. The filter has been implemented with 3 surface mount capacitors of 1µF.

IX. FEE SYSTEM DESIGNS

This section analyzes the performance of different CMS tracker subsystems. All tracker subsystems are configured using the same FEE electronics: silicon micro-strip detector, the APV-25 amplifier and the optical driver. These devices are integrated following different geometries depending upon the location in the Tracker (TIB, TOB or TEC).

Part of the tests performed on the CMS tracker consisted in CM noise injection through the power cable. The subsystems measured were the Tracker Outer Barrel (TOB) and the Tracker End Cap (TEC). Fig. 13 shows the immunity function to CM noise currents of TEC and TOB FEE setting.
the APV in peak mode. The immunity of TEC system is much higher than the TOB immunity to CM currents flowing into the FEE through the power cable. Despite that both subsystems use the same basic electronic devices; there is a large difference in the interference rejection. The main difference in both designs is the power distribution within the FEE through the interconnection board (ICB). The TEC subsystem includes a ground plane in the ICB that shields the EM fields generated by power currents. This EMI is coupled by near-field to the strip detector. The TOB ICB design does not include that shielding.

Routing the power distribution and slow control signal within the subsystem using proper shielding has a strong impact in the FEE susceptibility. A ground plane in the ICB design helps to decrease the length of ground connections and confine within the board the EM fields generated by the DC power distribution. These considerations in the ICB design improve the immunity of the FEE.

X. SLHC IMPLICATIONS

Up-grades for the central detector in both the CMS and the Atlas experiments require defining new schemes for the DC power distribution. The power schemes proposed can be grouped into: Serial Power Distribution System and DC-DC switching power converters. Both schemes have advantages and disadvantages, but the viability of each of them will be closely associated to the FEE design.

- DC-DC switching power converter based: Aspects like CM noise and radiated noise are very important. It is important to pay attention to power distribution boards, ground planes and CM filters to ensure the compatibility between FEE and power system.
- Serial power Distribution System: Noise aspects (CM and radiated noise) associated to the Detector-FEE connection will be crucial to guarantee good performance due to the lack of global ground.

In both cases, it will be crucial to conduct EMC studies to be able to improve the noise immunity of the front-end electronics to be compatible with the noise emitted by the power converters. The compatibility between PS and FEE can only be achieved minimizing both the radiated and conducted noise emitted by the power supplies and the sensitivity of the FEE to EM noise.

XI. CONCLUSIONS

EMC studies based on numerical simulations and tests have been conducted on prototypes of CMS sub-detectors to characterize the FEE against EM interference. A summary of these studies, including the impact in the FEE susceptibility of FEE topology, Detector-FEE connection, power distribution board design and CM filter, and FEE grounding connection is presented. These tests have been remarkable important to evaluate weak areas of the system and the impact of the design in the FEE noise immunity. Similar procedures will be valuable to assess the electromagnetic compatibility between the FEE and power supplies in critical sub-detector up-grades for the LHC calorimeters.

XII. ACKNOWLEDGMENT

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XIII. REFERENCES

Design Considerations for Area-Constrained In-Pixel Photon Counting in Medipix3

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Abstract

Hybrid pixel detectors process impinging photons using front-end electronics electrically connected to a segmented sensor via solder bumps. This allows for complex in-pixel processing while maintaining 100% fill factor. Medipix3 is a single photon processing chip whose 55 µm x 55 µm pixels contain analog charge-processing circuits, inter-pixel routing, and digital blocks. While a standard digital design flow would use logic gates from a standard cell library, the integration of multiple functions and configurations within the compact area of the Medipix3 pixel requires a full-custom manual layout. This work describes the various area-saving design strategies which were employed to optimize the use of available space in the digital section of the Medipix3 pixel.

I. INTRODUCTION

Medipix3 is a single photon processing hybrid photon detector (HPD) which records the number (as well as the energies) of discrete photons incident on the segmented sensor. It aims to correct the effects of charge diffusion across the sensor volume by considering the total charge collected by all pixels within a local neighbourhood during the evaluation of a charge event. Simulations [1] and a prototype chip [2] have demonstrated that the distortion resultant from charge (of a single event) being shared amongst a cluster of pixels can be corrected by the reconstruction of the total charge into a single pixel. The in-pixel charge summing scheme necessitates complex inter-pixel routing, control logic, and decision-making circuitry. Furthermore, the successful use of the previous chip, Medipix2, in a variety of application fields, such as x-ray imaging [3], x-ray crystallography [4], astrophysics [5], medical instrument prototyping [6], and dosimetry in space [7] and high energy physics experiments [8], has motivated Medipix3 to be made programmable with enriched functionality. Whereas Medipix2 was realized in 0.25 µm technology, Medipix3 is implemented in a 0.13 µm 8-metal layer CMOS process. Although the reduced feature size of the latter technology enables higher transistor density, it was nonetheless challenging to fit the complex processing circuits within the Medipix3 pixel, which maintained Medipix2’s 55 µm pixel pitch.

This work explores considerations for designing pixels with high functional density. Section II provides a brief overview of the Medipix3 operation modes and a functional description of the pixel. Section III describes a layout optimization method for area reduction, with a practical example from the Medipix3 pixel. Finally, Section IV presents the conclusions of this work.

II. MEDIPIX3 PIXEL

A. Architecture

As an HPD, the Medipix3 detector consists of a photosensitive semiconductor sensor (e.g. 300 µm Si) bump-bonded to a front-end electronics chip. To facilitate the user interface, Medipix3 has kept the form factor of its predecessor’s active matrix, with 256 x 256 pixels of 55 µm pitch. Programming of Medipix3 however, will be much more complex than for Medipix2, given the large combination of functional modes and structural configurations. Table 1 lists the operation modes and Table 2 lists the readout modes of Medipix3.

Figure 1 shows a block-level description of the pixel’s architecture. The charge, collected from the sensor via the solder bump, is preamplified and then converted to a current. This current is replicated and sent to neighbouring pixels for charge summing and energy threshold discrimination. A winner-take-all routine performs the arbitration to decide to which pixel to assign the photon hit (i.e. the pixel with the largest quantity of charge within the local neighbourhood).

Each pixel has two threshold discriminators and two corresponding digital counters, which can be configured as two 1-bit, two 4-bit, two 12-bit counters, or a single 24-bit counter. The two counters/serial shift registers can be programmed to operate simultaneously in the same mode, or can be controlled to operate independently from each other using separate Shutter (Exposure) signals. In continuous read/write mode, the high energy threshold is ignored and the counters take turns counting pulses from the low threshold discriminator, thereby eliminating readout dead-time. When a counter saturates, its value is held at the maximum value for the remainder of the exposure duration (i.e. binary counter overflow is prevented). The counters can also be reset to zero by serially shifting logic-0 through all the bits, or by asserting a FastClear control signal to reset all the bits (within 48 clock cycles).

Due to the complexity of the Medipix3 processing circuits, there are almost 1600 transistors in each pixel, which is three times the number of transistors in the Medipix2 pixel.

B. Area Constraints

While circuit area is an issue for all chip designers, the space available for transistors is particularly constrained in pixels, where layouts are necessarily compact in order to achieve fine granularity. There exists a tradeoff between spatial resolution and functional complexity. Figure 2 shows the layout a Medipix3 pixel.
Table 1: Summary of Medipix3 Operation Modes

<table>
<thead>
<tr>
<th>Operation Mode</th>
<th>Charge Collection Configuration</th>
<th>Pixel Size</th>
<th>No. Energy Thresholds per Pixel</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Pixel Mode</td>
<td>1 solder bump per pixel (the sensor is connected to each pixel in the electronics)</td>
<td>55 µm by 55 µm</td>
<td>2</td>
<td>Each pixel operates independently from its neighbours and processes the charge collected from the sensor via its solder bump. The counters are incremented if the charge is greater than the associated energy threshold.</td>
</tr>
<tr>
<td>Charge Summing Mode</td>
<td>1 solder bump per pixel (the sensor is connected to each pixel in the electronics)</td>
<td>55 µm by 55 µm</td>
<td>2</td>
<td>Each pixel considers the total charge from the local 2x2 pixel neighbourhood (110 µm by 110 µm area) for threshold discrimination. The digital hit is assigned to the pixel which received the largest amount of charge from that event.</td>
</tr>
<tr>
<td>Spectroscopic Single Pixel Mode</td>
<td>1 solder bump per 2x2 pixels (the sensor is connected to each group of 4 pixels)</td>
<td>110 µm by 110 µm</td>
<td>8</td>
<td>Each 'macropixel' operates independently from its neighbours and counts photons based on the charge collected by its associated solder bump.</td>
</tr>
<tr>
<td>Spectroscopic Charge Summing Mode</td>
<td>1 solder bump per 2x2 pixels (the sensor is connected to each group of 4 pixels)</td>
<td>110 µm by 110 µm</td>
<td>8</td>
<td>Each 'macropixel' considers the total charge from the surrounding 2x2 'macropixel' neighbourhood (220 µm by 220 µm area) for threshold discrimination. The digital hit is assigned to the 'macropixel' which received the largest charge.</td>
</tr>
</tbody>
</table>

Table 2: Summary of Medipix3 Readout Modes

<table>
<thead>
<tr>
<th>Readout Mode</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sequential Read/Write</td>
<td>In the COUNTING STATE, both CounterA and CounterB record the number of photons impinging on the pixel while ShutterA and ShutterB, respectively, are open. In the READOUT STATE, the bits of CounterA and CounterB are serially shifted in turn.</td>
</tr>
<tr>
<td>Semi-sequential Read/Write</td>
<td>CounterA and CounterB can operate in COUNTING STATE or READOUT STATE independently from each other. Note: Only one counter can be serially shifted at a given instant.</td>
</tr>
<tr>
<td>Continuous Read/Write</td>
<td>The counters alternate operations: one counter is in COUNTING STATE while the other is in READOUT STATE. Each pixel effectively has only one energy threshold because both counters record the pulses from the lower threshold discriminator. Readout deadtime is eliminated because one counter is always recording while the other is being read out.</td>
</tr>
</tbody>
</table>
The Medipix3 pixel measures 55 µm on each side. The analog circuits (~220 transistors), occupy 30 µm x 52 µm, while the digital circuits (~1350 transistors), occupy 20.5 µm x 52 µm; the digital circuits are almost 10 times as dense as the analog circuits. The remaining area is reserved for inter-pixel communication lines, and physical separation between analog and digital circuits/lines to reduce crosstalk.

III. LAYOUT OPTIMIZATION

The Medipix3 pixel has a high transistor density due to the complexity of its functionality. Normally, a standard digital design flow would involve the use of logic gate building blocks from a standard cell library, with the physical layout realized by commercial place and route tools. While this is the most efficient method, it does not achieve the smallest area. To achieve the transistor density necessary to realize the complex processing capabilities of Medipix3, we used a full-custom manual layout approach.

A. Design Rule Restrictions

Figure 3 depicts the minimum sizes and spacing required in the layout of transistors. When adjacent transistors share an active region, the minimum distance between the polysilicon gates is c. When adjacent transistors occupy separate active regions, there is a minimum 2a + d distance between the gates. Since c < a, there a large overhead with respect to area when we place two neighbouring transistors on separate active regions. There is in fact 255% area cost to separate the active regions between adjacent transistors.

Figure 4 shows the limit on the number of transistors which can fit in a row of transistors. The worst case is to have all transistors lying on discrete active regions (1-T cells only). A 2-input logic gate in a standard cell library would be in the 2-T cell category, i.e. two NMOS (or PMOS) transistors on a single active region. A standard cell library would also contain some complex gates, e.g. OAI, composed of two simple gates. Complex gates would contain three or four transistors in an active region, such that the layout of each cell would be optimized for at most four transistors in a row. The most area-efficient approach would therefore be to have all transistors along a row share a common active region.

B. Full-Custom Layout Method

Due to the high number of transistors, a full-custom manual layout of a digital circuit is tedious and labour-intensive; hence, a full-custom design approach is necessary. Figure 4 shows the minimum area per row of transistors, assuming minimum-length transistors in 0.13 µm technology, minimum spacing between objects, and contacts on all the diffusion nodes. 4b shows that a customized layout, which places as many transistors as possible on a single active region, can result in a layout which is up to 44% smaller than using pre-laid out standard cells.

Clearly, if the two neighbouring diffusion nodes do not share the same signal, then the two transistors must occupy separate active regions. It would therefore be sensible to place transistors which share signal nodes side-by-side so that their active regions may be merged to conserve layout area. This would require that the hierarchy of a circuit block be flattened from the logic gate level to the transistor level.

Figure 2: Pixel layout

Figure 3: Minimum spacing requirements defined in process design rules of a given technology. a) Active region overlap past the polysilicon. b) Length of the transistor. c) Separation between two transistors on the same active region (with a contact on the common diffusion node). d) Minimum separation between two active regions. e) Separation between two transistors on the same active region (without a contact on the common diffusion node).

Figure 4: Minimum area per row of transistors, assuming minimum-length transistors in 0.13 µm technology, minimum spacing between objects, and contacts on all the diffusion nodes. 4b shows that a customized layout, which places as many transistors as possible on a single active region, can result in a layout which is up to 44% smaller than using pre-laid out standard cells.
intensive. While Figure 4b showed that it may be possible to save 44% in area by flattening the hierarchy of a circuit block, this strategy can also complicate metal routing. However, the added routing complexity may be the required tradeoff in order to achieve the transistor density necessary to realize the specified functionality within a pixel. The following describes the systematic approach which was used in the full-custom manual layout of the densest sections of the Medipix3 pixel:

i) Divide the overall circuit into major functional blocks of 40-100 transistors.
ii) Draw a flat (transistor-level) schematic for each block.
iii) Number each transistor and label each node.
iv) Label small squares of paper with the transistor numbers and nodes (each square to represent one transistor).
v) Optimize the arrangement of the squares, with the aim to maximize the number of transistors in an active region while aligning gates sharing common signals.
vi) Create a circuit floorplan diagram (e.g. Figure 6) to map the circuit.
vii) Place and route the transistors following the floorplan diagram.

By abstracting the transistors into labeled paper squares, it simplifies the visualization of common nodes and allows the designer to easily manipulate different floorplan arrangements. The floorplan map also makes it possible to keep track of 100 transistors of a flat schematic.

C. Practical Example

The following example illustrates the concepts described in the previous sections. Figure 5 shows the logic-gate level schematic of a control circuit used in Medipix3.

Figure 5: Schematic of a control circuit used in the Medipix3 pixel

Figure 6 shows a floorplan diagram of the circuit. This floorplan diagram aids the visualization of shared signal nodes, both between gates and diffusion nodes. This helps to align common signal nodes to reduce the complexity of routing. When the gates are properly aligned, it is also possible to achieve some routing in polysilicon, which can save space at a slight performance cost due to the additional resistance.
IV. CONCLUSIONS

In this work, we described the complexity of the photon processing circuits in the Medipix3 pixel. This functional complexity necessitated high digital transistor density, which could be realized using a full-custom manual layout.

The Medipix3 design has recently been sent to the fabrication facility. The impact of this level of density on yield will be determined after we test the completed chips.

V. REFERENCES

The VFAT Production Test Platform for the TOTEM Experiment


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Abstract

VFAT is the front-end ASIC designed for the charge readout of silicon and gas detectors within the TOTEM experiment of the LHC. A stand alone portable Totem Test Platform (TTP) with USB interface has been developed for the systematic testing of the TOTEM hybrids equipped with VFAT chips. This paper is divided into 3 sections; the first describes the hardware features of the TTP, the second describes the software routines for the control and systematic testing of VFATs, the third presents the analysis and a sample of results.

I. INTRODUCTION

The front-end ASIC designed for the readout of silicon and gas sensors within the TOTEM [1] experiment at the LHC at CERN is called VFAT [2,3]. Two types of VFAT hybrid have been developed for the TOTEM silicon and gas sensors. Figure 1 shows a close-up view of 4 VFAT chips bonded to an edgeless silicon sensor intended for use within the TOTEM Roman Pots.

Figure 1: A Roman Pot hybrid containing 4 VFAT chips bonded to an edgeless silicon sensor.

Figure 2 shows a VFAT hybrid designed for use with TOTEM GEM and CSC gas sensors.

Figure 2: VFAT mounted on a gas sensor hybrid. The chip and bond wires are protected from damage by a protective cap (not shown).

The Totem Test Platform (TTP) was conceived to be a “light” DAQ system for the production test of VFAT together with the hybrid. The goal was to have a compact and portable test bench for VFAT hybrids that can be controlled by USB connection from a laptop. Data is also read through the USB and data analysis software used to interpret the results. Further extensions to the use of the TTP as a “light” DAQ are also possible.

II. VFAT BRIEF OVERVIEW

VFAT [2,3] produces both “Trigger” and “Tracking” information. “Trigger” information, in the form of a programmable fast “OR”, can be used for trigger building. The “Tracking” information is in the form of binary “hit” channel data corresponding to a given clock period selected by a first level trigger (LV1A).

VFAT has 128 channel inputs. Each channel contains a low noise pre-amplifier and shaper followed by a comparator. Following the comparator are digital circuits used for generating the “Fast-OR” outputs, data storage and data packet construction.
On receipt of a trigger, the corresponding binary data is packaged together with time stamps into a data packet. The data packet has the form shown in Figure 3. Hence, for every trigger, the DAQ receives a data packet containing the individual VFAT identification no. (ChipID), the Bunch crossing no. (BC), trigger Event no. (EC) and the corresponding binary channel data. Also contained within the packet are, some status flags and a CRC check.

![Figure 3: The VFAT data packet corresponding to a triggered event.](image)

VFAT has a multitude of programmable options which range from programmable biasing to testability options. A full list of programmable options is contained within [3]. One extremely useful feature is an internal programmable test pulse generator which can deliver a charge pulse to a given channel for test and calibration purposes. Variables include channel selection, the polarity of the charge, the amount of charge and the phase of the charge delivery within one clock period. The amount of charge is controlled by an internal DAC called “VCal”. Another important variable is the comparator threshold. The coarse comparator threshold is given by the difference of two DAC values called VT1 and VT2. Positive thresholds are obtained by fixing VT2=0 and varying VT1, Negative threshold by fixing VT1=0 and varying VT2. Individual “fine” threshold adjustments are also possible using 5 bit “TrimDACs” in each channel.

### III. THE TTP HARDWARE DESIGN & ARCHITECTURE

![Figure 4: The TTP, itemizing its main components.](image)

The TTP is a compact (26cm x 10 cm) card, a photograph of which is shown in Figure 4 and followed by an itemized list of its main components.

2. A Roman Pot hybrid socket.
3. Four GEM hybrid sockets.
4. An i2c master hybrid socket (CCUM, that hosts a custom rad-hard i2c master ASIC namely CCU25 [5]).
5. A clocking & triggering hybrid socket (TTCrm, that hosts a custom rad-hard ASIC namely TTCrx [6]).
7. A USB 2.0 high-speed interface (CY7C68001-56PVC or “SX2” [8] by Cypress semiconductors).
8. Linear Regulators.

The TTP architecture is largely based on an existing test bench developed for the CMS Preshower [9]. It can be divided into four main subsystems controlling the functions of Triggering, Readout, Front-end control and Local control.

#### A. The Triggering Subsystem

The purpose of the triggering subsystem is to provide timing and fast command information to the front-end chips in a programmable way in order to facilitate system tests. The four encoded fast T1 commands are generated as described in Table 1. The encoding scheme used is a 3-bit pattern, thus requiring 3 clock cycles to be transmitted through a single line. The first bit of the pattern is always ‘1’ denoting the existence of a fast command and the remainder which is being transmitted (“00”=LV1A, “01”=BC0, “10”=Resynch, “11”=CalPulse).

The triggering subsystem is developed in such way that it can generate bursts of triggers by specifying the time intervals between consecutive triggers expressed in no. of clock cycles.
Table 1: The four fast T1 commands that can be sent by the triggering subsystem.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Priority</th>
<th>Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resynch</td>
<td>Synchronising reset of the front-end chips</td>
<td>1</td>
<td>110</td>
</tr>
<tr>
<td>BC0</td>
<td>Bunch crossing zero</td>
<td>2</td>
<td>101</td>
</tr>
<tr>
<td>CalPulse</td>
<td>Signal sent to the front-end to generate internal injection pulses</td>
<td>3</td>
<td>111</td>
</tr>
<tr>
<td>LV1A</td>
<td>Level 1 Trigger Accept</td>
<td>4</td>
<td>100</td>
</tr>
</tbody>
</table>

Figure 6: Timing variables for the generation of multiple triggers by the pattern generator.

Figure 7: RAM based pattern generator implementation.

Figure 8: VFAT Controller first panel.

Figure 6 shows how a burst of pulses (each of one clock cycle width) can be defined by a sequence of numbers (t1, t2, t3 … tN). The implementation of the pattern generator is based on a RAM, where the values T1, T2, T3 etc. are stored (Figure 7). Initially, the address counter is reset and therefore the first value (T1) stored in RAM appears at its output. This value is loaded to the down counter. When the down counter reaches zero, the output initiates a pulse. At the same time the address pointer of the RAM is incremented providing the next value (T2) to the decrementing counter and so on.

The triggering subsystem is able to generate bursts of up to 1024 LV1A (and/or CalPulses), with the time between two consecutive pulses being between 3 and $2^{12}$ clock cycles. The trigger bursts may appear in different ways depending on the internal triggering mode settings and other related parameters. Another feature of the system is that for every event, the corresponding event and bunch numbers are stored locally in two 256 word-deep FIFOs. By comparing the numbers stored in the FIFOs with the ones generated by VFAT included in every data packet, the user of the test bench can verify the synchronization with the front end system. The system can also accept trigger and clock signals provided from external sources. In addition, the ability to host a TTCrm module gives the possibility to interface with a standard TTC system.

### IV. TTP SOFTWARE

There are 2 principal packages used by the TTP. The first is the "VFAT Controller" and the second is the Analysis Software. Both of these packages are needed to run the VFAT Test Procedures used to characterise VFATs. This section describes the VFAT Controller, Analysis Software and the Test Procedures.

#### A. The VFAT Controller
The VFAT controller is used (as its name suggests) to control VFAT operation. The software was developed as a part of the FEC software package [10],[11] and the graphical user interface is based on the Qt libraries [12].

The first user panel is shown in Figure 8. This panel serves two functions. The first is a search for all components responding to I2C commands on the I2C bus. The results of the search are displayed on the top line indicating the number of VFATs found, their chip ID and other components such as CCU. The rest of the panel is used for downloading constants to the VFAT internal registers. In this way the VFAT mode of operation can be chosen and the biasing set-up. The panel also reads back from VFATs the downloaded parameters to verify the communication. A second VFAT Controller panel is used to command VFAT during manual tests and a third panel is used to select test procedures used in systematic chip testing. The different test routines available are described in part C of this section.

B. Analysis Software

The analysis software has been developed within the framework of the TOTEM Online Monitor [13]. It has two distinct parts; a graphical user interface based on Qt, and a data processing framework based on ROOT [14]. As a consequence it can be run in both interactive and batch modes.

The monitor takes three files as the input: a hardware configuration file, a binary data file and a VFAT I2C configuration file.

The hardware setup can be described as a tree. For example, one Roman Pot contains 10 hybrids, each hybrid has 4 VFATs and each VFAT has 128 channels. Each element in the tree is assigned a C++ class that can process event data and produce output plots or fit results.

The "Canvas layout" dialog shows the tree of all hardware elements in the left column. The right column shows the list of available output plots for the selected hardware element. This mechanism ensures that at each level of the tree, just the dedicated analysis is performed and the relevant plots are produced. Events are successively read from the binary data file (performing various consistency checks) and recursively processed through the element tree. Fits and production tests are performed and summary protocols are saved.

C. Test Procedures

The functions of the different routines available in the VFAT Controller are detailed in Table 2.

The results are then summarised in a summary file as well as fits and acceptance cuts. These summary files are stored in unique directories created from VFAT IDs and measurement timestamps. For detailed study; the results can be visualised by the analysis software.

Figure 9 shows plots of the response of DACs following the DAC scan. From these curves a precise knowledge of the analog biases and calibration of charge delivery can be obtained.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power measurement</td>
<td>The power consumption is measured automatically for VFATs in “Sleep” and “Run” modes.</td>
</tr>
<tr>
<td>I2C Check</td>
<td>Writes and reads to all VFAT internal registers and verifies the success of the operation.</td>
</tr>
<tr>
<td>Data packet check</td>
<td>Vigorously applies multiple triggers to VFAT and checks consistency of the data packets with a reference file. This routine checks the memory logic functions ie. counters, flags, CRC etc.</td>
</tr>
<tr>
<td>Mask check</td>
<td>Each channel is masked and then pulsed to verify “mask” functionality.</td>
</tr>
<tr>
<td>DAC scan</td>
<td>Routes the analog output of each DAC in turn to the DCU and scans the 8 bit DAC range. This is an important operation for calibration of the chip.</td>
</tr>
<tr>
<td>Pulse Scan</td>
<td>Characterisation of the analog performance such as noise and threshold. A channel is selected and an input charge swept through a fixed threshold providing data for S-curve analysis. Options include polarity of signal charge and High or Low resolution. High Res. instructs VFAT to inject charge to one channel at a time while Low Res. performs the procedure on many channels simultaneously.</td>
</tr>
<tr>
<td>Binary Scan</td>
<td>The binary scan is a quick method for identifying excessively noisy (singing) channels or dead channels. For each channel in turn, a constant signal charge is delivered a number of times well above threshold. A channel operating correctly will show the number of hits equal to the number of signal charge pulses (100%). A singing channel will also record hits when no signal charge is applied and hence will record greater than 100% whilst a dead channel 0%.</td>
</tr>
</tbody>
</table>

Table 2: Test routine options within the VFAT Controller

The results of the Pulse Scan can be viewed in the form of S-Curves. An S-Curve (shown in the top right hand plot of Figure 10) is a histogram of hits on a selected channel as a function of input pulse amplitude. Starting below threshold with 0% of hits and continuing to well beyond threshold (to 100% of hits) an “S” is formed. An error function fit to the curve yields the noise and threshold as the sigma and mean of the fit.
detector hybrids are connected to the detector using the onboard connector. This makes it possible to test other detectors with a full readout chain from the flexible VFAT front end to the USB connection of a PC. Often the lack of such system is a bottleneck in detector development.

The FPGA and additional connectivity on the TTP also allows larger systems with one TTP operating as a master for several others, and evolution of the system to match the needs.

VI. REFERENCES


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Parallel Session A6
Trigger 2
The Sector Collector of the CMS DT Trigger system:
Installation and Performance

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Abstract
Drift Tubes chambers are used for muon detection in the central region of the CMS experiment at LHC. Custom electronics is used for reconstructing muon track segments and for triggering the CMS readout. The trigger Sector Collector modules collect muon segments identified by the on-chamber devices, synchronize the data received from different chambers and convert from LVDS to Optical for transmission to the off-detector electronics. Installation and integration tests were developed for tuning both firmware and hardware of the Sector Collector system: results are reviewed. The system performance during CMS data taking with cosmic rays is discussed.

I. DRIFT TUBE TRIGGER SYSTEM

A. The Drift Tube detector
Drift Tubes (DT) chambers are installed in the central part (“barrel”) of the CMS experiment [1], they are used both for muon track reconstruction and trigger purposes. Chambers are embedded in the return yoke of the magnetic field. The “barrel” iron yoke is segmented in 5 elements (wheels) along the beams direction and in 30° azimuthal sectors in the transverse plane. Four chambers are installed in any sector at increasing distance from the beam pipe; they provide transverse momentum ($P_t$) measurement using the track bending in the CMS magnetic field. Schematic layout of the DT system for one wheel is shown in Figure 1.

Each DT chamber is composed by several layers of drift tubes, performing track segment reconstructions with mean-timer technique [2]. 250 DT chambers are installed in the CMS barrel (4 in most of sectors, 5 in the bottom and top ones of each wheel).

II. CMS LEVEL-1 TRIGGER SYSTEM

The CMS level-1 trigger is designed with custom pipelined electronics, so every collision (BX = 40 MHz bunch crossing frequency) is analyzed with no dead time. Goal of the Level-1 Trigger System is to select interesting events, in order to reduce the total rate of accepted events to less than 100 kHz. If a given event is accepted, a Level-1 Accept signal is issued to the sub-detectors and raw data are transmitted to the following CMS trigger level, called HLT.

A. DT Trigger Electronics Overview
Goals of the DT-based muon trigger are to perform muon identification, $P_t$ measurement and assignment to the correct BX. The electronics is organized in a logical tree structure.

First processing stages are installed on the detector, into aluminium boxes mounted on each DT chamber, called Mini-Crates. They have to reconstruct and select two track segments per chamber having higher $P_t$. Main requirements of the Mini-crate electronics are reliability and radiation tolerance, so that ASICs and pASICs technology have been preferred and redundant designs have been implemented [3].

Following processing stages are performed by track-finder electronics [4]. They are implemented on several custom VME boards which are installed in the underground counting room (UXC), which is separated from the detector hall with a several meters wide concrete wall. Their major tasks are to match segments among DT chambers and select 4 higher $P_t$ muons in the whole barrel.

The Sector Collector (SC) system perform link between local trigger (on-detector) and track-finder (in UXC) electronics.

III. THE SECTOR COLLECTOR SYSTEM

A. System Overview
The SC system, connecting on-detector and UXC electronics, has been designed following a sector-wide
segmentation. Any SC processing unit receives trigger data from the Mini-crates within a given azimuthal sector, synchronizes and transmits them (after properly remapping) to the track-finder electronics. SC units are located in VME crates hosted on the CMS towers (the metallic structures surrounding the detector, see Figure 2). Each Mini-crate delivers its output through 2 copper FTP cables using serial LVDS transmission (480 Mbit/s). Every SC unit receives data from 4 (5 in the top and bottom sectors of each wheel) Mini-Crates and send the output to the track-finder electronics through optical links. Sector output is transmitted through 6 optical links (GOL chips @ 1.6 Gbit/s). 2 crates per wheel are foreseen (lodged in the same rack); they host both SC units and read-out electronics devices.

Figure 2: View of CMS underground halls. Sector crates location and trigger data path from the detector to the underground counting room are shown.

B. Hardware Implementation

The SC unit is implemented with a 9U VME board (see Figure 3). Five piggy boards are plugged in: four of them are equipped with LVDS receiver electronics (LVDS-RX boards) and one (Opto-Tx) with optical transmitters. Each LVDS-RX receives trigger data from one Mini-crate (2 cables – 2 separate LVDS channels). In the top and bottom sectors of every wheel, the outer DT chamber is split in two separate ones, so that a special 4-channel receiver board has been produced.

The output optical links are connected to the track-finder electronics, through the Optical receiver cards (Opto-RX), installed on the same crates in UXC. 84 Optical receiver cards (Opto-RX) are being installed, 60 of them receiving trigger information relative to the transverse CMS coordinates (1 Opto-Rx per sector); 24 receive information relative to the longitudinal CMS coordinates, wedge-wide grouped (2 receivers per wedge).

A complete hardware description can be found in [5]. Main features are:

- Implementation of the processing devices with Flash-based Actel ProAsicPlus300 devices (radiation tolerance required);
- On-board FPGA programming through custom VME-to-Altera Jtag interface;
- Independent piggy board power supplies; LVDS-RX and Opto-Tx can be powered off in case of failure with I/O lines isolation;
- Spying of portions of trigger data that can be injected in the data acquisition stream;
- I2C internal bus for reading temperature and current sensors;
- Configurable custom JTAG chain for accessing ICs on the piggy boards (configuration, boundary scan, spying …).

In the Opto-Rx cards Altera StratixGX devices, with 8 embedded gigabit transceivers, are used.

Figure 3: Implementation of the Sector Collector.

C. Synchronization tools

Most important task of the SC system is to perform timing alignment of trigger data received from the chamber electronics within each sector; moreover, hardware tools have been provided in order to ease synchronization between sectors and wheels. DT trigger system has several sources of de-synchronization, inducing both fine (phase of signals) and coarse (several BX skew) de-synchronization among chambers and sectors data:

- Unrelated clock phases for different Mini-Crates (however each Mini-Crate behaves as a global synchronous device);
- Length of copper cables from Mini-crates to SC (ranging from 10 m minimum to 40 m maximum);
- Optical fiber skew: measurement of the propagation delay for all installed final fibers gave a maximum skew less than 20 ns.

Several hardware features have been implemented to take care of de-synchronization sources:

- Delay lines on the clock used to sample the SC input (32 steps – 1 ns/step, 1 delay line per LVDS-RX) and automatic confront between received and re-calculated parity bit; the check is performed on each LVDS cable independently;
- 0-to-7 BX pipeline on every single Mini-crate input;
- 0-to-3 ¼ BX pipeline (¼ BX step) on the Opto-Rx output.
D. Drift Tube Technical Trigger

A Technical Trigger based on DT has been developed during the SC commissioning. Its purpose is to provide a trigger signal suitable for debugging purposes. It is shown in Figure 4. Looking at the CMS official trigger path, the output of the SC units is fed into the track-finder devices and then sent to next selecting devices (Sorters). A Technical Trigger signal is built with the SC outputs taken at the track-finder input. Each track-finder checks its input data, received from the connected SC, and delivers a Technical Trigger bit signal if at least one chamber has valid triggers. Then, a cabled logic is used to perform (anti)coincidences. For instance, simple coincidences between upper and bottom sectors in the same wheel can be used to trigger on muons from cosmic rays when cross the CMS inner detectors.

Several V976 C.A.E.N. modules are used to implement the required cabled logic. The DT Technical Trigger has not been yet integrated within the CMS trigger but it was expensively used in DT local data-taking during sub-detector commissioning.

![Figure 4: Description of the DT technical trigger w.r.t. the standard DT trigger implementation. In this figure a simple connection with two adjacent sectors is shown.](image)

IV. SECTOR COLLECTOR PERFORMANCE

SC production and pre-installation tests were described in [5].

The system commissioning was performed with long data-taking both with random triggers and with muons from cosmic rays. First, each sector were instrumented with final connections and tested stand-alone, then several sectors were integrated in the official CMS data-taking campaigns, called Global Runs. Their aim was to gradually integrate CMS sub-detectors and perform global data-taking both with cosmic muons and technical triggers (random…). Participation of DT trigger electronics increased from few sectors (June ’07) to the full system (during last August ’08 Global Run). More than 250 millions of events from cosmic rays have been taken.

During Global Runs the Sector Collector performance were studied in order to achieve an overall DT trigger synchronization as well as with other CMS sub-detectors.

A. DT Trigger System Synchronization

The DT trigger synchronization procedure has been tested with cosmic muons but it’s very similar to the one that will be done with LHC beam.

First, for each Mini-crate the best clock phase has to be found. Details can be found in reference [6] where methods used for the best tuning with respect to the LHC beam phase are reviewed.

Then, a scan on the SC input has to be done, by varying the phase of sampling clock on each cable and finding (through parity bit check) the best value for the correct data sampling (Figure 5).

![Figure 5: Screenshot get with the SC control software, showing an example of scan in order to find the best phase of the input sampling clock.](image)

Next step is performed using the spied data of a SC boards. Spy registers are acquired when a fixed DT chamber into a sector has triggered; the trigger distribution vs BX shows peaks in other chambers, due to the correspondent muon which crosses (and induces a trigger in) more than one chamber. Pipelines on each station output are used to align peaks in time (Figure 6).

![Figure 6: Number of triggers vs. bunch crossing number for each station within a given sector. Example of the plots used for coarse timing synchronization.](image)
Finally, pipelines on Opto-RX cards are used to align data coming from nearby sectors (analyzing coincidences in the spy registers on the Track-Finder input) See Figure 7 for an event display showing a reconstructed muon track crossing chambers in nearby sectors.

Using the Technical Trigger can be useful even during beam data-taking. By accepting all single chambers triggers the contribution expected at trigger rate from cosmic muons will be less than 300 Hz (~ 260 Hz has been measured in the last Global Run). At low luminosities the contribution due to muons produced in collisions will be still acceptable. For instance, when \( L = 10^{31} \text{cm}^{-2} \text{s}^{-1} \) the trigger rate obtained with a global OR of all single chamber triggers will be about 500 Hz. Such a rate will allow a data sample useful for DT synchronization to be taken in few hours.

V. CONTROL SOFTWARE

During the SC commissioning, control software has been developed starting from the custom applications used during the system production and tests at the Bologna laboratory. Its major goal is to be integrated in the CMS software platform, properly designed in order to integrate all CMS trigger applications in a common framework.

The control software has to:

- Retrieve the hardware configuration parameters from database;
- Perform automatic power on of piggy boards;
- Load configuration parameters on hardware;
- Monitor hardware status (error flags, temperatures, current drawing…);
- Export monitored data to a “conditions” database;
- Provide user-friendly panels, showing system health.

The software has been implemented in the CMS Trigger Supervisor project. It provides facilities for customizing single applications (called “cells”), their communications (via SOAP protocol), connections with databases and graphical user interfaces for managing cells via http client.

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**Figure 7:** event display showing a reconstructed tracks of a muon which crosses nearby sectors.

**Figure 8:** event display of a cosmic muon track triggered with DT and crossing both muon and inner-tracking sub-detectors. CMS magnetic field was set to 3 T for this run.

**Figure 9:** Overview of the implementation of the Control Software for the SC system.

The overview of the implementation of the SC control software within the trigger supervisor has shown in Figure 9. Modularity requirements led to a two layer system. One Supervisor cell acts as interface with the CMS central TS.
application, as well as access point for any task performed by expert. Supervisor cell automatically manages 10 workers in parallel, each one performing hardware operations with a given VME crate.

As an example of the software performances, the configuration of the whole SC system takes \(\sim 30\) s from scratch (the so-called “cold start”, which needs all piggy boards to be powered on) and less than 1 s to only configure hardware (“warm start”).

Screenshot of one of the user-friendly panels implemented is shown in Figure 10, as seen from HTML browser. Information on the temperature sensors vs. time are provided with useful views (one panel per crate, one plot per board, one coloured tick per sensor).

![Figure 10: SC control software – screenshot showing panel for on-line temperature monitoring.](image)

A similar panel is shown in Figure 11, where a summary of the status of all boards in the system is summarized. Faulty boards are represented with red boxes. Buttons in the top of the web-page are used to select hardware features to be checked against faults, in order to provide easy diagnostic.

![Figure 11: SC control software – screenshot showing panel for on-line monitoring of board faults.](image)

VI. REFERENCES


The Commissioning status and results of ATLAS Level1 Endcap Muon Trigger System

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Abstract

The ATLAS Level1 endcap muon trigger selects potentially interesting events containing muons with the transverse momentum ($p_T$) greater than 6 GeV/c from 40 MHz proton-proton collisions. The system consists of 3,600 Thin Gap Chambers (TGCs) and the total number of readout channels is 320,000. The trigger logic is based on the coincidence between seven layers of TGCs. All processes are performed on fast electronics within 2.5 \(\mu\)s. To be ready for the first beam, we have succeeded in sending trigger signals of cosmic-ray muons with the synchronous operation at 40 MHz and fine signal timing adjustment. We report on the status of the commissioning and the results from the combined runs with all ATLAS detectors.

I. INTRODUCTION

The ATLAS experiment at CERN will start exploring new physics up to TeV energy scale at the beginning of spring 2009. We will start from the proton-proton collisions with a single bunch, and then the bunch-crossing rate will be increased to 40 MHz. In order to select interesting events efficiently with rejecting the large backgrounds generated with the production rate of 1 GHz (25 minimum bias events will be expected in a single collision, i.e. $25 \times 40 \text{ MHz} = 1 \text{ GHz}$), three levels of the trigger are designed at the ATLAS experiment. The first stage of the trigger (Lvl1) is based on the dedicated fast electronic circuits and makes a trigger decision to the second stage of the trigger (Lvl2) within 2.5 \(\mu\)s. The Lvl2 trigger and the third level of trigger, so called the event filter (EF), are performed by the simple event reconstruction codes on computers. The muon detectors and the calorimeters provide the Lvl1 trigger and reduce the event rate from 1 GHz to 75 kHz, while the Lvl2 and the EF select the events of interest more precisely using the muon detectors, the calorimeters, and the tracking systems and reduce the event rate from 75 kHz to 2 kHz, and from 2 kHz to 100 Hz, respectively.

The Lvl1 is a system of pipelined processors synchronized with the clock of 40 MHz, which is delivered from the clock of the LHC accelerator, so that all readout electronics of the subdetectors can identify the bunch-crossing numbers of interesting events, which are tagged by the Lvl1 trigger signals. Therefore, the constant latency and synchronous of the Lvl1 systems are mandatory. Since some of the trigger electronics are mounted on the detectors and the others are located in the shielded counting room, it is crucial to handle the latency and the timing of the trigger signals step by step as well as channel by channel.

In this paper, we report on the commissioning of the Lvl1 endcap muon trigger system and the results of the trigger analysis based on the data taken during the combined runs. In particular, we focus on how we handle the pipeline of the Lvl1 endcap muon system.

II. TGC TRIGGER

A. Thin Gap Chamber

The ATLAS detector has two kinds of muon trigger detectors. One is the Resistive Plate Chamber (RPC), which is located in the barrel region (pseudo-rapidity $|\eta| < 1.05$), and the other is the Thin Gap Chamber (TGC), which is located in the two endcap regions ($1.05 < |\eta| < 2.4$). The TGC is the gas chamber with multi-wires operated at the limited proportional
region (typical high voltage is 2,800 V). The small cell size with the short intervals of wires (1.8 mm) makes the time jitter less than 25 ns, which is comparable with the interval of the bunch-crossing. Thus, the TGC can distinguish a bunch-crossing of an interesting event from the others. The typical size of a TGC unit is around 1.5 m², and around 600 TGC units construct a wheel-shaped TGC station of 25 m in diameter, as shown in Figure 1.

![Figure 1: A picture of the TGC wheel. Almost all infrastructure including chambers, chamber services, electronics have been installed successfully in the ATLAS cavern at the beginning of 2008.](image)

There are two kinds of TGC units. One consists of 2 gas gap layers (doublet), and the other consists of 3 gas gap layers (triplet). The inner-most TGC station (TGC1), which consists of TGC units with triplet-layer, stands vertically 13 m apart from the interaction point in z coordinate defined by direction of the beam pipe. The middle TGC station (TGC2) and the outer-most TGC station (TGC3), which consist of doublet TGC units, stand vertically 14 m and 15 m in z direction, respectively (Figure 2).

![Figure 2: The cross-section diagram of the muon detectors looking at one fourth y-z plane. The scheme of the fast muon track finding is also overlaid. The TGC trigger finds muon tracks by taking coincidence between hits on three TGC wheels. Depending on the coincidence windows, low $p_T$ or high $p_T$ is determined. [1]](image)

The wire and strip signals from TGC are amplified, shaped, and discriminated on the Amplifier Shaper Discriminator circuit (ASD) on the TGC. Digitized signals are fed into Patch-Panel ASICs (PP-ASIC). Because of varieties of the time-of-flight (TOF) from the interaction point to the TGC and the cable length from the ASD to the PP-ASIC, the timing of the signals from ASD are not aligned between the channels at the PP-ASIC inputs. The difference of the timing between ASD outputs is adjusted by the PP-ASIC. The PP-ASIC also applies a proper bunch-crossing identification (BCID) for each hit, so that the coincidence logics are performed properly in the next circuit (Slave Board ASIC ; SLB-ASIC). The SLB-ASIC performs a coincidence between four layers in the The TGC2 and the TGC3 (the pivot plane) and three layers in the TGC1. While 3 out of 4 layers coincidence and 2 out of 3 layers coincidence are usually taken for the pivot plane and for the TGC1, respectively, the trigger condition can be tightened or relaxed depending on the beam condition, the noise rate of the TGC, and the response of the TGC. The outputs from SLB-ASIC are fed into High-$p_T$ coincidence Boards (HPT). The HPT combines coincidences from the TGC1 and pivot plane to find high $p_T$ track.

B. Trigger Electronics

Figure 3 shows an overview of trigger electronics.

![Figure 3: The TGC trigger electronics. Three steps of coincidence logic find high $p_T$ muon track out with $r$-$\phi$ coincidence. [1]](image)
candidates. Information provided by the HPT is \( r \) and \( \delta r \) for the wire signals, and \( \phi \) and \( \delta \phi \) for the strip signals. The \( r, \phi \) and the \( (\delta r, \delta \phi) \) mean the coordinate of muon tracks on the pivot plane and the deviation of hits on the TGC1 between the track trajectory of the virtual infinite momentum and the real track trajectory which is bent by the toroidal magnet, respectively. The HPT outputs are fed into the Sector Logic Boards (SL), which determine the momentum of the muon track by making coincidence based on \((r, \delta r, \phi, \delta \phi)\). The momentum of the muon track, which is quantized by six \( p_T \) thresholds, is calculated by the \( \delta r \) and \( \delta \phi \). In case of multi-candidates of the muon tracks, two muon candidates with the highest and the second highest \( p_T \) are selected. Since the trigger logics in SL are based on the Field Programmable Gate Array (FPGA), the requirements of the \( p_T \) threshold can be implemented whenever the experimental conditions are changed. The lists of the muon candidates are sent to the Muon Central Trigger Processor Interface (MUCTPI), which combines the number of the muon candidates provided by the TGC and the RPC triggers and makes the final decision of the muon trigger.

C. Requirements on Operation

Since the individual modules and a part of the trigger systems have been tested well during the development and the assembly of the TGC system, we focus on establishing a complete pipelined trigger system synchronized with the 40 MHz clock. In particular, the TOF between the interaction point and the TGC chambers are different depending on the \( \eta \), and 45 varieties of the cable length between the ASD and PP-ASIC are used as shown in Figure 4.

![Figure 4: Left: The varieties of the cable Length. Right: TGC response for 30 degrees incident angle. [2]](image)

We also use two varieties of the category 6 twisted pair serial links between the SLB and the HPT, and 26 varieties of the optical fiber links between the TGC detector and the counting room, so as to pass the cables with the minimum length. In order to make three kinds of coincidences described in the previous section, all signals need to be aligned properly. All ASICs and FPGAs have a functionality to delay the signals accordingly. Since the response of the TGC is varied within 25 ns due to the drift time as shown in Figure 4, the gate width needs to be optimized and the phase of the 40 MHz clock also needs to be set at the best position for the coincidences.

Furthermore, the goodness of the synchronization is not trivial, in particular, for such a high speed data transfer. The trigger links between the HPT and the SL send more than 12,000 bits in every 25 ns without any idle cycle. A proper procedure for synchronization is mandatory.

III. COMMISSIONING

Figure 5 summarizes variable delay functionalities. As described in the previous sections, due to the TOF and many varieties of cable length, the timing of the trigger signal needs to be adjusted in every circuits before making coincidences.

![Figure 5: Variable delays to align signals timing in each component.](image)

So as to send the Lvl1 muon trigger signals with the constant latency synchronized with the 40 MHz clock, we need to take care of

- timing alignment of the control signals,
- absorbing delays due to the varieties of TOF and cable length,
- absorbing delays due to varieties of category 6 serial links, and
- absorbing delays due to varieties of optical fiber links.

In the following subsections, we report on how to control these items in the ATLAS cavern.

A. Timing Alignment of the control signals

In the ATLAS experiment, the control signals including the 40 MHz clock, the Lvl1 trigger accept (L1A), the event counter reset (ECR), the bunch counter reset (BCR), the hardware initialization, and the test pulse trigger are distributed by the Timing, Trigger and Control (TTC) system [3]. Handling the timing of the control signals from TTC is crucial. In particular, the phase of the 40 MHz clock needs to be aligned channel by channel. Otherwise some channels may have an extra delay comparing with the other channels. For the TGC trigger system, the TTC system is located in the counting room and the all control signals are distributed from there to all hardware registers via several varieties of the optical fiber links. The propagation delay of each fiber link has been measured in the ATLAS cavern. The fastest control lines from the counting room to the electronics on detector are 251 ns, while the latest ones are 452 ns. The difference of them (i.e., \(452 \sim 251 \approx 200 \) ns) needs to be absorbed at the receiver of the TTC signals on detector, so called the TTCrx chip, which can set the variable delay with the resolution of 100 ps (fine tuning) and 25 ns (coarse tuning) [4]. Configuration
procedure for the TTCrx chip delay has been established in the ATLAS Data Acquisition System framework to have LHC clock signals with the same phase in all front-end electronics.

### B. Delays due to TOF and varieties of the Cable Length

The timing of the signals at the input of the PP-ASIC is different channel by channel due to the TOF and the varieties of the cable length. The difference needs to be aligned in the PP ASIC, before the SLB ASIC starts the first coincidence. The PP ASIC has a functionality of a variable delay which can set an additional delay for each channel. The delay can be varied from 0.9 ns to 28.5 ns with 32 quantized steps by using phase locked loop circuits.

The difference of the cable propagation delay can be emulated with the test pulse. As shown in Figure 5, the test pulse can be generated for all 320,000 channels, and the timing of the test pulse is configurable with the test pulse variable delay, which can be set with 0.9 ns steps (fine tuning) and 25 ns steps (coarse tuning). The propagation delay for each channel has been measured in the ATLAS cavern by scanning the response for the test pulses with several variable delays.

The delays due to the varieties of the TOF are simply calculated, assuming the muon tracks with the infinite momentum that come from the interaction point. Further fine tuning will be done using the beam collision data.

We estimate the propagation delay due to the sum of the cable length and the TOF from 64.7 ns to 116.0 ns. Based on these measurements, proper values of variable delays for all channels are set at the configuration process in the ATLAS data acquisition framework.

### C. Delays due to varieties of the Serial Link length

After the SLB ASIC, the trigger signals need to be synchronized with the 40 MHz clock via high speed serial links (category 6 serial links). Before the coincidence between the pivot and TGC1 plane, the difference of the propagation delay in the serial links needs to be absorbed, because we use the different length of cables for the pivot plane and the TGC1 plane. The serial link receiver in the HPT has functionalities of the variable delays and the switches of clock edges for latching input signals to align the input signals, and to absorb the phase difference between input signals and the 40 MHz clock on the trigger processor, as shown in Figure 6. The same functionalities are implemented for the optical links between HPT and SL.

The patterns of the test pulses emulating high-PTT muon tracks are used to optimize these delays. The wrong configuration of these delays causes the missing of coincidences, the instability of the latency, and the wrong correlation between the inputs and the outputs. 2,100 test track patterns have been sent via the serial links (12,096 bits/clock) and output patterns have been checked to be perfectly same as expected. The proper configuration of the delays for all serial links has been identically set from this measurement.

### D. Synchronization of the signals via optical fiber links

We use the Agilent HDMP-1032/1034 Transmitter/Receicer chip set for the communication between the HPT and the SL via the optical fiber links (G-Link) [5][6]. A 20-bits parallel word including a 4-bits coding field (c-field) and a 16-bits word field (w-field) are defined in this data transfer. 20-bits per an optical link are sent as the result of the muon track candidates at every 25 ns, which means the trigger system makes the decision of the muon trigger at every bunch-crossing. However, all "0" bits transfer, which means no muon candidates in an event, causes sometimes the problem with the synchronization between the HPT and the SL, because of two allowed data patterns of the optical fiber link. Therefore we need a special manner to solve this problem.

The G-Link protocol allows two kinds of data transfer, either 17-bits data transfer or 16-bits data transfer, depending on the setting of the 4-bits c-field. The 4-bits c-field must be "1101" in case of the 17-bits transfer mode, while c-field must be “1101" in case of the 16-bits transfer mode. Both transfer modes can be accepted for the communication of the SL with the HPT. If no muon candidates are found, HPT may send the pattern of w-field="0000 0000 0000 0000" and c-field="1101", followed by the inverted pattern (w-field="1111 1111 1111 1111" and c-field="0010"). In this case, however, the pattern with shifting by 1 bit, w-field="0000 0000 0000 0001" and c-field="1011", followed by the inverted pattern (w-field="1111 1111 1111 1111" and c-field="0100") can also be acceptable. This alternative causes the wrong synchronization and results the incorrect data transfer.

So as to solve this problem, we set the unique idle word (w-field="1111 1111 0000 0000" and c-field="0011") followed by w-field="1111 1100 0000 0000" and c-field="0011") at the beginning of the synchronization and establish the following the synchronization procedure;

1. Set the idle mode before the data taking.
2. Keep the synchronization to be locked.
3. Change the idle mode to the data transfer mode, when the data taking starts.

The procedure has been added into the ATLAS data acquisition procedure and confirmed to work well.
IV. COMBINED RUN

A. Combined run with the Cosmic Ray

Since the cosmic ray does not come from the interaction point but top of the ATLAS cavern, the trigger condition for the cosmic ray is set as the coincidence on the only pivot plane. With this condition, the total rate of the TGC trigger for the cosmic rays is around 50 Hz.

Since the data of the cosmic rays are collected by the TGC-self trigger without the synchronization with the beam-bunch crossing, in this combined run we check a part of trigger chain. We learn from the cosmic data that the trigger latency in the pipelined system (from the SLB coincidence logic to the SLB fifo buffer memory shown in Figure 5), measured as 91 clocks (= 2.275 µs), is fast enough. This assures the latency from the collision is shorter than the ATLAS requirement of 2.5 µs. Furthermore it is stably pipelined with the constant latency, which means the adjustment of the delays are well under-controlled.

B. Combined run with Proton Beam

On September 10th, 2008, we have successfully circulated the first proton beam with a single bunch in the LHC accelerator. The ATLAS has taken the data and seen the muons from the collision of the proton beams with the materials inside the beam pipe (the beam halo). We use not only the usual trigger with the 3-station coincidence but also the special trigger for the beam halo data which requires only hits on the pivot plane, in order to take the data of the beam halo effectively. Using the beam halo data allows us to measure the timing of the trigger for the tracks coming from the beam pipe. Since we can measure the timing when the proton beam passes the ATLAS detector (beam pickup trigger), comparing the timing of the TGC trigger with the beam pickup trigger tells us whether the TGC trigger timing is tuned for the beam collision. Figure 7 shows the TGC trigger timing with respect to the beam pickup trigger, in case the proton beam pass from one endcap side to the other.

Two sharp peaks around 1 and 5 correspond to the timing of the both of endcaps. The difference of two peaks (= 4 bunch-crossing, i.e. 100 ns) indicates the TOF of the proton beam between endcaps (~ 30 m) with the light velocity. We find that the timing of the TGC trigger is under-controlled for the beam collisions. Only concern is the width of the peaks is not within one bunch-crossing. This is understood because the estimation of the TOF for timing alignment is not for the tracks from the beam halo but for the tracks from the beam collision. We expect that the width of peaks should be within one bunch-crossing for the only beam collision data.

V. FUTURE PLAN

Further improvements of the TGC trigger can be done only with the data of the proton-proton collisions. They include the optimization of the phase difference between the signal and the clock, the optimization of the gate width of the signal, and the optimization of the high voltage and the threshold voltage. They are all under preparation to be achieved as soon as we have first collision data.

VI. CONCLUSION

Since the installation of all hardware components has been successfully finished at the beginning of 2008, we have been concentrated on the timing study for the beam collision and on the establishment of the operation procedure. All we can do without the beam collision have been done systematically. Furthermore, in the commissioning we have fixed the misconnections of the cables, and the bad modules and chips. The data taken with the cosmic rays and the first proton beam circulation indicate that the signal timing is fine-adjusted and the latency is well-understood. We are await for the first beam collision to search for the physics beyond the standard model, using muons triggered by the TGC which is well-understood.

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Level-3 Calorimetric Resolution available for the Level-1 and Level-2 CDF Triggers
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Abstract

As the Tevatron luminosity increases sophisticated selections are required to be efficient in selecting rare events among a very huge background. To cope with this problem, CDF has pushed the Level 3 calorimeter algorithm resolutions up to Level 2 and, when possible, even at Level 1, increasing efficiency and, at the same time, keeping under control the rates. This strategy increases the purity of the Level 2 and Level 1 samples and produces free-bandwidth that allows to reduce the thresholds. The global effect is an increase of the trigger purity and efficiency, most notably for physics triggers searching for Higgs and new physics. The Level 2 upgrade improves the cluster finder algorithm and the resolution of the Missing Transverse Energy (MET) calculations. The improved MET resolution will be soon available also at Level 1. We describe the CDF Level 2, Level 1 calorimeter upgrades, the architecture and the trigger performances. The Level 2 upgraded system is running as the official one since August 2007, the Level 1 is under commissioning.

I. Overview of the CDF Calorimeter Trigger

The CDF trigger [1] for Run II is a three level system. The goal of each stage in the trigger is to reject a sufficient fraction of the events to allow processing at the next stage with acceptable dead time. The Level 1 and Level 2 triggers use custom-designed hardware to find physics objects in a subset of the event information. The Level 1 is a deadtimeless synchronous pipelined system which form a trigger decision in 5.5 \(\mu s\). The Level 1 decision is taken on the basis of a limited reconstruction of the muon, track and calorimeter information. When an event is accepted by the Level 1 trigger, all data are moved to one of four Level 2 data buffers in the front end electronics for all subsystems. At the same time, subsets of detector information are sent to the Level 2 trigger system where some limited event reconstruction is performed and a Level 2 decision is made inside a dedicated PC. Level 2 decision PC has at its disposal all trigger objects used in Level 1, such as tracks from the eXtremely Fast Track trigger (XFT/XTRP), muon primitives and global energy information, as well as the complete Level 1 trigger decision information. Upon a Level 2 accept, the full detector is readout and data are sent to the Level 3. The Level 3 trigger uses the full detector information for complete event reconstruction in a farm of x86 PCs. Only the events accepted at L3 will be sent to mass storage. The goal of the calorimeter trigger (both at Level 1 and Level 2) is to trigger on electrons, photons, jets, total transverse energy (SumET) as well as missing transverse energy (MET).

Figure 1: CDF Run II Trigger System. Boxes in gray are subsystems upgraded in the past few years to prepare for the expected high luminosity of the Tevatron. L2 and L1 Calorimeter (L2 CAL) and Global Level 2 and 1 are the subsystems involved in the upgrade stages described in this paper.

In the following we use a coordinate system defined by the polar angle \(\theta\), measured from the proton direction, the azimuthal angle \(\phi\), measured from the Tevatron plane. The pseudo-rapidity is defined as \(\eta = \ln(\tan(\theta/2))\). For CDF Run II, all calorimeter tower energy information, including both electromagnetic (EM) energy and hadronic (HAD) energy, is digitized every 132 ns and the physical towers are summed into trigger towers, weighted by \(\sin(\theta)\) to yield transverse energy. A trigger tower covers 15 degree in azimuth \(\phi\) and approximately 0.2 in pseudo-rapidity \(\eta\). This results in a representation of the
The main task of the existing L2CAL was to find clusters using the transverse energy ($E_T$) of trigger towers. The cluster finding algorithm was based on a simple algorithm used for Run I, and was implemented in dedicated hardware. In this simple algorithm, the L2CAL hardware forms clusters by simply combining contiguous regions of trigger towers with non-trivial energy. Each cluster starts with a tower above a “seed” threshold (typically a few GeV) and all towers above a second lower “shoulder” threshold that form a contiguous region with the seed tower are added to the cluster. The size of each cluster expands until no more shoulder towers adjacent to the cluster are found. Because of this, large “fake clusters” are likely to be formed as the occupancy of the detector increases because towers which are unrelated to any jet activity have their $E_T$ boosted above clustering thresholds. One example of such kind of “fake cluster” is when towers above shoulder threshold between true jets link multiple jets together into a single large cluster (cluster merging). This would reduce the efficiency, and increase the rate, for triggers requiring multiple jets at Level 2 at higher luminosity, such as some important triggers for Higgs and top physics.

One more limitation of the existing hardware-based L2CAL system is that it does not re-calculate SumET and MET using the full 10-bit resolution energy information available, instead it uses the SumET and MET information directly from current L1CAL, which is based on 8-bit resolution. This design feature limits its trigger selection capability, or rejection power, for triggers with global transverse energy requirements.

The existing L2CAL trigger system has worked reasonably well at lower luminosity for Run II, however, as the occupancy in the calorimeter increases with luminosity, the simple hardware-based L2CAL system starts to lose its rejection power. As an example, figure 2 shows the Level 2 JET40 (Jet above 40 GeV threshold) trigger cross section growth with increasing luminosity.

II. THE CALORIMETER TRIGGER UPGRADE

The basic idea of Calorimeter upgrade is to provide the full 10 bit resolution trigger tower energy information directly to the Level 2 decision CPU where a cluster finding algorithm can reconstruct jets and recalculate MET and SumET and to recalculate the MET at the full resolution for the Level 1 Global Decision.

At hardware level, the full resolution (10-bit) calorimeter trigger tower data are received, preprocessed and merged by a set of Pulsar boards [2] before being sent to the Level 2 decision CPU where more sophisticated algorithms can be implemented. Since the actual cluster-finding is done inside the CPU, it is more flexible and more robust against increasing luminosity or higher occupancy in the calorimeter. With this approach, jet reconstruction using a cone algorithm which is currently being done at Level 3 can be moved to Level 2, albeit clustering trigger towers (instead of physical towers) and using only a single iteration in order to save processing time.

The inputs for the jet algorithm are all the non-zero energy towers. For each trigger tower, HAD and EM energy information are provided. The algorithm performs the following tasks:

1) Sums EM and HAD energy for each tower, selecting the seeds and shoulders according to the corresponding thresholds.
2) MET calculation: this operation can be done while looping over all the input towers for the previous item.
3) Sorts the seed list (for jets) by decreasing $E_T$.
4) Generates clusters, beginning with the first seed: sums the $E_T$ of all the towers above the shoulder threshold in a fixed cone centered on the seed tower.

The shoulder towers around the seed are directly addressed using a look-up table in order to speed up the algorithm. All towers used in the current cluster are identified as “used”. The algorithm then moves to the next seed tower in the list that is not identified as “used” and iterates. When the seed tower list is exhausted, a list of all the clusters that have been found is returned. At the same time the MET and SumET calculated exploiting the full 10 bits resolution of the trigger tower energy information.
The same Pulsar-based hardware can be used to calculate the full resolution MET information for L1.

A. Hardware Architecture

At hardware level, the basic idea of the L2CAL upgrade is to use Pulsar [2] boards to receive the raw (full 10-bit resolution) trigger tower energy information from L1CAL, merge and convert the data into SLINK format, then deliver the SLINK package to the Level 2 decision PC using FILAR (Four Input Links Atlas Readout) [5]. This is very similar to what has been done to all the other Level 2 trigger data paths for the Level 2 Global Decision upgrade [3].

The description of the Pulsar Board can be found in [2] and [3]. The design philosophy of the Pulsar board was to use one kind of general purpose motherboard, with powerful FPGAs and SRAMs, and to interface any custom data link with an industry standard link through the use of mezzanine cards. The key devices on the Pulsar board are three FPGAs (APEX 20K400BC-652-1XV [6]): two DataIO FPGAs and one Control FPGA. Both DataIO FPGAs are connected to the Control FPGA. Each DataIO FPGA interfaces with two mezzanine cards and the connections are bidirectional. Pulsar has a user defined interface to the P3 connector, and is used here for Control FPGA to send SLINK data package to the SLINK mezzanine card on a transition module on the back of the VME crate.

For the existing L2CAL system, since the clustering is done in hardware (designed in mid 90’s), the system is quite complicated. The entire system consists of eighty-six 9U VME boards (five different types) with six VME crates using custom P3 backplane. The upgraded L2CAL system only consists of eighteen identical Pulsars as data receivers, and a few existing Pulsar SLINK merger boards from the Level 2 Global Decision upgrade [3]. In order to receive the trigger tower energy LVDS signals from the L1CAL, a new Pulsar mezzanine card is designed for the data receiver Pulsars. Figure 4 shows how the mezzanines are mounted on Pulsar. Since the clustering algorithm will now be done in the Level 2 decision CPU, the Pulsar-based L2CAL system is much simpler and more uniform at the hardware and firmware level.

In the existing system one L2CAL board receives four LVDS input cables from the L1CAL system, corresponding to energy information (both HAD and EM) from eight trigger towers. In the new system, one new LVDS mezzanine card receives the same amount of input data as one L2CAL board in the existing system. With four mezzanine cards per Pulsar board, eighteen Pulsar boards are required to receive all the input data. A second set of SLINK Merger Pulsars receives and merges the eighteen SLINK channels into four and then deliver the data to the Level 2 decision PC using FILAR [5]. The same set of eighteen LVDS receiver boards can be used to improve the MET resolution at L1: they sent immediately the trigger tower energy information to an additional, but identical to the previous ones, LVDS Pulsar board which calculates MET and makes the L1 trigger calorimeter decision within the L1 timing constraints (5.5 µs). The LVDS pulsar boards will start to elaborate the L2 information when they will receive back the global L1 decision (3).
III. Performances

The Pulsar-based L2CAL upgrade has improved both jet and MET measurements at Level 2; at Level 1 will improve the Met measurement. Figure 6 shows the difference between the Level 2 and Level 3 in MET (Missing ET) and Jet transverse energy, for the existing system as well as for the upgraded system, with data taking at an average luminosity of $180 \times 10^{30} \text{cm}^{-2} \text{s}^{-1}$. The same MET difference has been measured between the future L1 Cal system and L3. These improvements allow a significant rate reduction as well as efficiency improvement in jet and MET based triggers both at Level 1 and Level 2. As example, Figure 7 shows the Level 2 JET40 trigger cross section growth with luminosity before and after the upgrade. Figure 8 shows the trigger efficiency curve for the Level 2 JET15 (Jet with $E_T$ above 15 GeV) trigger, for the upgrade L2CAL system and the existing system.

IV. Conclusions

We have presented the design, the hardware and software implementation and the performance of the Pulsar-based new L2CAL system for CDF experiment. The new L2CAL system makes the full resolution calorimeter trigger tower information directly available to the Level 2 decision CPU. The upgraded system allows more sophisticated algorithms to be implemented in software and both Level 2 jets and MET are made nearly equivalent to offline quality, thus significantly improving the performance and flexibility of the jet and MET related triggers. This is a big step forward to improve the CDF triggering capability at Level 2, to have enough flexibility to deal with potential new challenges at the highest luminosities, and to improve CDF new physics reach sensitivities beyond baseline. We’ve also presented the under commissioning L1CAL...
upgrade, easily obtained exploiting the flexibility of the same pulsar boards used for the L2CAL. We foresee many opportunities for additional improvements in trigger purity and efficiency, most notably for physics triggers searching for Higgs and new physics.

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Commissioning of the ATLAS Level-1 Central Trigger

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Abstract

The ATLAS Level-1 Central Trigger (L1CT) consists of the Central Trigger Processor (CTP) and the Muon to Central Trigger Processor Interface (MUCTPI). The CTP forms the final Level-1 Accept (L1A) decision based on the information received from the Level-1 Calorimeter Trigger system and from the muon trigger system through the MUCTPI. Additional inputs are provided for the forward detectors, the filled-bunch trigger, and the minimum-bias trigger scintillators. The CTP also receives timing signals from the Large Hadron Collider (LHC) machine. It fans out the L1A together with timing and control signals to the Local Trigger Processor (LTP) of the sub-detectors. Via the same connections it receives the Busy signal to throttle the Level-1 generation. Upon generation of L1A the L1CT sends trigger summary information to the DAQ and Region-of-Interest to the Level-2 Trigger system.

In this contribution we present an overview of the final L1CT trigger system as it is now installed in the ATLAS experiment and we describe the current commissioning and integration activity at the experimental site. The system is now continuously used during cosmic-ray runs to exercise the full trigger chain and read-out of sub-detectors. These test are bridging the experiment towards the commissioning phase with protons in the LHC started this summer. We discuss in particular the results achieved in operating the system with cosmic-rays and, the commissioning results with the first proton events in the LHC.

I. INTRODUCTION

ATLAS [1] is a general-purpose detector at the CERN Large Hadron Collider (LHC). At the design luminosity of \(10^{34}\text{cm}^{-2}\text{s}^{-1}\) the detector will be exposed every 25 ns to, on average, 25 proton-proton interactions. These conditions make the environment for the trigger system extremely demanding. It has to reduce the input event rate of 1 GHz to the limit of the storage rate of 200 Hz or less.

The ATLAS trigger system is divided into the Level-1 Trigger (LVL1), which is implemented in dedicated hardware, and in software-based High-Level Trigger. The LVL1 is a synchronous system working at the LHC bunch crossing (BC) rate of 40.08 MHz. It uses information from the calorimeter detector and muon spectrometer to reduce the event input rate to less than 75 KHz within 2.5 \(\mu\)s. Figure 1 shows an overview of the Level-1 ATLAS trigger system.

The Level-1 Central Trigger (L1CT) [2] consists of the Muon-to-Central-Trigger-Processor Interface (MUCTPI), the Central-Trigger-Processor (CTP), and the Timing, Trigger and Control partition (TTC). The MUCTPI receives information from the muon trigger detectors and combines it before sending it to CTP. The CTP forms the the Level-1 decision every BC and sends it together with the timing and control signals to the TTC partition of each sub-detector. The TTC distributes the timing, trigger and control signals to the sub-detector front-end electronics.

II. THE MUCTPI

The functionality of the MUCTPI is to combine the muon candidates from each muon trigger sector and to produce the total muon multiplicity for each of the six \(p_T\) thresholds. It resolves possible candidate double counting due to muon tracks that traverse more than one muon sector. This information is made available to the CTP, and for events selected at Level-1 the MUCTPI sends data to the Level-2 and to the DAQ system.

The MUCTPI is implemented in custom-designed 9U-VME64 modules and comprises 3 different kinds of modules plus a dedicated active backplane. There are 16 Octant Modules (MIOCT) which receive muon candidates from all 208 trigger sectors, resolves candidate overlaps and forms the local multiplicity.
The results are made available on the backplane (MIBAK). Each module has also memory used either in snapshot or programmable mode to monitor the trigger input or store the calculated candidate multiplicity. The MIBAK forms the total multiplicity and transfers the readout data from the MIOCT to the readout driver (MIROD). The MIBAK also distributes the timing and trigger signals to the system. The candidate multiplicity is sent to the CTP via the CTP interface module (MICTP) which also receives from the CTP the trigger and timing signal. The MIROD, for each Level-1 accepted event, sends summary data to the Level-2 and the DAQ system. Figure 2 shows the system, in its final configuration, as it is installed in the experiment.

III. THE CTP

The CTP receives, synchronizes, and aligns all trigger inputs, and forms the Level-1 Accept (L1A) decision. The L1A is throttled by preventive dead-time and ROD Busy signals from DAQ in order to avoid front-end buffers to overflow. The CTP receives timing signals from the machine if available, or generates them. It sends these signals with the L1A to the TTC partition of each sub-detector. For each L1A it sends summary information to the Level-2 trigger and to the DAQ system. The CTP CORE also has extensive monitoring capabilities. It can count incoming trigger rate and monitor the rate of programmable trigger combinations.

The Level-1 trigger decision is based on several trigger inputs. Candidate multiplicity from the calorimeter and muon detectors comprise electron/photons, taus/hadrons, jets and muons. The calorimeter detectors also provide the following energy flags: the scalar sum of the total transverse energy, the total missing transverse energy and the total scalar sum of the jet energy. There are 5 specialized triggers, namely: the Beam Pick-ups (BPTX), the Minimum Bias Trigger Scintillator (MBTS), the Beam Condition Monitors, the Luminosity Counters and the Zero Degree Calorimeter. Each sub-detector can also request triggers for calibration purposes. At any given run period a maximum of 160 trigger inputs can be used. In addition the CTP generates 2 random triggers, 2 pre-scaled clocks and 8 bunch groups. According to a programmable Level-1 trigger menu 256 trigger items are created by combining one or more conditions on trigger inputs. Each trigger item has a mask, a priority and a pre-scale factor. The priority is used in the algorithm to generate dead-time such that high priority items see as little dead-time as possible. The L1A is the logical OR of all enabled 256 trigger items.

The CTP is implemented in 6 different types of custom-designed 9U-VME64 modules and 3 dedicated backplanes as shown in Figure 3. The machine interface (CTPMI) receives the BC and Orbit signals from the LHC, and make them available to all other modules through the common bus (COM). The input module (CTPIN) receives trigger input signals, aligns and synchronizes them. The CTPIN has also scalers to monitor combinations of trigger inputs. There are three CTPIN in a CTP crate in order to receive up to 372 trigger inputs. Up to 160 trigger inputs are sent to the core module (CTPCORE) via the Pattern-In-Time bus (PIT). The CTPCORE combines the trigger signals into up to 256 trigger items, forms the L1A, and sends summary information to the Level-2 and the DAQ system. The CTPCORE applies to each trigger item the pre-scale factor and the preventive dead-time, and at each of these consecutive steps it features counters to register the trigger items.
activity. The monitoring module (CTPMON) performs bunch-per-bunch monitoring of trigger items. The output module (CTPOUT) sends timing and trigger signals to the TTC partition and receives the busy signal and the calibration request. There are four CTPOUT modules in a CTP crate. The calibration requests are sent to the calibration module (CTPCAL) through the calibration bus (CAL). The CTPCAL time-multiplexes the calibration requests and receives additional front panel input. The NIM to LVDS module receive additional front panel input.

**V. COMMISSIONING**

The L1CT system is being used in cosmic-ray runs since more than 2 years to provide trigger signals to an increasing number of sub-detectors as they are being integrated in the ATLAS experiment. Since few months the L1CT has been running in its final configuration receiving all foreseen trigger inputs and providing trigger signals to all sub-detectors. Cosmic-ray runs are particularly useful to exercise the system, to spot problems, and to improve monitoring capabilities. These runs are also important to synchronize the distribution of the timing signals to sub-detectors and to timing-in trigger inputs. At the beginning of September we started preparing for the first beam events in the ATLAS experiment. To have a reference signal induced by the beam we used two systems: the BPTX and the MBTS.

**A. BPTX**

The Beam Pick-ups are electrode pads placed onto the beam pipe at 175 m upstream the ATLAS interaction point. Both beam pipes are equipped with a set of electrode pads to monitor the passage of each beam. When a bunch traverses these pads it induces a very fast (rising time $O(\mu s)$ bipolar signal, proportional to the number of protons in the bunch. This signal is discriminated and send to the CTP. The BPTX signal is the time reference for the ATLAS experiment determining the presence of a filled bunch in the detector. It will be also used to monitor the beam intensity and the presence of satellite bunches around filled bunches. At bunch intensity $> 5 \times 10^9$ protons it has a trigger efficiency of 100% up to nominal LHC intensity.

**B. MBTS**

The Minimum Bias Trigger Scintillator are plastic scintillators placed in the forward region of the ATLAS detector. They are arranged in two discs located 3.5 meters from the interaction point and covering the transverse region within 14−88 cm from the beam axis. Each disc is divided into 8 identically $\phi$ sectors and each section is divided into an inner and outer part, for a total of 16 scintillators per side. Each scintillator is readout by a single photomultiplier. The signal of the photomultiplier is shaped by using the hadronic calorimeter electronics, it is discriminated and fed into the CTP. The CTP receives a trigger input for each of the 32 MBTS signals. This system is particularly useful in the initial period of the LHC start-up. It is relatively simple to commission, and it has a good trigger efficiency for single beam events like beam-losses, beam-gas, and beam-halo events.
C. Commissioning with beam

The very first events to trigger on were exceptional events, where a proton bunch was sent onto the beam collimators. About $2 \times 10^9$ protons interacted with the collimator upstream the ATLAS detector and resulted in a extraordinary number of secondary particles traversing the detector. The trigger setup for these initial events was such to ensure a good probability to trigger some of these events. The trigger items enabled were the lowest $E_T$ threshold in the electromagnetic and hadronic calorimeter (1EM3, 1TAU5, 1J5) and the MBTS. We chose these trigger items because they had a large probability to fire a signal, they were timed-in with the detector readout and because they had an acceptable cosmic trigger rate of about 20 Hz. A small cosmic trigger rate helped in minimizing the dead-time of the system, and thus enhancing the probability of being ready to trigger on the “collimator event”. Figure 5 shows one of these events as reconstructed in the ATLAS detector. After these spectacular events, we had a phase where the beam had been circulating for several turns. At the beginning of this phase the beam was not very collimated producing large signals in the detector (fig. 6) and had a lifetime of 10 to few hundreds LHC turns. In these conditions we had signals in the BPTX, in the MBTS and in the other triggers contributing to the L1A. These events enabled us to measure the relative delay of the BPTX with respect to the MBTS. We measure the BPTX delay by looking at the scope traces (fig. 7) of the BPTX and the MBTS, and by using the CTP readout data. The BPTX input to the CTP was then pipelined by the appropriate delay. The BPTX trigger bit was taken as the time reference of the passage of a bunch in the ATLAS detector. For this first period the BPTX signal was the only trigger item contributing to the L1A decision. The oscilloscope screen shot in Figure 7 shows the BPTX discriminated pulse and signals from three MBTS counters. The time separation between two consecutive signals in each channel corresponds to the LHC turn of $89\mu s$. It is interesting to notice that the BPTX and the MBTS are sensitive to different beam conditions. At the beginning of injection (first pulses) there were BPTX triggers and little signals in the MBTS, this is probably due to the fact that the bunch had its maximum intensity and it was relatively clean. After few turns the BPTS didn’t fire a trigger probably because the bunch lost intensity, while the MBTS were still producing large signals being sensitive to beam-halo.

The monitoring capabilities of the CTP were particularly useful at this time. We constantly monitor online the rate of each trigger input to the CTP versus time. This is the first sanity check to determine if trigger signals sent to the CTP are actually received, and to monitor the behavior of trigger inputs which are not enabled in the trigger menu. For all Level-1 trigger items included in the trigger menu, the rate at each step towards the Level-1 trigger decision is monitored, made available on the online information service, and permanently stored in a database. The rate is sampled for each luminosity block: a programmable time interval that represents the time unit of data taking of the experiment. The rate is calculated for signals on the PIT bus, for trigger items before pre-scale, after pre-scale, and after dead-time is applied. This information is essential to determine the dead-time of the experiment. This information is based on counters that record signals every bunch crossing, independent of whether or not the corresponding event will be accepted by the trigger decision. For events accepted by the full trigger chain the L1CT readout data are available offline. The CTP can be programmed such that it sends to the DAQ system together with the information relative to the Level-1 decision the activity of each trigger item in a programmable time window around the bunch-crossing corresponding to the L1A. This information is relevant to determine the time alignment of trigger items with respect to the L1A. Figure 8 shows such information in the form of a two-dimentional plot. On the x-axis there are the different trigger items before pre-scale (this plot only shows item 8 to 86
of the 256 items), and on the y-axis there is time in unit of BC with respect to the L1A. For this data sample the L1A was always fired by the BPTX. By using this information, after having integrated more events, we started to determine the time offset of stable trigger items with respect to the L1A. After the very first period of circulating beam in the LHC, the beam became much more clean, circulating in the LHC for several minutes. During this phase, the majority of the events had activity only in a small part of the detector, being compatible with beam-halo and beam-gas events. At this stage we triggered also on forward muons using the muon forward trigger input (TGC). Figure 9 shows a display of an event triggered by the TGC and also seen in the muon precision chambers. This event is compatible with a beam-gas event upstream the ATLAS detector.

![Oscilloscope screen shot. From top to bottom the four channels correspond to the BPTX discriminated pulse and signals from three MBTS counters. The time separation between consecutive signals in each channel corresponds to the LHC turn of 89 µs.](image1)

Figure 7: Oscilloscope screen shot. From top to bottom the four channels correspond to the BPTX discriminated pulse and signals from three MBTS counters. The time separation between consecutive signals in each channel corresponds to the LHC turn of 89 µs.

![Two-dimensional plot that shows the number of triggers for each trigger item around the BC associated to the L1A. The plot shows only items 8 to 86 of the 256 items. The time window on the y-axis in unit of BC is centered on the BC of the L1A (BC=0) and goes from -15 to 15 BCs. The colors (gray intensities) are proportional to the number of triggers in the cell.](image2)

Figure 8: Two-dimensional plot that shows the number of triggers for each trigger item around the BC associated to the L1A. The plot shows only items 8 to 86 of the 256 items. The time window on the y-axis in unit of BC is centered on the BC of the L1A (BC=0) and goes from -15 to 15 BCs. The colors (gray intensities) are proportional to the number of triggers in the cell.

![Event display of an event triggered by the forward trigger muon detector (red), seen also in the muon precision chambers (blue).](image3)

Figure 9: Event display of an event triggered by the forward trigger muon detector (red), seen also in the muon precision chambers (blue).

VI. CONCLUSION

The ATLAS first-level trigger is a 40MHz synchronous system based on information from the calorimeter and the muon detector and on dedicated trigger detectors. It reduces the event rate from 1GHz to about 75KHz within a latency of less than 2.5 µs. Since a few months the system is complete and it has been routinely used during cosmic-ray data taking. This September, we have successfully used the system with the LHC in inject and dump mode and with single beam radio-frequency capture and circulating for several minutes. These first days of data taking with beam represented an important milestone in the commissioning and operation of the trigger system. We succeeded in collecting beam events then reconstructed in the ATLAS detector, and we started the final phase of the commissioning of the L1CT with circulating beam in the LHC.

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Abstract
The CMS Global Calorimeter Trigger HCAL Muon and Quiet bit processing function is being implemented with a micro TCA system. This system is reconfigurable in both logical functionality and data flow, allowing great flexibility to meet processing requirements. The system consists of a processing module based on a Xilinx Virtex 5 FPGA and custom backplane based on a Mindspeed crosspoint switch. The overall progress of the design will be presented. In addition, future application of this technology for the SLHC level 1 trigger will be discussed.

B. Architecture
This function is being implemented utilizing a multi-gigabit switched serial mesh processing topology. It represents an evolution of the current GCT architecture, taking advantage of the lessons learned implementing the optical data transmission and concentration between the Regional Calorimeter Trigger racks and the GCT leaf cards. This topology is realizable in the micro TCA communications equipment standard, with a custom (though spec compliant) backplane, and has been described in detail in a previous paper. Due to the flexibility of the optoGTI, the Muon and Quiet bits function can be implemented with three processing modules in a commercial micro TCA crate. The core concept is that high speed serial links (both fiber and copper) are used for all communications both internally and externally. Analog crosspoint switching technology is used to provide a flexible communications mesh, allowing a regular hardware topology while retaining significant data routing options. Based on extensive experience with FPGAs in many applications, a conscious decision was made to provide plentiful link routing, since connectivity remains the primary limiting factor in fully utilizing the logic resources of large FPGAs.

II. PROCESSING MODULE DESIGN
The processing module provides the data manipulation functionality to implement muon and quiet bit system logic, and directly interfaces to the fiber input from the RCT (through the GCT source cards). It consists of three fiber I/O modules, a Xilinx V5LX110T or FX70T FPGA, a Mindspeed 21141 crosspoint, and an Ethernet enabled micro controller for slow control. The design has been presented previously, but is necessary background for the detailed implementation information that follows.
A. Primary Elements

The fiber input modules are the same family of MTP modules used on the GCT leaf cards, and provide the dense packaging required to physically concentrate data to feed the large FPGA. These modules provide either 12 input, 12 output, or 4 in and 4 out. They are currently available rated up to 3.2Gbps.

The processing FPGA is a Xilinx V5LX110T or V5FX70T, which provides 16 3.2Gbps (6Gbps in FXT70) serial links in addition to generous logic and routing resources. This family of FPGAs also provides analog PLLs, which result in more stable frequency synthesis. All control and configuration information for the Mindspeed crosspoint flows through the V5, allowing firmware to directly control local data switching if required.

The Mindspeed 21141 crosspoint is the data hub of the module, routing data to/from the optics, FPGA, and backplane. Since all data flows through the crosspoint, it can be routed, or duplicated, to any destination. The crosspoint switch automatically detects and powers down unused links to reduce power consumption, and includes analog conditioning to clean up degraded signals.

The micro controller is the slow control interface, and includes an integrated Ethernet MAC. This device supports TCP/IP sockets, simple telnet, and http protocols. It also supports I2C, which is the system management interface of uTCA. It performs all the required negotiation with the backplane during module initialization and removal. In addition, it is possible to program the FPGA and configuration memory via the micro controller. The device chosen is the NXP (Phillips) 2368, an ARM-7 based device with 512K of FLASH on chip, and many integrated peripherals in addition the the Ethernet MAC. The selection criteria was maximum integration, and though not impressive, the performance is more than adequate for control and configuration tasks.

B. Power

The module power subsystem, although not as functionally interesting, is a critical part of the module design. The power subsystem consists of two parts, the uTCA mandated power management logic, and the high current analog and digital power required by the FPGA and crosspoint.

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The module receives 3.3V management power and 12V payload power from the backplane. The management power is activated first, and powers the micro controller and related logic. When the module is plugged in, or the system is powered up, the micro controller negotiates with the backplane, which then commands the crate power module to energize the payload power. Similarly, when the module is unplugged from a running system a micro switch on the ejector signals the micro controller to shut down the payload. A front panel LED is used to indicate that it is safe to remove the module.

More critical from an engineering standpoint is the low voltage generation scheme. Five voltages (3.3V, 2.5V, 1.8V, 1.2V, 1.0V digital/analog) are required for the various core and I/O loads on the module. These are derived from three switching POL supplies, running at 3.3V, 1.8V, and 1.0V. Analog regulators supply the 2.5V, 1.2V, and 1.0V analog. The 1.2V and 1.0V analog supplies power the crosspoint and FPGA serial links, and require careful attention to achieve reliable link operation. Due to the potentially high power required by the crosspoint (10 watts), this more complex supply was prototyped to verify it’s performance.

C. Clocking

The module supports a simple clock distribution scheme designed to supply the FPGA with a low jitter reference clock, and general logic clocks. The clock tree is based on a differential 4x4 discrete crosspoint that connects both backplane clock inputs, a local oscillator, and an output from the crosspoint to 4 groups of 2 high speed serial reference clocks, 1 global clock, and 1 crosspoint input. Of these clock sources, the local oscillator and backplane clocks are best suited for serial link references.

D. New PCB Structures

The module implements over 150 multi Gbps differential signal and clock pairs, and required the use of more advanced PCB design and construction techniques than used on the GCT. When preliminary design files were sent to the PCB vendor, they recommended that the construction technique be modified to including new structures to reduce fabrication risk. These techniques are considered main stream by the PCB
vendor, and in their view reduced fabrication risk. The prototype production had a yield of 100% (admittedly on only 5 boards), which supports their assertion. The new technologies used on the module are via in pad, micro vias, and build up PCB manufacture.

With BGA ball pitches of less than 1mm becoming more common, it is becoming more challenging to use traditional escape techniques and maintain required clearances. This is especially true when drill vias are used. The alternative of drilling the via directly through the pad has always carried the risk of compromising the solder joint of the BGA ball. The void in the pad wicks solder away from the BGA ball, starving the joint of solder and creating a weak bond. As the via gets deeper (more layers traversed), the worse this problem becomes. The module utilizes BGAs with .8mm ball pitch, which precluded the standard escape pattern. Instead, a 6 mil laser drilled via is used directly through the pad. The use of such a small via, which only penetrates 2 layers, produces a very small void in the pad, and is considered acceptable for reliable bonding of the BGA.

Micro vias are very small laser drilled structures that span a single PCB layer. Their small size and span makes them ideal for high speed signalling, providing minimal inductance and impedance discontinuity. Obviously, they are limited in use with other construction techniques to be very useful. Typically, they are aligned with an underlying via (stacked), to allow for greater spans. In order to properly join vias in this manner, the underlying via needs to be filled to create a large enough contact surface.

It is typical to combine micro vias with a incremental PCB fabrication technique known as build up manufacturing. This entails depositing one layer of the PCB at a time, and laser drilling the micro vias for that layer before going on to the next. This allows the micro vias to be stacked to provide many more blind and buried spans than previously possible, while providing better registration for small PCB structures.

E. Module Stackup

In comparison with the GCT leaf cards\(^2\), the processing module used fewer layers with more via spans. The GCT leaf cards were constructed in 14 layers with four via spans in a three layer laminate process. Maintaining proper registration in a three layer laminate was a manufacturing challenge, and resulted in a surcharge for production. In contrast, the uTCA processing module was constructed in 12 layers with 8 spans in a 2 layer laminate with two layers of buildup (both top and bottom). This board was considered standard process, and will be less expensive to produce. In our case, the cost reduction was not the goal, but rather to use the extra via spans to successfully route the many high speed pairs within the overall board thickness allowed.

The detailed stackup of the module is shown in figure 3. It was constructed as two 4 layer boards with through drill vias laminated together. The laminated assembly was then drilled through, and vias filled. A single built up layer was added top and bottom, and micro via spans (1 layer) laser drilled. These vias were then filled, and the final top and bottom layers deposited. The final micro via spans were added, completing the construction.

F. Signal Integrity

The requirement of maintaining a 100 ohm impedance, and meeting micro TCA board thickness requirements necessitated the use of 3.5 mil trace widths on all stripline differential pairs (layers 3, 5, 8, and 10). Such small dimensions are not optimal for multi GHz signals, and several tests were performed to insure adequate signal amplitude over the trace lengths used in the design. In addition to software simulations, a test was performed on equivalent coax to verify the attenuation characteristics. Figures 5 and 6 show the results of the equivalent coax test. Note that 10-20% pre-
emphasis will be required to maintain full amplitude on the receiving end.

Figure 5: Input test pulse (equivalent coax test)

Recognizing that our testing is really a “best case” scenario, a test board has also been designed using the same stackup and PCB structures to verify the design margins. While unfortunately too late for the processing module, the results will be used to guide the backplane design, which we believe will have even higher routing congestion. The test board utilizes high performance edge mount connectors (over 10GHz analog bandwidth) and is designed for easy connection to network analysers, TDRs, and high bandwidth oscilloscopes. The test board is the same form factor as the processing module, so that in addition to testing board trace properties it can also be used to test backplanes and connect test equipment to running systems. Several connections are available on the front panel for this purpose, while the trace test connectors are designed for bench use only. During assembly a board will be dedicated to one of these purposes, and will have a subset of all possible connectors installed. The test board is now in the process of being ordered, and should be available within a few months.

III. ALGORITHMIC IMPLICATIONS

Experience on the GCT has shown that much more effort is spent on the firmware design and integration than on the initial hardware design and test. While the initial application of the processing module in the GCT Muon and Quiet bit system is rather trivial, using such modules in future trigger applications will not be.

A. Current State of Trigger Processing

The GCT implements the jet finding algorithm defined by CMS as large combinatorial functions. The details are a bit more complex, but the goal was to achieve the jet finder with as few clocks as possible. This is due to the fact that the latency budget is limited, and large combinatorial functions avoid the dead time associated with the combinatorial settling time versus the clock period. Currently this is hand tuned to optimize throughput by matching these times as closely as possible while maintaining the required setup time for the pipeline registers. The jet candidates identified by each jet finder are then forwarded to a series of comparator stages which sort the candidates and forward the most energetic three to the Global Trigger. Due to the large number of parallel connections required to transport the jet objects, much of the GCT is composed of I/O bound FPGAs that utilize a small fraction of their logical capacity. The large number of signals that need to be routed between stages drive the design of the system, and favour large boards with extensive cabling. This situation is not unique to the GCT, but is shared by many subsystems of the CMS Trigger.

B. Future opportunities

The hard serial nature of the processing module lends itself to a physical concentration of data not possible in current systems. Along with this advantage comes the challenge of processing much larger data sets as efficiently as possible.

The current scheme of hand tuning the combinatorial object finding functions works well, but will run into problems as the number of regions scanned increases, or if several types of data are required to properly discern trigger objects. The root cause of this is that the size of the functions increase geometrically with a linear increase in the number of inputs. Unfortunately these are exactly the algorithmic modifications being discussed for the SLHC upgrade. The result of this situation will be much longer compile/optimization run times, and a loss of synthesis efficiency since the FPGA devices are being used in a mode which does not take full advantage of their functional architecture.

The optimal solution is not obvious, and will depend on the details of the algorithmic modifications deemed appropriate. An obvious implementation option is to utilize a pipeline clocked by a multiple of the LHC clock that approaches the limit of the FPGA. While less efficient than a combinatorial implementation, it will result in much faster optimization and higher synthesis efficiency. The key challenge in this implementation will be to break the algorithm into small stages compatible with a few levels of FPGA logic. It is likely that this approach will lead to FPGA
A related option is to evaluate new technologies that may be better suited to the primary algorithms than what is currently being used. Archronix\textsuperscript{[4]}, a relative newcomer to the FPGA business, has developed an FPGA based on an asynchronous handshaking model. In this model the data flows through the processing logic as fast possible, so no dead time accumulates due to setup margins required to accommodate a global clock. Figure 7 illustrates the general idea of this approach. The efficiency gained allows these FPGAs to run at 3 times the speed of comparable synchronous designs – 1.5GHz at 65nM. While conceptually simple, it is obvious that for complex designs the overall data interlocking will not be trivial. While Archronix claims these complexities are handled transparently in their technology mapper, allowing the use of familiar synchronous RTL design entry, it will require serious evaluation before they can be considered as a viable alternative. However, if the tools prove to be robust, these devices will likely provide the most efficient implementation of future trigger algorithms.

![Figure 7: Synchronous vs. Asynchronously interlocked logic](image)

### IV. Conclusions

The uTCA architecture lends itself well to the processing requirements of the GCT muon and quiet bit system and provides a path forward to the future. The hard serial nature of the system lends itself well to the physical concentration of data required to implement more sophisticated trigger algorithms currently being discussed. Much work still needs to be done in the definition of SLHC trigger requirements and evaluating the appropriate technology for implementing future systems.

### A. Current Status

The processing module PCB has been fabricated and received at Los Alamos. Assembly has been delayed due to problems with finding an appropriate vendor. A vendor has currently been selected and finished boards are expected by the end of October. The test board is currently being quoted, and is expected in the same time frame as the processing module.

### B. Future Development

The modular nature of the system, with its considerable data routing flexibility, make it an attractive architecture for future trigger system development on the SLHC. Basing a large trigger system on a high bandwidth fine grained modular commercial standard would allow a degree of standardization not possible with the traditional full custom approach. As it stands, the generic nature of the V5LXT/FXT FPGA and it’s built in features suggest that many applications could be addressed. The technology utilized is also compatible with the Archronix asynchronous devices, but would need a board spin to support the pinout and power supply configuration required by these parts. Indeed, the module is little more than a stand alone FPGA carrier with a fiber interface and multi-gigabit serial switching support.

The challenges of firmware development for such a system are beyond the scope of the paper. Experience on the GCT has shown that utilizing many serial links on the same device is not trivial, and moving to a hard serial architecture will highlight these difficulties. Focusing on standard implementations supported by the manufacturers will be key in overcoming this challenge. Merely providing a solid hardware platform will not insure success. Much effort will need to be made in providing a stable, reusable framework of firmware modules to allow designers to be productive and keep integration efforts reasonable.

### V. References


Friday 19 September 2008

Parallel Session B6
Programmable Logic, Boards, Crates and Systems
Transmission-Line Readout with Good Time and Space Resolutions for Planacon MCP-PMTs

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Abstract

With commercially-available multi-anode microchannel plate photomultiplier tubes (MCP-PMT) and electronics, resolutions significantly better than 10 psec have been achieved in small systems with a few readout channels\cite{1, 2}. For large-scale time-of-flight systems used in particle physics, which may cover tens of square meters, a solution must be found with a manageable number of electronics channels and low total power consumption on the readout electronics without degrading the system timing resolution. We present here the design of a transmission-line readout for a Photonis Planacon MCP-PMT that has these characteristics. The tube, which is 5 cm square, is characterized by signal pulse rise times in the order of 200 psec and transit time spreads (TTS) in the order of 25 psec\cite{1, 2}. The model 85011-011 MCP has 1024 anode pads laid out in an array of 32 by 32 on the back of the tube. The proposed readout is implemented on a Rogers 4350B printed circuit board with 32 parallel 50-ohm transmission lines on 1.6 mm centers, each traversing one row of 32 pads. The board is connected with conductive epoxy to the 1024 anodes of the tube, each transmission line being read out on each end.

We have simulated the electrical properties of the transmission-line readout board with Hyperlynx and Spice simulators. The simulations predict that the readout transmission-lines can achieve a signal bandwidth of 3.5 GHz, which should not significantly degrade the time and spatial resolutions intrinsic to the MCP-PMT signals.

I. INTRODUCTION

The typical timing resolution in large time-of-flight detector systems in high energy physics experiments has plateaued at approximately 100 psec \cite{3, 4}. This is set by the characteristic difference in light collection paths in the system, which in turn is set by the transverse size of the detectors, characteristically in the order of one inch (100 psec). To do significantly better requires building detectors covering tens of square meters with variations in the length of signal path appreciably less than 1 mm, and electronics systems to read them out with long-term stability \cite{5, 6}. Commercially developed MCP-PMT tubes with micro-channel diameter size (pore size) of 2 micron to 25 microns, which achieve an output pulse with rise time in the order of 200 psec and transit time spread in the order of 25 psec, could offer a possible solution, using Cherenkov light generated at the MCP face as a relativistic particle traverses the detector.

Recent measurements have achieved time resolutions on the order of 6 psec using commercial tubes \cite{3, 4}. However, the output signals of commercial tubes are collected by a large number of discrete anode pins or pads, typically from 64 to 1024. For instance, the Burle/Photonics model X85011 tube, which is 2 x 2 inches overall, has 32 x 32 anode pads. If we readout each anode pad individually, we require 1024-channels of readout electronics. The challenge is not only to find a solution that retains the tube’s intrinsic fast-timing performance, on the order of a few picoseconds, in large scale detectors, but also to have a manageable number of readout channels and low power consumption.

II. TRANSMISSION-LINE READOUT BOARD

Achieving a very fast rise time signal in MCP-PMT outputs is essential for good timing performance. With commercial tubes, pore size, anode pad size, and the number of anodes have been defined by the manufacturers. However if one buys tubes with bare anode pads, one can design ones own readout boards to
reconfigure the outputs to meet the application requirements.

As shown in Figure 1, Burle/Photonics’ custom X85011 tube has 32 x 32 anode pads on the back. Each pad is 1.1 x 1.1mm, with a pitch of 1.6mm. Our goal is to design a readout board using fewer channels of electronics to readout all 1024 anodes of the tube without significant degradation of tube’s fast timing performance.

![Figure 1: View of 32 x 32 anodes on the back of Burle/Photonics’ tube X85011.](image)

Figure 1: View of 32 x 32 anodes on the back of Burle/Photonics’ tube X85011.

Figure 4 shows a prototype of transmission-line readout board designed to adapt for Burle/Photonis tube X85011.

![Figure 4. The transmission-line readout board which ties 32 anodes pads in a row, the signals being readout at both ends of the line.](image)

Figure 4. The transmission-line readout board which ties 32 anodes pads in a row, the signals being readout at both ends of the line.

The transmission-line readout board is implemented on a Rogers 4350B printed circuit board with 32 parallel 50-ohm transmission lines on 1.6 mm centers, each traversing one row of anode pads on the back of the tube. Each transmission line is being readout on each end. With this transmission-line readout board, one 1024-anode tube only needs 64-channel readout electronics.

III. MODELING AND SIMULATION OF TRANSMISSION-LINE READOUT

The transmission-line readout board can present excellent analog bandwidth to incorporate with the fast signals from the tube. Figure 5 shows interconnections between the transmission-line and 32 stub-loaded anodes pads.

![Figure 5: 32 anodes on the back of the tube are stub-tied evenly in a row within 2-inches in the middle of 4-inch transmission-line on the readout printed circuit board.](image)

Figure 5: 32 anodes on the back of the tube are stub-tied evenly in a row within 2-inches in the middle of 4-inch transmission-line on the readout printed circuit board.

Each anode pad contributes a ~100fF capacitance to the line. The lossy transmission-line model in the simulation was extracted from a layout of the printed circuit board by Hyperlynx.

![Figure 6: Equivalent schematic of simulation on signal integrity for transmission-line readout board.](image)

Figure 6: Equivalent schematic of simulation on signal integrity for transmission-line readout board.

The simulation of signal integrity was setup with the equivalent schematic shown in Figure 6. The input signal can be applied on any of the 32 anodes in the simulation.

Figure 7 shows the simulation result of signal integrity. A input force with 100 psec rise time is applied to pad #16. The green is the input pulse on pad #16; the red is the output pulse at the left end; the blue is the output pulse at the right end. The expected 9.6ps time delay was observed over a 1.6mm length difference between left and right with the velocity of ~0.55c on the PCB. The simulation shows that the transmission-line presents an analog bandwidth of 3.5GHz, well-matched to the signal bandwidth from a tube with a rise-time of 100 psec. The observed reflecting ringing on the output pulses are caused by impedance discontinuities over the transmission line. Because the 32 stub-loaded capacitance in the middle of the line results in a slightly lower impedance than 50-ohm.
Figure 7: Simulation result of signal integrity on the transmission line with 32 stub-tied anodes. The input force with 100ps rise time is applied to pad #16. The green is the input force; the red is output waveform at the left end of the line; the blue is the output waveform at the right end of the line. The line is designed with 50-ohms and terminated at each end.

In order to avoid stub capacitance over the transmission-line, we propose to design a transmission-line anodes being directly incorporated to the tube in the future. Since there is no more stub capacitance coupled onto the transmission line, the problem of impedance discontinuity can be solved.

Figure 8 shows the simulation result of transmission-line anodes without stub-tied anode pads, the output signals on each end can be well-terminated. No reflection has been found on either side of the line in the simulation.

Figure 8: Simulation result of transmission-line without stub-tied anodes. The input force with 100ps rise time applied to pad #16. The green is the input force; the red is output waveform at the left end of the line; the blue is the output waveform at the right end of the line. The line is designed with 50-ohms and terminated at each end.

Figure 9: A diagram of transmission-line readout system using fast sampling circuits, aimed to achieve a one to few picoseconds timing resolution.

IV. TRANSMISSION-LINE READOUT ELECTRONICIS

Depending on the system requirements, the transmission-line anodes can be readout in a number of different methods. Figure 9 shows a system aimed to achieve a one to few picoseconds timing resolution.

The readout system described above is based on fast sampling techniques. Comparing to the widely used timing measurement electronics in high energy physics experiments such as leading edge discriminator and time-to-digital converter (TDC); multi-threshold discriminator and TDC; constant-fraction discriminator and time-amplitude and ADC; the fast sampling system up to 40GS/s can achieve better timing resolution [7]. With pulse sampling system, a 40GS/s custom designed sampling circuit can be employed to record pulses from both ends of the transmission lines. An additional precision system reference clock may be used as timing calibration.

Transmission-line readout can give timing, spatial and energy information with the same data recorded by sampling circuits. For instance, a photon causes an electron avalanche in the tube; this group of electrons is collected at the time t0 at a point of the transmission line. The collected charge induces a corresponding electric pulse which propagates to both ends in a delay time of t1 and t2 respectively. The voltage waveforms on each end can be recorded by the fast pulse sampling chips. We can process the recorded pulses to precisely find t1 and t2. The “mean-time”, which presents the particle striking time t0 can be calculated by summing t1 and t2 then divide by 2; the location hit by the particle can be obtained by taking a
difference between t1 and t2. In addition, the integration of total charge collected on both ends represents the energy.

V. CONCLUSION

The ultimate goal in the front-end electronics is to develop a custom ASIC that incorporates fast sampling of the MCP pulses for transmission-line readout. This design is in progress. As an intermediate step, we will test the transmission-line architecture using a 40GS/s digital oscilloscope as well as Ortec NIM module constant-fraction discriminators and time-to-digital converters having approximately 3 psec resolution. The system will first be tested using the Argonne laser test stand.

REFERENCES


Abstract

The size and complexity of the latest generations of FPGAs has increased dramatically. This in turn means that the time taken to develop and build even small firmware projects is increasing exponentially. Pre-constrained logic placement and routing are becoming critically important for the use of specialized components in the FPGA such as serial link interfaces. This necessitates significant changes from 'normal' firmware tool flows in order to effectively develop systems based on these devices.

In this paper we discuss several methods for improving turnaround speed and design safety, including: pre-placed and pre-routed hard macros / Relationally Placed Macros (RPMs), and pre-synthesised black-box netlists. Possible methods of dynamic partial reconfiguration are also discussed in this context.

I. INTRODUCTION

The current CMS trigger and DAQ electronics are largely based on FPGA and processor technology several generations behind the currently commercially-available devices. Most systems in CMS are based on either the Xilinx Virtex-II or the Xilinx Virtex-II Pro (and similar Altera-made FPGAs). Since then Xilinx has developed the Virtex-4 and Virtex-5, scaling in feature size from 250nm to 65nm and incorporating many new hardware features such as Digital Signal Processing (DSP) cores, tri-mode Gigabit Ethernet (GbE) MACs and PCI express (PCIe) endpoints amongst others. Furthermore, total logic capacity has increased approximately ten-fold with a corresponding increase in maximum clock speed.

However this creates a new problem: FPGA firmware synthesis and routing, being an NP-hard problem, is an extremely computationally-intensive process. Given the arrangement of logic and routing in the devices and the scaling of feature size in deep submicron technology, the complexity of logic placement and routing is increasing at a greater-than-geometric rate. Without the development of new firmware development techniques to manage this increase in complexity, firmware build times can increase from minutes to hours and even days.

Compounding these issues are limitations in the performance of the available development tools. In particular, when using certain advanced features of the device, the behaviour of the design and performance may change significantly. In the worst case a new revision of a previously working design can cease to function after minor changes are made to the design [1].

II. FPGA TOOL FLOWS

A. Standard Xilinx FPGA Tool Flow

A typical Xilinx tool flow might proceed as follows:

- **Synthesise** a design from either VHDL or Verilog (or both). This may be achieved using either vendor-specific tools such as Xilinx's XST or Mentor Graphics' Precision Synthesis. The end product is a Look-Up Table (LUT)-level netlist. At this stage proprietary IP cores may also be introduced.
- **Translate** a LUT-level netlist into a device-specific format and combine it with user-defined constraints. These can also be included as device-specific attributes in original VHDL or Verilog. At this point any black-box components must also be included, such that the design is complete once translate has finished.
- **Map** the logic component of a design into place in the device. This process uses a coarse timing definition to place the components.
- **Place and route** the design using a precise timing model for the device, including temperature dependency.
- **Generate** a device programming file that can be downloaded into the FPGA.

This tool flow will always provide the best implementation, although it may take several iterations as part of the process involves a pseudo-random search. Ultimately it is impossible for the tools to test every permutation of design that will fit in the FPGA, so this is a necessary step, but it also implies that an undefinable amount of time will be taken to achieve timing closure. In large, complex designs, the turnaround time is growing rapidly, from minutes to hours and even days.

In order to reduce this turnaround time, there are various techniques that can be adopted. The key requirement is to avoid repeatedly processing unchanging components of a design every time a minor revision is made. There are several ways to achieve this.

B. Pre-Synthesised Netlists

The simplest (and most generally-applicable) approach to speeding up a firmware build is to use the same method used for pre-built IP core generation. This involves synthesising a core component of the design that doesn't frequently change, and then integrating it into the full design at a later stage. This approach has few limitations, but can only speed up the first stage of the build process.
The only required change compared to normal synthesis is to turn off pad instantiation. This prevents the tools from inferring the top-level ports as FPGA pins. The output is an ngc/edf file that can be re-imported during a normal build. The file name and ports must also match those in the component definition of the main design.

C. Post-Place/Route Macro

A more advanced technique involves taking a sub-component of the design, then synthesising, placing and possibly routing it. The placement of the component must also be defined as a constraint. The end product is known as a Relationally-Placed Macro (RPM), a logic and routing template that must have a fixed location in the device.

Unlike the creation of a pre-synthesised netlist, the creation of an RPM is not a completely automated process. Firstly, the connections must be defined between the macro and the outside world, and timing constraints must also be carefully set. When the design is created it must be ensured that all timing requirements can be satisfied in the final design as well, because once the macro is built it cannot be changed by the tools. Secondly, part of the process involves using FPGA Editor to directly convert the design, strip out unused wiring and logic and define the macro ports.

RPMs can either be designed directly at the hardware level using FPGA Editor, or converted from a placed (and possibly routed) design. The first of these processes is completely manual. The second one involves taking an automatically-generated design and removing unwanted nets. This can be partly automated using a script but the initial macro generation must be done by hand. It is also necessary to prevent the removal of logic from the design that is optimised away by the tools. This involves turning off logic trimming during map.

Unfortunately, Xilinx RPMs have several limitations: firstly, a placed macro cannot use any FPGA blocks that connect to modules that are also externally connected on the device (the tools currently do not 'understand' what this means). An example of this includes the gigabit transceivers.

Routing can also be included in a macro, however unfortunately, creating a routed RPM can crash the Xilinx tools and is therefore not recommended. Unless the design has a very specific layout that's required for optimal behaviour, it is better to not use RPMs but instead use guided place and route, where the tools will use a previous build as a reference for the new one.

D. A Bus Macro Example

As an example, one can consider a simple pass-through bus macro. Bus macros are commonly used to pass signals between static and reconfigurable firmware modules in a design (see section III). In order to do this one must create a pass-through LUT which acts as a buffer connected to another on the other side of the design. One can then divide the design where the routing crosses a logic boundary to create a boundary interface where the logic never changes.

Figure 1 shows a LUT-level view of the macro in a Virtex 5. Only one of the inputs is used per 6-LUT as it is simply buffering the input signal to the output. This macro also includes a register on the output (although this is optional).

E. Constraint-Based Placement and Routing

In order to avoid the limitations of hard macros, one can use the Xilinx User Constraints File (UCF) to force the tools to use particular CLBs and routing connections for a given component of a synthesised design. This does however require a non-standard step and involve large constraint files. One generates the constraints in much the same way as an automatically-generated hard macro, with one significant difference: instead of creating a macro design and re-inserting it during the translation phase of the firmware build, one
exports the placement and routing constraints to a UCF. This can then be re-imported during standard firmware build.

This does however require an exact name match between the net and logic names in the new build and the one from which the constraints were originally generated. This is in fact rather difficult as the tools hierarchically-optimise the firmware, and so it's possible for changes in different components of the design to stop this from working. The solution is to pre-build the component corresponding to the constraints as a LUT-level netlist. The tool flow will then be forced to keep the names that were present in the original design.

In spite of the complexity of this process, it ultimately allows one to pre-constrain a portion of a design precisely. This leads to the possibility of modifying one component of a design while keep others completely static, allowing for dynamic reconfiguration.

III. DYNAMIC PARTIAL RECONFIGURATION

Dynamic partial reconfiguration is the process by which one can pre-place and route part of a design while changing another component depending on the demands of the system. It has many uses, in particular being used to reduce the required device size by configuring for two mutually-exclusive modes of operation (e.g. an encryption core where one chooses between DES/AES). It is also useful when there's no access method to modify the device's configuration apart from the device itself. Xilinx FPGAs contain an Internal Configuration Access Port (ICAP) which has all of the capabilities of the external configuration interfaces.

Xilinx FPGA programming can be broken down into 'frames', which represent the smallest configuration unit of the device. These frames can also be changed without powering down the device. In Virtex FPGAs, it is possible to modify a portion of a frame without disrupting the configuration of the rest of the frame. The only complication this creates when considering partial reconfiguration is that the FPGA's master reset does not occur for the logic's initial state, so every component in the firmware must contain an explicit reset circuit.

If one reads Xilinx documentation on partial reconfiguration, it will describe two processes: difference-based reconfiguration and module-based reconfiguration. These will first be briefly discussed, followed by an alternative method that uses constraint-based placement and routing.

A. Module / Difference-Based Reconfiguration

Difference-based partial reconfiguration is the simplest technique available. It involves editing the design in Xilinx FPGA Editor and simply re-saving the design. One can then use the Xilinx configuration file generator bigen to create a file containing the difference between the two firmwares (using the '-r' flag). As such it is useful when the design changes are very small but it is not generally useful.

Module-based partial reconfiguration uses area constraints to segregate a static portion of the design from the dynamic component (see figure 3). As such it splits the design into regions, where a bus macro is used to cross the boundaries between the different parts of the design. Figure 4 shows an example of this where the static component of the design is on the left and the dynamic component of the design is on the right. This process unfortunately requires the splitting of the bitstream into components, thereby requiring custom build steps, some of which are not supported in the latest tools or require special patches.

Figure 3: An example from the Xilinx online documentation of module-based design. Note the use of bus macros to traverse the boundaries between configuration regions.

Figure 4: An example of module-based reconfiguration [4]. The left component of the design is a static microprocessor core. The right component is a reconfigurable AES core. Note the boundary between the devices is marked by a bus macro.

B. Constrained Reconfiguration

Using constraint-based firmware builds presents an alternative approach to the generation of partial reconfiguration firmwares. In this approach one uses loose area constraints to place a static firmware on one part of the design. This component contains a bridge to the ICAP inside
the FPGA, and a secondary interface for interfacing to the reconfigurable firmware. In addition there is a bus macro used to create an interface port in another portion of the design. By exporting the routing and logic of this design as a constraints file, new firmwares can be generated by simply feeding the constraints into the new design. The only other requirement is that the static component of the firmware is not changed, otherwise every related design must be rebuilt. The partial configuration bitstream can then be generated using the same method used for difference-based reconfiguration. The major advantages of this technique are that there are no arbitrary region constraints and that bus macros are not explicitly needed. Static and dynamic firmwares can even be interleaved.

C. A Virtex-5 Floating Point Multiplier

As an example, consider the following. Figure 5 shows an initial configuration providing a GbE connection via a Xilinx MGT and a bus bridge in the lower part of the FPGA. However nothing is connected to the bus in this firmware.

![Figure 5: A simple static configuration firmware. Note the bus macro in the middle of the lower portion of the design.](image)

Figures 6 and 7 show more developed firmwares with multiple DSP cores (the first is a double-precision multiplier, the second a double-precision square). The interesting feature of these designs is that the firmware interleaves with the original static firmware, allowing better use of FPGA resources than in module-based reconfiguration.

![Figure 6: A more complex firmware with a double-precision multiplier connected to the bus in the lower part of the FPGA.](image)

![Figure 7: A two-multiplier firmware interleaved with the original static firmware.](image)

IV. CONCLUSIONS

There are many ways in which one can improve turn-around time and reliability of firmware builds. Pre-built netlists offer a safe and reliable way of accelerating turnaround, while hard macros have some additional benefits. Unfortunately there are reliability issues with these processes in the current Xilinx tools. Constraint-based design can be used as a work-around until the tools implement hard macros in a more reliable manner.

Partial reconfiguration is an extremely useful tool in some applications, and can be largely automated. There are many caveats but for a certain class of applications the benefits of dynamic firmware modification outweigh the difficulty in its implementation.

V. REFERENCES


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