Serial Powering of Silicon Strip Modules for the ATLAS Tracker Upgrade

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Abstract

The costs, difficulties and inefficiencies associated with the cabling of silicon detector systems are well known. Serial Powering is an elegant solution to these issues and is being actively pursued by the ATLAS Tracker upgrade community.

Demonstrator supermodules have been produced using the ABCD3TA chip from the present ATLAS SCT together with serial powering circuitry built from commercial components. Two 6 module supermodules have been built, and construction of a third supermodule to a 30 module design is in progress. Recent results from these supermodules will be presented.

I. INTRODUCTION

In the current generation of silicon detector systems for particle physics experiments, it has generally been considered best practice to power each detector module independently. For example, the present ATLAS SCT detector uses 4088 independent power supply channels and cable chains, one for each detector module. Physically routing the cables into the detector volume can be a major challenge in itself, and with return path cable resistances of order 4.5 ohms power efficiency is generally poor due to thermal losses in the cables [1].

Independent powering is not a practical solution for future detectors, where the total channel count may be expected to increase by a further order of magnitude. The ATLAS Tracker upgrade community is actively pursuing the serial powering alternative [2, 3]. For chains of many modules with identical power requirements, serial powering offers potentially higher efficiency and lower mass than the use of DC-DC converters. An overview of tracker power distribution R&D is given in [4].

With serial powering, a number of detector modules are connected together in series to a constant current source. Each module has its own shunt regulator and power transistor combination to provide digital power and, as low power front end amplifiers typically operate at a lower voltage than their digital back ends, a linear regulator is used to provide analogue power. Each module will now be at a different potential with regard to the off detector readout electronics, so it is also necessary to provide AC or opto-coupling for all clock, command and data signals.

Demonstrator "supermodules" have been produced to two designs using the ABCD3TA chip from the present ATLAS SCT together with serial powering circuitry built from commercial components. Looking ahead, elements of the serial powering scheme have been incorporated into new, radiation hard, custom integrated circuits: the ABCN readout chip and the SPI serial powering chip. These developments and their application to future demonstrator supermodule will be outlined.

II. SIX-MODULE STAVES

Demonstrator staves have been made based upon a design for the Run IIb upgrade of the Collider Detector at Fermilab (CDF) [5]. Two such staves were built, one at LBNL and one at RAL. The stave assembled at RAL is shown in figure 1.
The mechanical stave, a carbon fibre and foam sandwich with embedded PEEK cooling tubes, was designed to support six silicon detector modules of detector dimensions 96.4 by 40.6 mm, the readout electronics being glued directly onto the detector surface. The silicon detectors have p-in-n strips of 75 μm pitch and, in common with the support staves, were spare components from the CDF Run IIb project. A new flexible bus cable with copper tracking and an aluminium screen layer and a new thick film hybrid were designed at LBNL and a companion serial powering board was designed at RAL. The resultant bus cables, hybrids and serial powering PCBs were all sourced from commercial vendors.

Each module comprises a silicon detector, the hybrid with four ABCD3TA [6] chips and the serial powering board. Both the hybrid and serial powering board are glued directly on top of the silicon sensor, and the resulting assembly is tested standalone before being glued to the stave. Communication with the modules utilises a number of LVDS signals passed down the bus cable: multi-drop clock and command buses which service all modules and six, single-drop data buses, one for each module. As each hybrid in the serial chain sits at a different potential with respect to the ground of the readout system, the LVDS signals are AC-coupled on each serial powering PCB. To facilitate better comparison between hybrid and module noise figures, a bare hybrid was mounted at one position of the pictured stave.

Early results from the RAL stave showed evidence of pickup between the detector bias traces on the bus cable and the silicon strips but, after a noisy high voltage supply had been eliminated from the test system, the results shown were obtained.

Figure 2 shows the gain of each channel of the stave. The channels of each module are shown in a different colour. Figure 3 shows the output noise of each channel of the stave. In addition to the bare hybrid placed at position 4, it can be seen that a number of channels were deliberately left unbonded at the first position. The bonded channels return of order 1100 ENC and the unbonded channels 600 ENC. These figures are in agreement with the expected performance of the ABCD3TA chipset, and the absence of spikes demonstrates that there is no pickup from the bus cable.
Additional studies were performed in which noise currents were injected directly into the serial powering chain, but no effect was noted upon the operation of the detector modules. Similarly if one module is left unbiased, the performance of the remainder of the serial module chain is not degraded. The first serially powered chains of silicon microstrip detector modules were found to operate cleanly under all tested circumstances.

### III. THIRTY-MODULE STAVES

The next stage in the development chain was chosen to be the preparation of a thirty-module stave of dimensions more representative of the needs of the ATLAS tracker upgrade. For this project, a new thick film hybrid, bus cable and stave were designed by Carl Haber of LBNL.

The hybrid is shown in figure 4. At the top of the image there are six ABCD3TA readout ASICs. Along the bottom edge six smaller, commercial ICs may be seen: toward the left are three LVDS transceiver chips used as part of the AC coupling scheme for clock, command and data signals; toward the right are the analogue regulator, digital regulator and shunt transistor at the heart of the serial powering circuitry. In a final implementation the data AC coupling would be placed off hybrid at the end of a stave, and the remaining commercial ICs would be replaced by a single custom, radiation hard die with an estimated footprint of order ten square millimetres (see Section IV).

From figure 4 it may also be seen that the present circuit uses several large ceramic capacitors, six of which form part of the AC coupling circuitry. The size of these components is driven by the desire to build a stave of 30 modules each running at 4.0V, hence each coupling capacitor needs to be able to withstand a little more than 120V. In the final solution, using a smaller number of hybrids each running at lower voltage of 1.2 to 1.5V, the real estate needed for the coupling capacitors again will be considerably reduced.

Due to limitations imposed by the number of address pads available on the ABCD chip, the thirty-module bus cable provides six differential command buses, one to each group of five hybrids. Three differential clock signals are available, but there is also an option to use a single clock bus. The present bus cable is actually made in two sections connected together by wirebonds: vendors that can make the necessary length in one piece have subsequently been identified.

Before proceeding to the construction of the thirty-module stave, a “test vehicle” was assembled comprising thirty hybrids attached to a bus cable, but mounted on a copper clad board in place of the carbon fibre stave. The resultant thirty hybrid assembly, recently completed at LBNL, is shown in figure 5. This has provided a valuable tool for the study of signal propagation along the bus cable, and has led to small revisions being made to the communication scheme.

Work to populate the thirty-module stave continues. Figure 6 shows the stave when five modules had been mounted upon the support structure: at the time of writing a total of seven modules have now been mounted and operate reliably together. A preliminary result showing the input noise of all channels of one module operated on the serially powered stave is shown in figure 7. Although the programme has not yet been completed, to date the modules have been shown to perform in accordance with expectations.

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Figure 4: Thick Film hybrid for six ABCD3TA chips with integrated Serial Powering circuitry.

Figure 5: Thirty Module Stave “Test Vehicle”: thirty six-chip hybrids with integrated Serial Powering circuitry (without sensors).
IV. FUTURE DEVELOPMENTS

The use of custom integrated electronics in place of commercial discretes is crucial to the further development of the serial powering concept. To this end, several mature designs have been submitted for fabrication including the ABCN silicon strip readout chip [7] and the Serial Powering Interface (SPI) chip [8]. At least three different serial powering architectures have been identified with differing locations for the shunt regulator, power transistor and linear regulator components. These elements have been incorporated into the ABCN and SPI chip such that a fair comparison may be made of the performance of all three schemes. Studies will continue, in part, by construction of a further prototype stave using kapton hybrids together with ABCN and custom serial powering circuitry together with n-in-p short strip sensors to ATLAS upgrade specifications. A first prototype of a custom constant-current source has recently been produced [9] which will be made available to power this and future staves, into which protection and monitoring features will be incorporated.

V. SUMMARY

Serial powering is an attractive concept for the powering of the upgraded ATLAS tracker, offering significant reductions in both power loss and material budget compared with other powering schemes. Staves have been built which have successfully demonstrated the application of serial powering to silicon strip detector modules, including the AC coupling of digital signals, with noise levels in agreement with individually powered modules of similar design.

Custom ASICs suited to the ATLAS tracker upgrade development programme have recently been submitted for fabrication, and will enable more fully integrated, serially powered staves to be produced. Studies of system features such as protection and monitoring schemes are now underway. Serial powering remains a most promising choice.

VI. REFERENCES

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[9] Private Communication, J. Stastny, Prague, Academy of Sciences of the Czech Republic