PRELIMINARY TEST OF A FOUR-CHANNEL TTL HYBRID INTEGRATED CIRCUIT FOR MULTIWIRE PROPORTIONAL CHAMBERS

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ABSTRACT

A thick film hybrid integrated circuit has been designed to fit the needs of the SPMD proportional chambers. The results of preliminary tests on few four-channel prototypes are discussed; several modifications will be necessary before a final configuration can be obtained, but the main goals have been achieved already in the prototypes.
1. INTRODUCTION

The basic electronic circuit to be used in connection with the multiwire proportional chambers (MWPC) of the Split Field Magnet Detector consists of a sense amplifier, a delay, and a gated memory. An attempt has been made to implement the required function, using standard mass-produced integrated chips mounted on a ceramic substrate (thick film hybrid). The main advantages of such a technique, as compared to a complete monolithic integration, are as follows:

- there is the possibility of full breadboard test of the circuit, before the integration, using discrete elements;
- internal capacitors and resistors can be used, and the resistors can be trimmed with a typical 1% tolerance;
- there is reasonable development and prototype costs.

The present report describes a hybrid four-channel module realized by Marconi-Elliot Microelectronics*, using TTL integrated circuits. At present, twelve four-channel prototypes have been delivered and partially tested.

2. DESCRIPTION OF THE CIRCUIT

The electronics layout of the four-channel circuit can be seen in Fig. 1, and Fig. 2 shows a complete module and an uncovered one. The external dimensions of the modules are 1" × 2", and they are mounted in a dual-in-line 40-lead package. All components of the package (leads included) are non-magnetic, in view of our particular application into or very near a strong magnetic field. For historical reasons, the prototype circuits do not have the memory latch (it was foreseen that the module would be connected to another complex unit including the read-out facility). The finalized circuit, see Section 5, will include the memory; no problem is expected because of this modification (all difficulties should lie in the linear part). Each channel consists of three integrated circuits, plus an RC timing constant for the one-shot; the resistor is automatically trimmed by the manufacturer to get the correct input to output delay. A prompt output is also available (Fast OR), and threshold and delay can be adjusted externally with a reference voltage.

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3. MEASURED PERFORMANCES OF THE CIRCUITS

The input terminating resistors $R_1$ were not introduced into the module at this stage, so that we could optimize their value in connection with a proportional chamber. A big value of $R_1$ means larger signals, but also a smaller repetition rate; we found 2 kΩ to be a good compromise. The basic input circuit is:

For $R_1 = 2$ kΩ, $V_{REF} = 300$ mV, the typical range of values of $R_2$ that allow the same threshold to be obtained on all channels is 15 to 30 kΩ. The spread is due to the different offset of the amplifiers. In a finalized module (see Section 5) both resistors would be internal, and automatic trimming of $R_2$ will generate the threshold value.

The timing constants $R_D C_D$ are already internal, and $R_D$ was trimmed by the manufacturer to get the required value and tolerance of the delay.

A summary of the main measured parameters is given here, based on the results obtained on eight measured channels:

- Minimum input threshold for safe operation of all channels (on 2 kΩ): $-4 \pm 1$ mV *).
- Temperature dependence of threshold (10 to 50°C): 50 µV/°C.
- Propagation delay Input-Fast OR: given in Fig. 3, as a function of the input pulse amplitude, for different values of threshold.
- Temperature dependence of the propagation delay Input-Fast OR (10 to 50°C): 0.1 nsec/°C.
- Total spread of the propagation delay Input-Fast OR for all measured channels at a fixed input pulse: ±5%.
- One-shot delay, input to trailing edge of monostable pulse (at 25°C): 300 ± 9 nsec.
- Variation of delay allowed by the reference voltage $V_D$: about ±50 nsec around the nominal value to keep a good matching between channels (see Fig. 4).

*) Obtained with a 5% trimming on each channel of the resistor $R_2$. 
- Temperature dependence of the delay Input-Trailing edge of the one-shot (10 to 50°C): 0.05 nsec/°C.
- Power dissipation of the four-channel module: min 900 mW, max 1100 mW.

In Fig. 5, the typical one-shot output pulse (available on a test pin in the prototype) is shown, as well as the output of the edge differentiating circuit.

The channels are insensitive to positive inputs as large as 1 V, of any shape and length (complete d.c. coupling).

The only problem was found to be the cross-talk immunity. A 40 dB protection was required, meaning that with a -5 mV threshold no channel should respond when all the adjacent ones are pulsed with a -500 mV input. Owing to a defective internal layout design (an output line too near to an input line on channel 4), only three channels in the module satisfy the requirement. This mistake could be easily corrected in the event of future production*).

4. MEASUREMENTS ON A PROPORTIONAL CHAMBER

The traditional time resolution and efficiency measurements have been realized in a standard MWPC, whose main parameters are summarized in the following table:

<table>
<thead>
<tr>
<th>Table 1</th>
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<tr>
<td>Active dimensions: 38 x 38 cm²</td>
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<td>Sense wires: 20 μm W, Au-plated, 2 mm apart</td>
</tr>
<tr>
<td>HV electrodes: 100 μm Cu-Be wires, 1 mm apart</td>
</tr>
<tr>
<td>Gap: 8 mm</td>
</tr>
<tr>
<td>Gas filling: 0.5% freon, 24.5% isobutane, 75% argon (magic gas)</td>
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</table>

Eight wires were connected to the hybrid electronics, and the efficiency plateau was made using a ⁹⁰Sr collimated β-source in coin-

*) Inclusion of an internal decoupling capacitor in a new set of prototypes has completely solved the problem. As much as ten four-channel modules have shown a minimum cross-talk immunity of 50 dB.
Figure captions

Fig. 1: Electronic layout of the four-channel hybrid prototype. A gated edge differentiating circuit provides the delayed pulse on DOut. In a finalized version (see Fig. 8) this last section will be replaced by a flip-flop memory. Typical values of components are:

\[ R_0 = 1.5 \text{ k}\Omega, \quad R_D = 10 \text{ k}\Omega, \quad C_D = 65 \text{ pF}. \]

Fig. 2: One uncovered and one complete four-channel module are shown. The substrate dimensions are 1" \times 2".

Fig. 3: Propagation delay Input-Fast OR as a function of input overdrive (in dB over threshold) measured for three values of threshold.

Fig. 4: Range of regulation of the one-shot delay. The nominal value of 300 nsec is obtained for \( V_D = V_{CC} = 5 \text{ V} \).

Fig. 5: One-shot output pulse (a), and Delayed Output (b) for a channel; the time scale is 100 nsec/cm in both cases, and the input pulse -7 mV high.

Fig. 6: Efficiency plateau of the chamber described in Table 1 as a function of the HV. The Fast OR output of eight wires was coincided with a 60 nsec gate generated by scintillation counters. The nominal threshold on the eight channels was -5 mV.

Fig. 7: Time jitter of the chamber for fast electrons and at 5.7 kV as given by the Fast OR output of eight wires. The time scale is 20 nsec/cm.

Fig. 8: Possible finalized version of the four-channel hybrid circuit. The same general performances are expected, since the only modifications are to the logical output structure.
Fig. 3
Fig. 4
H: 100 nsec/cm
V: 5 mV/cm (inputs) and 1 V/cm (outputs)

Fig. 5
Fig. 6

Fig. 7