ATLAS Insertable B-Layer

Michal Marcisovsky
Institute of Physics, Academy of Sciences of the Czech Republic

on behalf of the ATLAS Collaboration

**Introduction**

For the sLHC phase I, the ATLAS detector will be upgraded by the installation of one additional Pixel Detector layer. The new layer will be inserted between the B-layer of the existing pixel detector and a new smaller radius beam-pipe. This upgrade requires development of several new technologies to cope with increased radiation doses to which apparatus will be exposed, significant rise of the particle flux density to be detected, and further improvement of the detector physics performance. One of the means to achieve these goals is significant reduction of the pixel size, use of the deep sub-micron technologies for the read-out chip fabrication, novel materials for the stave construction, advanced methods for detector cooling etc. In the present phase of the projects some key components are being developed in several options.

**Present status & requirements**

- The existing B-Layer will gradually lose efficiency due to radiation damage to sensors and chips
- Removing the present B-Layer was found not to be feasible
- Critical material budget leads to the:
  - Sensor thickness < 250 µm or 0.32% X₀
  - Light mechanical support
  - Radiation hardness 5 x 10¹⁰ n/cm²

**Insertable B-Layer**

- IBL will take over the role of the present B-Layer for the LHC high luminosity running
- Minimizes the changes to the minimum from the present system and fully integrates into the present Pixel detector
- IP resolution is 60 µm in Z, 7 µm in R (around 40% improvement over current setup)
- Light jet rejection improves by a factor of 2, B-tagging
- IBL is a technological step towards the sLHC (improved FE IC, advanced radiation-hard sensors, faster readout)

**IBL sensors**

- Have compatible sensor design for different technologies. (FE requirement)
- There are 3 variants presently being studied:
  - Planar Si
  - 4.7” 6” wafers
  - N/P type
  - Proven technology
  - 3D Si
  - Good charge collection
  - Active edge
  - Low operating voltage
  - CVD Diamond
  - No leakage current with irradiation
  - No cooling issues

**IBL chip FE-I4**

- Biggest chip in HEP to date (19.6 mm x 20.1 mm)
- Lower power
- Increased radiation hardness
- Able to take higher hit rate
- No need for extra module control chip
- Sensor bump-bonded to the FE chip

**IBL stave R&D**

- Supports single or multi-chip modules
- Carbon foam support
- Carbon fiber / Ti pipes
- 2 basic types in consideration
  - Monostave -> prototyping in progress
  - Bi-stave
- Main challenges
  - Minimize amount of material
  - Low temperature gradient
- Cooling, CO₂, or C₂F₆
- Possibility of integration into existing system
  - Pmax ~ 1.5 kW

**Installation & access**

- Beam Pipe extraction & installation of IBL is complicated by:
- Activation of surrounding area
- Very little access to beam pipe and long lever arm (access is at z ~ 3.5 m)
- Minimizing risk to the present Pixel Detector

**Summary**

Number of key R&D tasks for IBL design and construction are in progress. The project is well advanced to meet project milestones, Technical Design Report in 2010 and detector installation for sLHC phase I.