Electronic Readout of the ATLAS Liquid Argon Calorimeter:
Calibration and Performance

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on behalf of the ATLAS Liquid Argon Calorimeter Group
LHC and ATLAS Performance

ATLAS Online Luminosity \( \sqrt{s} = 7 \text{ TeV} \)

- **LHC Delivered**: 9.1 nb\(^{-1}\)
- **ATLAS Recorded**: 8.35 nb\(^{-1}\)

### Subdetector Performance

<table>
<thead>
<tr>
<th>Subdetector</th>
<th>Number of Channels</th>
<th>Approximate Operational Fraction</th>
</tr>
</thead>
<tbody>
<tr>
<td>LAr EM Calorimeter</td>
<td>170 k</td>
<td>98.5%</td>
</tr>
<tr>
<td>Hadronic endcap LAr calorimeter</td>
<td>5600</td>
<td>99.9%</td>
</tr>
<tr>
<td>Forward LAr calorimeter</td>
<td>3500</td>
<td>100%</td>
</tr>
<tr>
<td>LVL1 Calo trigger</td>
<td>7160</td>
<td>99.8%</td>
</tr>
</tbody>
</table>
ATLAS Liquid Argon Calorimeter

S. Majewski

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Readout Electronics

**Goal:** Measure the energy in 182,468 detector channels over a wide dynamic range (tens of MeV – ~few TeV)

**Front-end electronics:**
- 1524 front-end boards read out + digitize calorimeter signals
- ~300 other boards (calibration, analog trigger sums, controllers, monitoring)
- 1524 fiber optic links (1.6 Gbps) to BE

**Back-end electronics:**
- 192 Read-out driver (ROD) boards provide digital filtering, formatting, and monitoring
- ~800 optical links to ATLAS DAQ

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Front-end Board Architecture

In this schematic block diagram of the FEB architecture, the data flow is shown for four of the 128 channels per board. The data comes from the detectors on the top left. The analog sums exit on the bottom left through the Layer Sum Boards (LSBs) while the digital results are transmitted to the next level of processing through optical transmitters (OTxs) on the right. If these were HEC channels, the preamps would be replaced by preshapers, as described in the text.

The shaped signals are sampled at the LHC bunch crossing frequency of 40 MHz by switched-capacitor array (SCA) analog pipeline chips. The SCAs store the signals in analog form during the L1 trigger latency. For events accepted by the L1 trigger, typically five samples per channel are read out from the SCA and digitized using a 12-bit Analog to Digital Converter (ADC). To optimize the precision of the energy measurement, the Gain Selector chips (GSEL) choose for each channel, in each event, which of the three gains to use, based on the value of the peak sample in the medium gain compared to two reference thresholds. The FEBs can also be configured to read out one or more fixed gains, a feature that is used for certain calibration runs. The digitized data are formatted, multiplexed, serialized, and then transmitted optically from each FEB to the corresponding ROD of the BE electronics.

The RODs, described in more detail in Section 7, perform digital processing of the samples for each channel to produce optimized measures of the energy. For channels passing an energy threshold, the time of the deposition and a “quality factor” are also calculated. For those channels passing a second (higher) threshold, the values of the raw samples are also written out, in addition to the results of the processing, to allow additional checks to be performed offline for large energy deposits. The quality factor, defined more precisely in Section 7, quantifies whether pulses match expectations or whether they may be mismeasured, for example from waveform distortions produced by energy depositions in neighboring bunch crossings, a phenomenon known as “pile-up.”

During development of the electronics, a partial FE system test was performed at Brookhaven National Laboratory (BNL) in 2004 using final prototypes of the various FE boards. Several configurations were tested, the largest of which corresponded to the setup required to read out one “half-crate” of the EMB (including 14 FEBs, one calibration board, and the associated trigger and control boards). This configuration included 1792 readout channels, corresponding to \( \approx \frac{144}{56} \) of the channels in the entire EMB, or \( \approx \frac{0.9}{2} \) of the total LAr calorimeter system. The purpose of the BNL test was to verify that the overall FE system met the required performance specifications, before launching production of the various boards. A similar partial system test of the BE electronics was performed at CERN in 2004.

**Preamp:**
97% warm; 3% cryogenic (hadronic endcap)
3 versions match detector capacitances / dynamic ranges

**Hadronic Endcap Preamp:**
mounted on the detector inside the cryostat
→ on the front-end boards, **preshapers** invert, amplify, and shape the signal
**Front-end Board Architecture**

**Shaper:**
3 overlapping linear gain scales (gain values: 1 low, 9.9 medium, 93 high)
fast bipolar shaping with $\tau = RC = 13$ ns

**Switched-capacitor Array (SCA):**
samples the shaped signals at 40 MHz (LHC bunch crossing frequency)
stores analog signals during L1 trigger latency (2.5 $\mu$s)
up to 32 samples for physics or calibration runs
Front-end Board Architecture

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**Events accepted by the L1 trigger (up to 75 kHz):**
digitized by 12-bit ADCs
Gain Selector (GSEL) chips choose gain for each channel based on peak value of each sample (in medium gain, compared to 2 reference thresholds)
data formatted, multiplexed, serialized, and transmitted optically
Readout Driver (ROD)

Input FPGA:
- parallelizes incoming data & verifies its integrity
- memory separated into 2 banks: 1 for writing incoming data, the other for data being read by the DSP

Digital Signal Processor (DSP):
- high performance: $5.7 \times 10^9$ instr/s
- stores DSP software, input and output data buffers, histograms, and calibration constants (packed in int formats)
- 1 DSP processes the data from 1 front end board (128 channels)
- energy, time, and quality factor calculations are performed on the DSP and have been validated

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Readout Driver (ROD)

**bandwidth limitations:**

**requirement:** 75 kHz, achieved w/ 5 samples read out
(currently reading out 7 samples)

**input:** determined by front end output and input FPGA (tested up to 157 kHz)

**output:** DSP computations and output data formatting (tested up to 85 kHz)

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**Figure 13.** An oscilloscope trace showing the time required for the various stages of the DSP processing of one event of FEB data, with five samples per channel. The time for each stage of the processing (between the pulses) is shown on the figure, while the labels are defined in the text.

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**DSP Processing Time for 1 Event**
(5-sample readout)

- energy calculation: (3.8 μs)
- histogram filling: (2 μs)
- time, quality factor calculation: (1.4 μs)
- checksum calculation: (0.9 μs)

**total:** 9.6 μs ~ 100 kHz

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Calibration runs are taken regularly and automatically processed

**Types of Calibration Runs**

- **Pedestal**: front end boards triggered and read out w/o input signal → determines pedestal value, noise (from RMS of pedestal)

- **Ramp**: fixed-amplitude calibration pulses injected (exponential before shaping) → determines gain of readout from slope of reconstructed pulse amplitude vs. DAC setting

- **Delay**: fixed-amplitude pulses injected; effective sampling rate of 1 ns → detailed study of signal shape
Noise Performance

- Typical noise levels: 30 – 50 MeV (EM); 100 – 500 MeV (HEC, FCal)
- Nominal pedestal value (∼1000 ADC counts) allows meas. of the pulse’s negative lobe (important for measuring drift time, effect of pile-up from earlier bunch crossings)
- Coherent noise, measured in situ: 2 – 6% of total noise per front end board (2 – 3% in second layer of EM → contains largest part of EM shower)
Pedestal and Noise Stability

* Stability of pedestal, noise, and auto-correlation monitored over extended periods of time (plots show a 6-month period in early 2009)

* \(\Delta\)Pedestal: \(\sim 0.02\) ADC counts / channel (\(\sim 1\) MeV for medium gain in EM, \(\sim 2\) MeV in HEC, \(\sim 10\) MeV in FCal)

* \(\Delta\)Noise: \(< 0.01\) ADC counts in EM high gain, \(< 0.02\) ADC counts in FCal (order of magnitude lower for medium, low gain)
Energy Resolution

\[ \frac{\sigma(E)}{E} = \frac{a}{\sqrt{E}} \oplus b \oplus \frac{c}{E} \]

- \( a = 10\% \) (stochastic term for EM shower)
- \( b = 0.25\% \) (constant term, dominates at high \( E \))
- \( c = 10 \text{ MeV} \) (noise from single sample, high gain)

\( \sigma = \text{RMS of a single sample (does not take into account improvement from using 5 samples)} \)

The energy resolution of the LAr electronic readout does not significantly contribute to the overall energy resolution.
Energy Linearity and Stability

- Energy linearity and stability determined from Ramp calibration runs
- The readout electronics are linear to ±0.2% or better (combined effects of front end and calibration boards)
- Gain variations with time are typically within 0.3%
  - outliers still under study; no obvious correlation with temperature or magnetic field
- Crosstalk dominated by capacitive couplings within calorimeter (4 – 7% EM 1st layer)
Timing Alignment & Resolution

Timing Resolution:
* Timing jitter per front end board < 20 ps (measured during production)
* Measured jitter dominated by calibration board TTCrx chip (~70 ps); expected to be lower during LHC collisions

Timing Alignment:
* Adjustments can be made by:
  * setting the delay per 128-channel front end board (applied based on first collision data)
  * adjusting the phase of the optimal filtering coefficients for each channel (in preparation)
* Goal: 100 ps (current resolution: ~1 ns)
Current front end design complexities / limitations:

* 11 application-specific integrated circuits (ASICs), some technologies obsolete → prevents component-level upgrade
* qualified for 10 years of LHC operation
* limited #spares (~6%)
* L1 trigger rate \( \leq 100 \text{ kHz} \), latency \( \leq 2.5 \mu \text{s} \) → super-LHC luminosities (up to \( 10^{35} \text{ cm}^{-2}\text{s}^{-1} \)) challenging
* analog summing limits L1 trigger sums to \( d\eta \times d\phi = 0.1 \times 0.1 \) grid → investigating more flexible, smaller granularity trigger sums
* consecutive L1 triggers must be spaced > 125 ns apart → difficult to handle bunch trains with shorter spacing
Proposed Design: “free-running” architecture (L1 pipeline moved off-detector)

**challenges:**
- digitization at 40 MHz (each bunch crossing) → need faster optical links (~100 Gbps/board)
- modern technology requires lower voltages (difficult to maintain req’d dynamic range & stringent noise performance)
- critical rad-hard components: analog front end, ADC, optical link, and power supply

**R&D ongoing:** e.g., IBM SiGe Quad Preamp/Shaper ASIC
- Preamp: based on current low noise line-terminating design
- Shaper: 16-bit dynamic range with 2 gain settings, low power consumption
- testing completed on hand-wired prototype (all measurements as expected)
  - will also explore other SiGe technologies and feasibility of CMOS-only design
Summary & Outlook

- The current LAr calorimeter electronics meets or exceeds the required performance
  - the readout performs over a wide dynamic range (and can be calibrated); the calibrations show excellent stability over 6-month periods
  - the DSP calculations have been optimized and validated, and the processing time meets the specification for the maximum L1 trigger rates
  - the coherent noise per channel is very low (~2–3% of the total noise)
  - pulses can be reconstructed with a precision that exceeds the intrinsic energy resolution of the calorimeters
  - front end board timing has been commissioned to ~1 ns with early 7 TeV collisions; we expect to achieve a resolution of 100 ps
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After 10 years of operation and with the sLHC expected radiation level, an upgrade to the front end electronics will be necessary:

- This provides an opportunity to modernize components and revise the architecture.
- R&D is progressing on new ASIC designs, radiation-hard optical links, a high-speed FPGA processing unit for the back end electronics, and a new power supply distribution scheme.