Electronic Readout of the ATLAS Liquid Argon Calorimeter: Calibration and Performance

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Abstract—The Liquid Argon (LAr) calorimeter is a key detector component in the ATLAS experiment at the Large Hadron Collider (LHC) at CERN. The LAr calorimeter is designed to provide precision measurements of electrons, photons, jets and missing transverse energy. It consists of a set of sampling calorimeters kept in three separate cryostats with liquid argon as the active medium.

The electronic readout of the ATLAS LAr calorimeters is divided into a Front End (FE) system of boards mounted in custom crates directly on the cryostat feedthroughs, and a Back End (BE) system of VME-based boards located in an off-detector underground counting room where there is no radiation. After a brief overview of the LAr readout electronics, we present a description of the methods used to reconstruct the calorimeter pulses and the system performance.

Given the intrinsic limitations imposed by the current FEBs, an upgrade will be necessary to maintain ATLAS physics potential at luminosities beyond $10^{33}$ cm$^{-2}$s$^{-1}$. We also present a brief description of the ongoing upgrade efforts.

I. INTRODUCTION

THE ATLAS detector [1] is a large, general-purpose detector designed to study the proton-proton collisions produced at the Large Hadron Collider (LHC) at CERN. The LHC is designed to provide collisions at a center-of-mass energy of 14 TeV; the machine was operated at energies of 900 GeV and 2.36 TeV in 2009, and is currently operating at 7 TeV in 2010. The LAr sampling calorimeter is a key component of the ATLAS detector, and is designed to provide precision measurements of electrons, photons, jets and missing transverse energy. Since its installation in 2006, the detector has collected a large amount of data from random triggers, calibration, cosmic muons, LHC beam splash events and collisions (2009 – 2010).

The LAr calorimeter consists of four subdetectors installed in three separate cryostats with liquid argon as the active medium. The electromagnetic (EM) barrel and endcap cover the central region of the detector ($|\eta| < 3.2$) and utilize accordion-shaped readout electrodes\(^1\). The hadronic endcap (HEC) covers the region $1.5 < |\eta| < 3.2$, and the forward calorimeter (FCal) extends the coverage out to $|\eta| = 4.9$. The number of channels per subdetector is shown in Table I. This sampling calorimeter is segmented in the $\eta - \phi$ plane, and is also divided into $2 - 4$ layers in depth, depending on the subdetector. A full description of the design and construction of the LAr calorimeter can be found in reference [2].

\(^1\)In the ATLAS coordinate system, $\theta$ is the polar angle and $\phi$ is the azimuthal angle with respect to the beam axis. The pseudorapidity, $\eta$, is defined as $\eta = - \ln \tan(\theta/2)$.

<table>
<thead>
<tr>
<th>Subdetector</th>
<th>Number of Channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>EM Barrel</td>
<td>109568</td>
</tr>
<tr>
<td>EM Endcap</td>
<td>63744</td>
</tr>
<tr>
<td>HEC</td>
<td>5632</td>
</tr>
<tr>
<td>FCal</td>
<td>3524</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>182468</strong></td>
</tr>
</tbody>
</table>

II. LAr READOUT ELECTRONICS

The LAr calorimeters are read out via a system of custom electronics whose goal is to measure the energy of the 182, 468 detector channels over a wide dynamic range (from tens of MeV to a few TeV). The electronic readout system is divided into a front end system of boards mounted in custom crates directly on the cryostat feedthroughs, and a back end system of VME-based boards located in an off-detector underground counting room where there is no radiation. The front end system [3] includes 1524 front end boards (FEBs) [4] that read out and digitize the calorimeter signals, along with calibration boards [5] that inject precision calibration signals, trigger boards which produce analog sums for the first level of the ATLAS trigger system, and control boards which receive and distribute the 40 MHz LHC clock as well as other configuration and control signals. There is a 1.6 Gbps fiber optic link from each FEB to the Read Out Driver (ROD) boards in the back end system which receive the digitized signals. The RODs perform digital filtering, formatting, and monitoring of the calorimeter signals before transmitting the processed data over $\sim 800$ optical links to the ATLAS data acquisition system (DAQ).

In the front end system, the detector signals are first subject to several stages of analog processing shown in Figure 1. Preamplifier hybrids amplify the raw signals; three versions match the subdetector capacitances and dynamic ranges. Although 97\% of the preamplifiers are on the FEBs, the HEC has cryogenic preamplifier summing boards mounted on the detector inside the cryostat. For the HEC, the preamplifiers on the FEBs are replaced by preshapers that invert, amplify, and shape the signal. The signals are then split and further amplified by shaper chips to produce three overlapping linear gain scales, with gain ratios of $\sim 10$ (the values for the low, medium, and high gains are 1, 9, 9, and 93, respectively). Fast bipolar shaping is performed with a time constant $\tau = RC = \ldots
Pulse Reconstruction and Calibration

A large energy dynamic range of the readout cells and a good energy resolution are some of the main challenges of the LAr readout electronics. A calibration board has been designed to allow computation of the electronic gain and extract the pulse shape of each individual channel. The board, hosted in the same crate as the front end boards, delivers a signal whose shape is close to the calorimeter ionization signal. This is achieved by applying an exponential voltage pulse across an injection resistor (of 0.1% accuracy) located in the cold, directly on the calorimeter electrodes.

The cell energy is converted from the reconstructed detector pulse as follows:

\[
E_{\text{cell}} = F_{\mu A \rightarrow \text{MeV}} \cdot F_{\text{DAC} - \mu A} \cdot \frac{1}{M_{\text{peak}}} \cdot R \left[ \sum_{j=1}^{N_{\text{samples}}} a_j (s_j - p) \right],
\]

where \( F_{\mu A \rightarrow \text{MeV}} \) relates the ionization current in the calorimeter to the energy deposited, \( F_{\text{DAC} - \mu A} \) converts the digital-to-analog converter (DAC) setting of the calibration board to the injected current, \( \frac{1}{M_{\text{peak}}} \) represents the ratio of the response of an ionization (physics) pulse to a calibration pulse, and \( R \) is the gain of the readout determined from the slope of

\[
\Sigma \Sigma
\]

and output data buffers, histograms, and calibration constants

second. The memory on each stores the DSP software, input and output data buffers, histograms, and calibration constants (packed in integer format). The energy, time, and quality factor calculations performed on the DSP have been optimized and validated with LHC collision data.

The bandwidth requirement is 75 kHz, which has been achieved with a 5-sample readout. (During current data-taking, the FEBs are configured to read out 7 samples.) The maximum input bandwidth is determined by the front end output and the input FPGAs, which have been tested up to 157 kHz. The maximum output bandwidth is limited by the DSP computations and formatting of the output data, and has been tested up to 85 kHz. The DSP processing time for one event (for 5-sample readout) is approximately 9.6 μs.

Fig. 1. Schematic block diagram of the FEB architecture. The signals from 128 channels come from the detector on the top left and proceed through several processing stages as described in the text. Analog sums exit on the bottom left through the layer sum boards (LSBs), and digitized results are transmitted to the back end RODs through an optical transmitter (OTx) on the right.

Fig. 2. The amplitude vs. time for the triangular pulse shape from the detector, overlaid with the bipolar-shaped and sampled pulse shape. Up to 32 samples (points) can be read out.

13 ns. The shaped signals are then sampled at the LHC bunch crossing frequency of 40 MHz by switched capacitor array (SCA) analog pipeline chips. Figure 2 shows the triangular pulse shape from the detector along with the shaped and sampled signal pulse shape. For events accepted by the level-1 trigger, up to 32 samples per channel are readout from the SCA using the optimal gain scale, and digitized using a 12-bit analog-to-digital converter (ADC). Gain selector (GSEL) chips choose the gain for each channel based on the peak value of each sample. The digitized data are formatted, multiplexed, serialized, and then transmitted optically out of the detector to the ROD in the counting room via a single 1.6 Gbps optical fiber per front end board. The RODs synchronize the output of the front end boards with the level-1 trigger and compute physical quantities such as the energy, time phase, and quality of the signal [6].

A schematic of a ROD motherboard can be seen in figure 3. Each ROD receives signals from eight FEBs. Four input field programmable gate arrays (FPGAs) parallelize the incoming data and verify its integrity. The memory is separated into two banks: one for writing incoming data, the other for the data that is read by the digital signal processor (DSP). Four processing units each contain two DSPs. These high-performance DSPs can process \( 5.7 \times 10^9 \) instructions per second. The memory on each stores the DSP software, input and output data buffers, histograms, and calibration constants (packed in integer format). The energy, time, and quality factor
the reconstructed pulse amplitude vs. the calibration board DAC setting. Each $a_j$ coefficient is calculated according to an optimal filtering algorithm [7]; $s_j$ is the $j$th recorded sample (where $N_{\text{samples}}$ is the number of readout samples), and $p$ is the pedestal value.

Three types of calibration runs are taken regularly and provide the values of the constants used to convert the reconstructed detector pulse into an energy measurement for a given cell: pedestal, ramp, and delay runs. During a pedestal run, the front end boards are triggered and read out without an input signal. In a ramp run, fixed-amplitude calibration pulses are injected for a range of DAC settings. In a delay run, fixed-amplitude pulses are injected with varying delays with respect to the FEB clock, allowing for detailed studies of the signal shape.

IV. PERFORMANCE

The LAr electronics performance can be characterized in terms of the noise performance, stability, energy reconstruction (including linearity and resolution) and timing performance. A detailed explanation of the electronics performance can be found in reference [8].

The noise is determined from the RMS of the pedestal values taken during a pedestal calibration run. The nominal pedestal value ($\sim 1000$ ADC counts) allows for a measurement of the pulse’s negative lobe, which is important for measuring the drift time and the effect of pile-up from earlier LHC bunch crossings. Typical noise levels are $30 - 50$ MeV for the EM calorimeters and $100 - 500$ MeV for the HEC and FCal. The coherent noise (measured in situ) is $2 - 6\%$ of the total noise per channel.

The pedestal, noise, and auto-correlation values were measured over a six-month period in early 2009 and show excellent stability. The variation in pedestal values was found to be $\sim 0.02$ ADC counts per channel (approximately $1$ MeV for the EM, $2$ MeV for the HEC, and $10$ MeV for the FCal in medium gain). The variation in noise was $< 0.01$ ADC counts in the EM and $\sim 0.02$ ADC counts in the FCal in high gain; the variation was an order of magnitude less in medium and low gain.

The LAr energy resolution must be precise over a wide energy range (MeV to TeV). Ramp calibration runs can be used to measure the contribution of the electronics to the overall energy resolution. Figure 4 shows the energy resolution ($\sigma(E)/E$) vs. the energy in GeV for all three gains for a typical cell in the second layer of the EM barrel, where $\sigma$ is the RMS of a single sample measured at the pulse peak, and does not take into account the improvement that can be gained from a 5-sample readout. These points can be compared to the curve, which represents an estimate of the energy resolution:

$$\frac{\sigma(E)}{E} = \frac{a}{\sqrt{E}} + b + \frac{c}{E},$$

where $a = 10\%$ (a typical value for the stochastic term for an EM shower), $b = 0.25\%$ (the local constant term that dominates at high energy), $c = 45$ MeV (the noise from a single sample in high gain), and $\oplus$ represents addition in quadrature. Since the points are below this estimated energy resolution curve for one cell, we conclude that the LAr electronic readout does not significantly contribute to the overall energy resolution.

Ramp calibration runs can also be used to determine the linearity of the energy measurement and the stability of the gain. From these runs, the readout electronics are linear to $\pm 0.2\%$ or better. The gain stability was also measured over a six-month period in early 2009; we find that the gain variations with time are typically within $0.3\%$.

The timing performance of the LAr electronic readout has also been studied. Coarse adjustments can be made to the timing by setting the delay per FEB (128 channels). The time offset for the FEBs in the EM barrel is shown in Figure 5. After correcting the FEB delay with collision data, the RMS of the timing is $\sim 1\text{ ns}$ for all of the subdetectors. Finer adjustments can also be performed by adjusting the phase of the optimal filter coefficients for each channel (in preparation); with this method the eventual goal for the timing resolution is $100\text{ ps}$. The jitter per FEB was measured during production and found to be $< 20\text{ ps}$ (typically $10\text{ ps}$) [4]. The jitter was also determined from calibration signals during calibration runs to be around $70\text{ ps}$, although this is dominated by the jitter from the custom TTCrx ASIC [9], and is expected to be lower during LHC collisions than from calibration runs.

V. CURRENT DESIGN COMPLEXITIES AND UPGRADE PROSPECTS

The present FEB architecture is qualified for 10 years of LHC operation with a limited number of spares ($\sim 6\%$). A FEB contains 11 application-specific integrated circuits (ASICs), and the technologies used for the existing ASICs are mostly obsolete, so a component-level upgrade is not possible. The FEB architecture was also not designed to allow any increase in the level-1 latency and trigger rate, which would make efficient physics data taking at super-LHC
Fig. 5. Number of FEBs vs. the FEB time offset in ns for FEBs in the EM barrel calorimeter. The RMS of the distribution is 1.0 ns with the timing determined from early $\sqrt{s} = 7$ TeV collision data. Similar timing results are found for the other LAr subdetectors.

![Graph](image)

Fig. 6. The proposed “free-running” front end design for the super-LHC upgrade. The signals from 128 channels come from the detector on the top left and proceed through several processing stages. The shaper only has two gain settings instead of the three in the current design. The level-1 pipeline is moved off of the detector, and the digitized signals (at 40 MHz) are transmitted in the “Serializer/Optics Out” stage at the right side of the diagram.

luminosities particularly challenging (up to $10^{35}$ cm$^{-2}$ s$^{-1}$). The analog summing limits the level-1 trigger sums to a $d\eta \times d\phi = 0.1 \times 0.1$ grid; for higher luminosities a more flexible, smaller grid is more desirable. Finally consecutive level-1 triggers must be spaced $> 125$ ns apart, making it difficult to handle bunch trains with shorter spacing.

The proposed upgrade design [10] is based on a free running architecture where the level-1 pipeline will be moved off-detector (see Figure 6). This requires digitization of all signals at 40 MHz, and transmission of all the data (approximately 100 Gbps per FEB) through multiple high speed radiation resistant optical links to the off-detector processing units, which will not only process the data in real-time but will also implement trigger algorithms. Modern technology requires lower voltages, making it challenging to maintain the required dynamic range and stringent noise performance. The critical radiation-hard components are the analog front end, the ADC, and the optical link.

Current research and development efforts are ongoing, including a front-end mixed-signal ASIC design. The ASIC design, Liquid Argon PreAmplifier Shaper (LAPAS), is designed in IBM SiGe 8WL. The preamplifier is based on the existing low noise line-terminating design, and the shaper has a 16-bit dynamic range with two gain settings (instead of the three settings in the current shapers) with low power consumption ($\sim 130$ mW) and uniformity better than 5%. The LAPAS design has been tested with a hand-wired prototype; all measurements are as expected and close to simulations. In the near term, other SiGe technologies will be explored and the feasibility of a CMOS-only design will be investigated.

Additional studies are continuing to develop fast, low-power ADCs, radiation-tolerant optical links in silicon on sapphire for faster data transmission [11], a high-speed back-end processing unit based on FPGAs, and a new power supply distribution scheme.

VI. Conclusion

The current LAr calorimeter readout electronics meets or exceeds the required performance. The readout performs over a wide dynamic range and can be calibrated; the calibrations show excellent stability over extended periods. The DSP calculations have been optimized and validated, and the processing time for 5-sample readout meets the specification for the maximum level-1 trigger rate. The coherent noise per channel is very low ($\sim 2 - 6\%$ of the total noise). The detector pulses can be reconstructed with a precision that exceeds the intrinsic energy resolution of the calorimeters. The FEB timing has been commissioned to a precision of $\sim 1$ ns with early 7 TeV collisions; preparations are underway to improve that resolution with a goal of 100 ps.

Although the calorimeter readout is performing quite well at current luminosities, after 10 years of operation and the higher radiation levels expected at the super-LHC, an upgrade to the front end electronics will be necessary to maintain the ATLAS physics potential at luminosities up to $10^{35}$ cm$^{-2}$ s$^{-1}$. This provides an opportunity to exploit technological advances, modernizing the components and improving on the existing architecture. Research and development is progressing smoothly on new ASIC designs, and the priority for the next few years is to demonstrate the feasibility of the proposed new architecture.

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REFERENCES


