FE-I4 Chip Development for Upgraded ATLAS Pixel Detector at LHC

Marlon Barbero, Bonn University
(for the FE-I4 Collaboration)

Pixel 2010, Grindelwald Switzerland, Sept. 6th-10th 2010
Contents

• Upgrades: IBL / sLHC.
  → FE-I4, new ATLAS pixel Front-End for IBL & sLHC.
• FE-I4A overview.
• Analog pixel.
• Digital pixel and digital Double-Column.
• Milestones and conclusion.
FE-I4 for IBL & sLHC

- **IBL (~2015):** inserted layer in current pixel detector.

- **sLHC tentative layout (~2020):**
  - 4-5 pixel layers, small radii / large(r) radii (note: Discussion on boundary pixel / short strips, ID layout...).
  - All Silicon.
  - Long Strips/ Short Strips / Pixels.
  - Pixels:
    - 2 or 3 fixed layers at ‘large’ radii
      (large area at 16 / 20 / 25 cms?)
    - 2 removable layers at ‘small’ radii

Present beam pipe & B-Layer

3 barrel layers / 3 end-caps
end-cap: z± 49.5 / 58 / 65 cm
barrel: r~ 5.0 / 8.8 / 12.2 cm

see F. Hügging, Monday
Motivation to re-design the FE

• Need for a new FE?

  • Smaller inner layer radius + potential luminosity increase
    \(\rightarrow\) higher hit rate.

  \(\rightarrow\) Current FE-I3 column-drain architecture saturated.

  \(\rightarrow\) FE-I4 new digital architecture:
    local regional memories,
    (stop moving hits around unless RO).

  \(\rightarrow\) FE-I4 has smaller pixel size (reduced cross-section).

  \(\rightarrow\) Technology 130 nm:
    \[0.25 \mu m \rightarrow 130 \text{ nm}\]
    Higher integration density for digital circuits, radiation-hardness (no Enclosed Layout Transistor), availability on timescales of our experiments.

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Future Thin FE-I4-Based Module
(& Consequences for FE-I4)

1) Big chip (periphery on one side of module).
2) Reduce size of periphery (2.8 mm → 2 mm).
3) Thin down FE chips (190 μm → 90 μm).
4) Thin down the sensor (250 μm → 200 μm)?
5) Less cables (powering scheme)?

- Big FE (~2x2cm!) with increased active area: from less than 75 % to ~90 %:
  → Reduced periphery; bigger IC; cost down for sLHC (main driver is flip-chip costs per chip).
- No Module Controller Chip:  
  → More digital functionality in the IC.
- Power:
  → Analog design for reduced currents; decrease of digital activity (digital logic sharing for neighbor pixels); new powering concepts. 8 metal layers [2 thick Alu.] → power routing.

see L. Gonella, Thursday
Target Specifications for FE-I4

- ToT coded 4 bits.
- DC leakage current tolerant to > 100 nA.

<table>
<thead>
<tr>
<th></th>
<th>FE-I3</th>
<th>FE-I4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel Size [μm²]</td>
<td>50×400</td>
<td>50×250</td>
</tr>
<tr>
<td>Pixel Array</td>
<td>18×160</td>
<td>80×336</td>
</tr>
<tr>
<td>Chip Size [mm²]</td>
<td>7.6×10.8</td>
<td>20.2×19.0</td>
</tr>
<tr>
<td>Active Fraction</td>
<td>74 %</td>
<td>89 %</td>
</tr>
<tr>
<td>Analog Current [μA/pix]</td>
<td>26</td>
<td>10</td>
</tr>
<tr>
<td>Digital Current [μA/pix]</td>
<td>17</td>
<td>10</td>
</tr>
<tr>
<td>Analog Voltage [V]</td>
<td>1.6</td>
<td>1.5</td>
</tr>
<tr>
<td>Digital Voltage [V]</td>
<td>2</td>
<td>1.2</td>
</tr>
<tr>
<td>pseudo-LVDS out [Mb/s]</td>
<td>40</td>
<td>160</td>
</tr>
</tbody>
</table>

biggest in HEP to date
analog / digital power
tuned for IBL occupancy
FE-I4A

- Full scale prototype.
- Many test features provided.
- Submitted August 2010.
pixel array: 336×80 pixels

periphery

CalPulse, ADC, InMUX, EFUSE, AltComp... and more.

+ Integration & Verification
Analog Pixel

- In FE-I4_proto1 (FE-I4 prototype submitted in 2008):
  - 2-stage architecture optimized for low power, low noise, fast rise time.
    - regul. casc. preamp. nmos input.
    - folded casc. 2\textsuperscript{nd} stage pmos input.
    - Additional gain, Cc/Cf2~6.
    - 2\textsuperscript{nd} stage decoupled from leakage related DC potential shift.
    - Cf1~17fF (~4 MIPs dyn. range).

13b configuration:
- 4 FDAC: tuning feedback current.
- 5 TDAC: tuning of discriminator threshold.
- 2 Local charge injection circuitry.
- 1 Hit Enable.
- 1 HitBus / IleakMonitor
Noise and Radiation Results

a) ENC on “Collaboration Proto 1” before and after irradiation (200 Mrad)

b) Measured ENC for pixels with and without $C_{load}$

c) Simulated ENC and time-walk @ 10 $\mu$A/pixel (preamp-amp2-comparator)

ENC = 160e- @ $C_d = 0.4pF$ & $I_L = 100nA$

$20 \text{ ns timewalk for} \ 2 \text{ ke}^- < Q_{in} < 52 \text{ ke}^-$ & threshold @ 1.5 ke-$^-$

$I_L = 100 \text{ nA}$

$I_L = 0 \text{ nA}$

ENC @ Low Current (10µA)

ENC = 160e- @ $C_d = 0.4pF$ & $I_L = 100nA$

$20 \text{ ns timewalk for} \ 2 \text{ ke}^- < Q_{in} < 52 \text{ ke}^-$ & threshold @ 1.5 ke-$^-$

$I_L = 100 \text{ nA}$

$I_L = 0 \text{ nA}$

200Mrad, $C_{load} \sim 400fF$

Q_{in}[C]  

<ENC> ~ 65 e

<ENC> ~ 90 e

I_{L} = 100 \text{ nA}

I_{L} = 0 \text{ nA}
4-Pixel Unit

- Store hits locally in region until L1T.
- Only 0.25% of pixel hits are shipped to EoC \(\rightarrow\) DC bus traffic “low”.
- Each pixel is tied to its neighbors -time info- (clustered nature of real hits). Small hits are close to large hits! To record small hits, use position instead of time. Handle on TW.

Consequences:
- Spatial association of digital hit to recover lower analog performance.
- Lowers digital power consumption (below 10 µW / pixel at IBL occupancy).
- Physics simulation \(\rightarrow\) Efficient architecture.
Performance / Efficiency

IBL: charge sharing in Z comparable to phi

Regional Buffer Overflow

<table>
<thead>
<tr>
<th>Memories</th>
<th>Simulation</th>
<th>Analytical</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>IBL</td>
<td>10xLHC</td>
</tr>
<tr>
<td>5</td>
<td>0.047%</td>
<td>2.19%</td>
</tr>
<tr>
<td>6</td>
<td>0.011%</td>
<td>0.65%</td>
</tr>
<tr>
<td>7</td>
<td>&lt;0.01%</td>
<td>0.16%</td>
</tr>
</tbody>
</table>

Inefficiency:
- Pile-up inefficiency (related to pixel x-section and return to baseline behavior of analog pixel) $\rightarrow$ $\sim$ 0.5%.
- Regional buffer overflow $\rightarrow$ $\sim$0.05%.
- Inefficiency under control for IBL occupancy.

@ IBL rate, pile-up inefficiency is the dominant source of inefficiency

Mean ToT = 4

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Pixel Layout

Power distribution and shield on top metals. Only vertical - no analog/digital crossing

Note: Digital ground tied to substrate, mixed signal environment BUT digital region placed in “T3” deep n-well.
Test Chip Submission

FE-I4-P1

61x14 array

Control Block

LDO Regulator

Charge Pump

Current Reference

SEU test IC

4-LVDS Rx/Tx

61x14 array

Capacitance Measurement

ShuLDO+trist LVDS/LDO/10b-DAC

turboPLL:
PLL core + PRBS + 8b10b coder + LVDS driv

low power discr.
Schedule and more information

- **Schedule:**
  - FE-I4A end September 2010.
  - Test setup readiness ramping-up, on time for IC back.
  - Tests: Wafer, single-chip, bump-bonded (planar, 3D, diamond), irrad...
  
  **see M. Backhaus, Poster Thursday**

- **Few references:**

- **plan for FE-I4B (= FE-I4 for IBL) in fall 2011**

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FE-I4 Collaboration

- Meeting 1 time a week.
- Collaborate remotely using Cliosoft platform.
- Participating institutes:
  - **Bonn**: D. Arutinov, M. Barbero, T. Hemperek, A. Kruth, M. Karagounis.
  - **CPPM**: D. Fougeron, F. Gensolen, M. Menouni.
  - **Genova**: R. Beccherle, G. Darbo.
  - **LAL**: J. Fleury.
  - **LBNL**: S. Dube, D. Elledge, M. Garcia-Sciveres, D. Gnani, A. Mekkaoui.
  - **Nikhef**: V. Gromov, R. Kluit, J.D. Schipper, V. Zivkovic.