ATLAS Tracker Upgrade: Silicon Strip Detectors for the sLHC

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Abstract—To extend the physics potential of the Large Hadron Collider (LHC) at CERN, upgrades of the accelerator complex and the detectors towards the Super-LHC (sLHC) are foreseen. The upgrades, separated in Phase-1 and Phase-2, aim at increasing the luminosity while leaving the energy of the colliding particles (7 TeV per proton beam) unchanged. After the Phase-2 upgrade the average luminosity will be a factor of 5-10 higher than the design luminosity of the LHC. Due to the increased track rate and extreme radiation levels for the tracking detectors, upgrades of the detectors are necessary. At ATLAS, one of the two general purpose detectors at the LHC, the current inner detector will be replaced by an all-silicon tracker. This article describes the plans for the Phase-2 upgrade of the silicon strip detector of ATLAS. Radiation hard n-in-p silicon detectors with shorter strips than currently installed in ATLAS are planned. Results of measurements with these sensors and plans for module designs will be discussed.

I. INTRODUCTION

THE Large Hadron Collider (LHC) at CERN started operation with physics data taking in 2009. To enhance the physics potential and to facilitate precision measurements of discoveries made at the LHC, plans for luminosity upgrades towards the Super-LHC (sLHC) exist [1]. The LHC is designed for a peak instantaneous luminosity of \( L = 10^{34} \text{cm}^{-2}\text{s}^{-1} \). After the Phase-1 upgrade around 2015 and the Phase-2 upgrade around 2020 (which marks the beginning of the sLHC) the peak luminosity will be increased up to \( L = 5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1} \), with luminosity levelling to further increase the average luminosity. Together with the aim to collect an integrated luminosity of 3000 fb\(^{-1}\) this will lead to a highly increased track rate and higher radiation damage in the tracking detectors compared to the conditions at the LHC. The number of pile-up events per bunch crossing will increase from \( \sim 23 \) at the LHC (for \( L = 10^{34} \text{cm}^{-2}\text{s}^{-1} \)) to 100-200 at the sLHC (for \( L = 5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1} \)). The radiation-induced bulk damage of the silicon detectors, quantified as a fluence of 1 MeV neutron equivalent particles per square centimetre (n\(_{eq}\)/cm\(^2\)), will increase by an order of magnitude. These effects require extensive upgrades of the detectors. In the projected sLHC tracker design of ATLAS the inner pixel layers (at a radius of \( R \approx 3.7 \text{cm} \) from the interaction point) will receive a fluence of more than \( 10^{16} \text{n}_{eq}/\text{cm}^2 \) and the inner strip layers \( (R \approx 38 \text{ cm}) \) will receive approximately \( 10^{15} \text{n}_{eq}/\text{cm}^2 \).

While the upgrade plans of the ATLAS detector for the Phase-1 upgrade are limited to the pixel detector, the entire inner detector will be replaced for the Phase-2 upgrade. The inner detector will then consist of a pixel detector in the inner layers and of a strip detector further outwards from the interaction point. The Transition Radiation Tracker (TRT), which currently constitutes the outermost part of the inner detector, will be entirely replaced by the silicon strip detector. The TRT is not expected to function at the high luminosity foreseen for the sLHC.

This article describes the plans for the strip part of the ATLAS inner tracker [2] upgrade. To keep the occupancy below an acceptable limit, a high segmentation is necessary. Therefore in the inner strip-region, the strip length will be shortened to 2.4 cm. In order to cope with the harsh radiation damage, radiation tolerant silicon detectors with n-side readout in p-type bulk material (n-in-p detectors) are planned. Results from various measurements, studying the performance especially after irradiation, are discussed. Furthermore, developments concerning module designs, powering concepts and front-end chips are discussed.

II. INNER DETECTOR LAYOUT

The proposed layout of the inner detector of ATLAS for the sLHC upgrade is shown in Fig. 1. It is an all-silicon detector, the innermost part will be covered by pixel detectors, followed by short strip detectors and then long strip detectors in the outermost region.

In the barrel region, four pixel layers are planned, where the innermost one, the B-layer, will have a radial distance of 3.7 cm to the beam. In the forward region, six pixel discs will be located on either side. As the B-layer will have to withstand a radiation fluence of approximately \( 2 \times 10^{16} \text{n}_{eq}/\text{cm}^2 \) (see section II-A), extremely radiation tolerant detector technologies are necessary. As a possible alternative to the planar silicon pixel detectors currently installed, several options are studied: 3D-detectors, diamond detectors and thin silicon detectors [3].

Three barrel layers will be equipped with short strip detectors, which have a strip length of 2.4 cm. The innermost strip layer will be located at approximately 38 cm from the beam line. Further outwards, two barrel layers with long strip detectors with a strip length of 9.6 cm are planned. The forward region will be covered by 5 discs on either side of the interaction point. On the discs sensors with different strip lengths will be employed. The outermost strip layer will be 1 m away from the beam line. In this way, the silicon strip detectors will cover the space where the TRT in the current inner detector of ATLAS is located.

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A. Radiation Fluence

The radiation fluence as a function of the radial distance to the beam axis for the ATLAS inner detector at the sLHC is shown in Fig. 2. The data shown were simulated for an integrated luminosity of 6000 fb$^{-1}$ and therefore include a safety factor of two with respect to the expected luminosity at the sLHC. At $R = 3.7$ cm, where the pixel B-layer will be located, a radiation fluence of $2 \times 10^{16}$ n$_{eq}$/cm$^2$ is expected. In the innermost strip layers, a radiation fluence of the order of $10^{15}$ n$_{eq}$/cm$^2$ is expected. These are a factor of 5-10 times higher than the total fluence expected at the LHC. While the fluence in the pixel layers is dominated by charged hadrons (protons and pions), it is dominated by neutrons in the region which will be equipped with strip detectors. The larger fraction of neutrons in the outer region of the inner detector is caused by neutrons which are backscattered from the calorimeters.

III. Silicon Strip Sensors

As a radiation hard technology planar n-in-p silicon strip sensors with float-zone substrate are planned. These have several advantages compared to p-in-n sensors, which are currently employed at the ATLAS SCT [2]. Detectors with p-type substrate do not undergo type inversion. Hence the depletion in n-in-p sensors starts from the structured side, where the maximum of the weighting field is located, before and after irradiation. Therefore, the sensors can be operated under-depleted. After irradiation fluences of the order of $10^{15}$ n$_{eq}$/cm$^2$ full depletion would be hardly possible. A further advantage is that the signal is dominated by electrons, which are less affected by trapping at radiation-induced defects compared to holes. Compared to n-in-n sensors, which are for example used in the current ATLAS pixel detector [2] and require double-sided processing, only single-sided processing is required for n-in-p sensors. This is an important aspect concerning the costs of the detector.

Since 2005, the ATLAS strip sensor upgrade collaboration has developed n-in-p silicon strip sensors in close collaboration with a commercial company, Hamamatsu Photonics [6]. Several sensor batches were fabricated by Hamamatsu. The most recent batch, named ATLAS07, was produced on 6-inch (150 mm) wafers having a thickness of 320 µm. The wafer layout is shown in Fig. 3. The central part is covered by a full-size sensor (97.54 mm × 97.54 mm), which corresponds to the dimensions of the sensors planned for the barrel part of the SCT upgrade. It has four segments of strips, two with axial strips (at the top) and two with stereo strips (at the bottom), having a stereo angle of 40 mrad. Each full-size sensor has in total 5128 strips (1282 per segment) with a pitch of 74.5 µm and a strip length of 2.4 cm. At the border of the wafer 24 miniature sensors (10 mm × 10 mm) are placed.
Fig. 3: Layout of the ATLAS07 wafer. The major part of the wafer is occupied by a full size sensor, while 24 miniature sensors are located at the wafer margin [7].

These detectors are made in different configurations, for example with different pitches (74.5 $\mu$m and 100 $\mu$m), different p-stop strip isolation structures and different punch-through protection structures. Furthermore, different ion concentrations for the p-stop structures and partly also p-spray isolation is applied. All sensors have an AC-coupling structure. A detailed description of the sensor design and the wide variety of sensor configurations produced can be found in [7]. Results of electrical measurements of ATLAS07 miniature and full-size sensors are described in [8], [9].

A. Charge Collection

The charge collection of ATLAS07 miniature sensors before and after irradiation was studied by various groups [10]. The sensors were irradiated with 70 MeV protons at the Cyclotron and Radioisotope Center (Cyric) at Tohoku university in Japan, with neutrons at the TRIGA reactor in Ljubljana, Slovenia, and with 25 MeV protons at the Compact Cyclotron in Karlsruhe, Germany. The measurements were performed using a radioactive beta source ($^{90}$Sr). The signal generated by electrons penetrating the detectors was measured applying LHC readout electronics. The collected charge after neutron irradiation to a fluence of $10^{15}$ $n_{eq}$/cm$^2$ is shown in Fig. 4. The signal reflects the Landau most probable value, extracted from a fit of a convolution of a Landau and a Gaussian to the signal spectra. At a bias voltage of 500 V a signal of approximately 12000 electrons can be measured, compared to an expected signal of $\sim$ 25000 electrons in the unirradiated detector. The noise level for the short strip detectors is expected to be approximately 600 e$^-$. Thus, the signal measured after the design fluence of $10^{15} n_{eq}$/cm$^2$ is still sufficient for operation and a signal-to-noise ratio of approximately 20 can be expected. However, increasing the bias voltage by a few hundred volts would lead to a significantly increased signal. The power supplies and cables of the current ATLAS SCT are limited to 500 V, but increasing the bias voltage limit for the sLHC upgrade is being discussed.

The data shown in Fig. 4 reflect the signal measured after annealing of 80 min at 60°C, which minimises the full depletion voltage before reverse annealing dominates. The measurements done by Liverpool and Valencia, which were performed un-annealed, were scaled by $(20 \pm 10\%)$ to account for the signal increase due to annealing [10]. An overall agreement of the results obtained by the different groups can be seen. Slight variations are apparent, these are likely due to the annealing corrections applied.

B. Efficiency

The upgrade will use binary readout, which is also employed in the current SCT. Therefore, the efficiency at a fixed threshold is of particular importance. The efficiency of ATLAS07 miniature sensors, which were irradiated with 25 MeV protons at the Karlsruhe Compact Cyclotron, was investigated with test beam measurements. The test beam was performed at the CERN SPS H2 beam line, which delivers 225 GeV pions. The reference tracks were measured by the silicon beam telescope (SiBT) [11]. Analogue readout with APV25 front-end chips [12] was applied. A detailed description of the test beam measurements with further results concerning charge collection, charge sharing and resolution can be found in [13].

The efficiency measured with detectors irradiated to $5 \times 10^{13}$ $n_{eq}$/cm$^2$ and $10^{15} n_{eq}$/cm$^2$ is shown in Fig. 5. The lightly irradiated detector can be regarded as almost unirradiated since no significant radiation-induced bulk damage leading to lower signal or decreased efficiency is expected. For the calculation of the efficiency a hit is regarded as
Bias Voltage (V)  
0  200  400  600  800  1000  
Efficiency  
0.8  0.85  0.9  0.95  1  2 

eq \frac{13}{10} \times 5 \ cm^2

eq \frac{15}{10} \times 1 \ cm^2

Fig. 5: Efficiency of ATLAS07 miniature detectors irradiated to $5 \times 10^{13} n_{eq}/cm^2$ and $10^{13} n_{eq}/cm^2$, measured in a test beam. The efficiency was calculated applying a threshold of 1 fC. detected if the signal of a single channel exceeds a threshold of 1 fC, where the search window is limited to the channel where the track is pointing to and one neighbour on either side. No clustering algorithm was applied, hence this strategy is comparable to binary readout. The threshold of 1 fC was chosen as it is applied at the current ATLAS SCT. In Fig. 5 it can be seen that the efficiency of an unirradiated detector can be reached with the detector irradiated to $10^{13} n_{eq}/cm^2$. However, this requires bias voltages higher than 500 V, which equals the limit of the current SCT power supplies, or a lower threshold. At a bias voltage of 500 V with a threshold of 1 fC an efficiency of 92% is achieved, while more than 99% can be reached with a threshold of 0.7 fC (for a fluence of $10^{13} n_{eq}/cm^2$).

It has to be noted that the efficiency studies were performed with unirradiated readout electronics. As the efficiency also depends on the width of the signal spectrum and therefore on the noise, a dependence on the strip length and on the readout electronics can be expected.

### IV. Integration Concepts

A well-advanced concept, the single-sided stave design, exists for integration of sensors, readout electronics and support structures. It is based on a high level of integration. This is complemented by a backup option, the double-sided module concept. So far, the developments concentrate on integration concepts for the short-strip region. The concepts must meet numerous requirements like mechanical stability, low mass, cooling performance, high voltage stability and low noise. Due to the high number of readout channels and the increased radiation-induced leakage current of the silicon sensors the performance of the cooling system and high thermal conductivity of the support structures are essential.

#### A. Single-Sided Stave Concept

The baseline integration layout is the stave concept [4], where single-sided modules are mounted on either side of a support structure, see Fig. 6. The hybrids, carrying the readout chips, are directly glued onto the sensors. The sensors are glued onto bus cables, which are glued onto the cooling substrate. Therefore, the sensors serve as heat conductors to remove the heat power generated by the front-end chips. On either side 12 modules are arranged in a row, see Fig. 7. Each module consists of one sensor tile with four rows of strips as described in section III. Single modules and a first “stavelet” carrying four modules have been built. Extensive work in several institutes is going on to produce and test the first full-size demonstrator stave.

Fig. 6: Cross-section of the stave concept. Hybrids with front-end chips are glued on either side of the stave on top of the silicon sensors.

Fig. 7: Stave design (length: 1.2 m) with 12 single-sided modules per side. The lower left corner shows the end part of the stave. The hybrid (green) is glued on top of the sensor (red) [4].

The single-sided module stave design is being adapted to the forward region. Here, individual petals are foreseen (see Fig. 8) which carry sensors having inclined strips, with fixed angular pitch. Several sensors will be mounted on a petal with short strips at the inner side and longer strips at the outer side. Plans exist for production of prototype sensors having a layout as foreseen for the forward region.

Fig. 8: Petal design in the forward region. The hybrids (yellow), carrying the front-end chips (dark grey), are glued onto the sensors (light grey).
B. Double-Sided Module Concept

The double-sided super-module concept [14] is an alternative to the stave concept with single-sided modules. It is a more modular approach following the concept realised in the current SCT. The minimal modular unit, see Fig. 9, carries one sensor on either side. The sensors are glued to a Thermo-Pyrolytically-Graphite (TPG) baseboard. The hybrids, carrying the front-end chips, are glued to heat conducting carbon-carbon bridges to take the heat to the module edges. Twelve modules are arranged in a row with cooling and support structures to make a super-module. Single modules have been produced, irradiated and tested; tests of a mini super-module are under way.

V. POWERING CONCEPTS

Individual powering of the on-detector electronics, which is currently applied, will be impossible at the sLHC due to the heavily increased number of channels. Aiming at minimising the power loss in the cables, and hence transmitting the power at higher voltage and lower currents, several powering concepts are under study [15].

One option is serial powering [15], [16], where a constant current is provided to a chain of detector modules. The module voltage is provided by shunt regulator and shunt transistor circuitry on the modules. As an alternative, power distribution with the use of local DC-DC converters is studied [15]. Groups of modules could be powered in parallel and the local step-down conversion could be achieved by buck converters. Extensive R&D on both options is on-going.

VI. FRONT-END CHIP DEVELOPMENTS

Based on the ABCD3T, the front-end chip which is currently employed at the SCT, the ABCN-25 has been designed [17]. It features binary readout and is implemented in 0.25 μm CMOS technology. Requirements concerning radiation hardness are considered in the layout and SEU detection and correction circuitry have been implemented. The chip has 128 input channels and is optimised for the short strips with a length of 2.4 cm. Modules have been realised with ABCN-25 chips and the results are encouraging. The ABCN-25 is an important milestone towards the front-end for the upgrade, which will be developed in 130 nm technology.

VII. SUMMARY

Several challenges exist for the sLHC upgrade of the ATLAS SCT. Especially, requirements concerning radiation hardness and increased track rate have to be considered for the design. As a key point, radiation hard n-in-p silicon strip detectors have been developed. Module integration concepts have been defined and extensive R&D is being performed concerning the final design. Serial powering and powering using DC-DC converters are studied and developments for the front-end chips are progressing.

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REFERENCES