The phase 1 upgrade of the CMS Pixel Front-End Driver

This article has been downloaded from IOPscience. Please scroll down to see the full text article.

2010 JINST 5 C12054

(<http://iopscience.iop.org/1748-0221/5/12/C12054>)

View [the table of contents for this issue](#), or go to the [journal homepage](#) for more

Download details:

IP Address: 137.138.124.142

The article was downloaded on 11/07/2011 at 12:46

Please note that [terms and conditions apply](#).

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2010,
20–24 SEPTEMBER 2010,
AACHEN, GERMANY

The phase 1 upgrade of the CMS Pixel Front-End Driver

M. Friedl,¹ M. Pernicka and H. Steininger

*Institute of High Energy Physics, Austrian Academy of Sciences,
Nikolsdorfer Gasse 18, A-1050 Vienna, Austria*

E-mail: friedl@hephy.oeaw.ac.at

ABSTRACT: The pixel detector of the CMS experiment at the LHC is read out by analog optical links, sending the data to 9U VME Front-End Driver (FED) boards located in the electronics cavern.

There are plans for the phase 1 upgrade of the pixel detector (2016) to add one more layer, while significantly cutting down the overall material budget. At the same time, the optical data transmission will be replaced by a serialized digital scheme.

A plug-in board solution with a high-speed digital optical receiver has been developed for the Pixel-FED readout boards and will be presented along with first tests of the future optical link.

KEYWORDS: Optical detector readout concepts; Electronic detector readout concepts (solid-state); Data acquisition concepts

¹Corresponding author.

Contents

1	Introduction	1
1.1	Present system	1
2	Upgrade plans	2
3	Digital optical receiver	3
3.1	Measurement results	4
4	Pixel-FED modification	5
5	Summary and outlook	6

1 Introduction

The present pixel detector [1] of the CMS experiment at CERN was designed for a maximum luminosity of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, a value which will be reached in 2015. Consequently, an upgrade of the pixel detector is scheduled thereafter. The whole year 2016 will be devoted to maintenance and improvement works on both machine and experiments, including the CMS pixel detector [2].

1.1 Present system

The CMS pixel detector consists of 3 barrel layers and 2 endcap disks on each side. Its innermost layer is located at a radius of 4.4cm, close to the beam pipe, in order to achieve good vertex resolution.

Each pixel “read out chip” (ROC) serves 4160 cells with a size of $100 \times 150 \mu\text{m}^2$ each. In the barrel part, 16 such chips and one sensor are arranged in one module, the basic unit of the pixel detector, while up to 24 chips and 3 sensors make up the endcap modules. Each of those units contains one control chip called “Token Bit Manager” (TBM) which interfaces incoming and outgoing signals. In the present system, one such TBM collects all the zero-suppressed ROC signals on a module and sends them to two analog optical links, each propagating 40MS/s of time-multiplexed analog data using 1310nm wavelength.

Figure 1 shows the readout chain of the pixel detector signals. The data are sent through about 100m of single-mode optical fiber to the electronics hut, where they are received by Pixel-FED [3] readout boards. Each of these modules contains three 12-way analog optical receivers (ARx12) and subsequent flash ADCs for conversion to digital signals. The data are buffered, sorted and processed using five FPGAs before being passed on to the central data acquisition system through S-Link [4] connections.

Figure 1. Readout chain of the CMS pixel detector from front-end modules to the central data acquisition (DAQ) system.

2 Upgrade plans

For the phase 1 upgrade to be commissioned in 2016, one layer will be added to both barrel and endcap parts of the CMS pixel detector. This will significantly increase its tracking capabilities and — thanks to new structural materials and a new cooling system — at the same time cut down its material budget, which is important to minimize multiple scattering. Despite of the additional layer, the overall mass of the pixel detector will only be half of its present value [5].

A serious restriction for the upgrade is that the services installed in the CMS experiment — cooling pipes, cables and fibers — will remain unchanged. Given the fact that the new front-end will be bigger, this necessitates significant changes in cooling (CO_2 instead of the present C_6F_{14}), powering (local DC-DC conversion) and signal transfer [6].

The only way of reading out a larger number of detector modules over the same number of fibers is apparently an increase in bandwidth utilization of each fiber. As this is difficult with the present analog system, it was decided to use digital optical transmission.

The current analog and the future digital transmission schemes are compared in figure 2. In the present system, each pixel hit contains a header, the pixel address which is coded using six different analog levels, and eventually the analog signal pulse height. In total, this requires nine clock periods. Translating to digital, this means that each clock period must contain four bits, where 12 bits denote the header, 16 give the address and the final 8 bits tell the pulse height. This scheme also takes nine clock cycles for a pixel hit and thus alone would not improve the system throughput. However, each current module is read out by two analog optical links, while the digital version should eventually multiplex two pixel data streams within the TBM and finally send out the data over a single fiber at 320Mb/s.

In order to use digital transmission, several devices in the readout chain need upgrades, starting at the ROC. Most of its circuitry, in particular the pixel cells and the column drain mechanism, will not be touched. The only modification will be done at the output interface, where the analog level encoding will be removed, but a PLL (to multiply the clock by four) and an ADC (to digitize the pulse height) will be added to achieve a digital output rate of 160Mb/s. Similarly, the TBM needs some modifications for both the interfaces to the ROCs as well as the output to the optical link, where two pixel data streams will be multiplexed, resulting in a data rate of 320Mb/s.

Figure 2. Data transmission from a pixel module in the (a) present analog and (b) future digital configurations.

Nonetheless, this scheme requires only minor alterations to the existing ASICs and thus was preferred to other solutions with Gb/s links, which would have demanded more substantial changes to the existing system.

In order to minimize the risk of ASIC design errors, the modifications in the front-end electronics will be as little as possible. This implies that the data transfer will not follow a standard code (such as 8b/10b). Nonetheless, some precautions must be taken in order to ensure a (globally) balanced code for the optical link. One such issue is the coding of the pixel address within the ROC, which will be done in a way to avoid more than seven consecutive 0s or 1s in the data stream (while 1111 1111 is reserved for the header). Moreover, the TBM, which multiplexes two pixel data streams, will generally invert one of those streams. In case one stream is empty (no data), the TBM will replicate and invert the non-empty channel and send it in place of the empty one, which will result in a perfectly balanced code.

The present optical transmitter boards are designed for analog transmission at 40 MS/s. Even though their actual bandwidth would (marginally) allow transmission at 320 Mb/s, it was decided to replace them with a faster optical sender for the upgrade. As mentioned before, the optical fibers will remain the same, so both sender and receiver are restricted to 1310 nm with single-mode fiber. In the electronics hut, the installed fibers end with 12-way MPO connectors which should ideally match with the upgraded receivers.

3 Digital optical receiver

The existing analog optical receiver (ARx12) has an integrated amplifier with a bandwidth limitation of about 100 MHz. Consequently, its operation at 320 Mb/s is not obvious.

Unfortunately, the CMS pixel system is bound to 1310 nm due to the installed single-mode fiber, where the supply situation is poor for arrays with 12-way MPO connection. Thanks to the effort of the CERN Optoelectronics Group, we could obtain an engineering sample of a commercial optical receiver which was modified to operate at our wavelength. It was manufactured by Zarlink company (now Tyco Electronics), part no. ZL60110.

Figure 3. Measurement setup for comparative testing of optical receivers.

We performed comparative measurements between the ARx12 (with a subsequent discriminator) and the Zarlink engineering sample using the setup shown in figure 3. A pattern generator was used to create arbitrary signals (e.g. PRBS) at 320Mb/s, which were fed into a 3-way optical transmitter board from the CMS Tracker. Its optical modulation amplitude was about 0.1 mW for all of these tests, measured with an optical head attached to a scope. For the actual tests, either ARx12 or Zarlink were connected to the other end of the fiber. Their electrical output was eventually analyzed by a fast digital scope.

3.1 Measurement results

The first test was related to continuously unbalanced code, e.g., sending rectangular pulses with a duty cycle below 50%. While the optical head correctly displayed the duty cycle down to 12.5% (corresponding to a continuous bit pattern “1000 0000”), both ARx12 and Zarlink had problems resulting in a prolonged “1” time measured at the receiver side compared to what was actually sent. Zarlink even started to create intermittent random (noise) pulses at heavily unbalanced code (12.5%). This is apparently related to shifts of the internal threshold and simply underlines the necessity of a globally balanced code.

Another test was performed to investigate the behavior with temporary excursions from otherwise balanced code. Surprisingly, Zarlink tolerates about 700 consecutive zeros (or ones) without an effect on the subsequent pattern. In case of the ARx12, the tolerance limit was even 3000. Again, this is an absolutely unrealistic situation as the pixel data code will by design have eight consecutive equal bits at most.

The third test was related to the transmission quality. Figure 4 shows the eye diagrams measured with the (analog) optical head, the ARx12 and the Zarlink, using a balanced PRBS14 signal. The analog recording reveals some bandwidth limitations (on the sender side), but still shows a clear opening. In case of the ARx12, however, the eye is almost closed due to a large jitter which depended heavily on the actual sender settings. In case of the Zarlink, the eye diagram looks perfectly fine, which is related to its specified data rate of 2.7 Gb/s.

From these tests we conclude that the ARx12 is not suitable for operation with a digital link at 320Mb/s and thus it must be replaced by a faster device — such as the Zarlink — for the Pixel-FED upgrade. However, we should also point out that these tests were only a first investigation to check the suitability of those receivers for operation of 320Mb/s. Further tests will follow, in particular bit error rate measurements with variable optical modulation amplitude (i.e. attenuation). We are

Figure 4. PRBS14 eye diagrams recorded with optical head, ARx12 and Zarlink at 320Mb/s.

presently preparing such tests using real pixel data (from the running CMS experiment) which are re-encoded into a bitstream as foreseen in the upgrade. This will give a more realistic picture of the optical link performance in the actual application.

4 Pixel-FED modification

The current Pixel-FED contains three ARx12 and 3×3 ADC daughter boards. As the latter are obviously not needed anymore for digital transmission, we have devised a plug-in replacement board that holds the Zarlink receiver as well as an FPGA for deserialization. This board eventually passes on the received data in a parallel fashion to the subsequent FED electronics such that no further changes in hardware are required. Thus, the modification is very cost-effective and abandons the need to develop a completely new main board. As seen in figure 5, the old ARx12 can even remain on the PCB which allows to quickly change between the two versions.

As the ROC does not use a standard protocol, a custom FPGA code needs to be developed for deserialization and synchronization. This work has been started by implementing a phase detector which samples the incoming data at different clock phases. In the future, these taps will be used to determine where transitions happen and consequently select the outputs which have the maximum distance to those transitions in order to get a self-adjusting, stable signal.

Figure 5. Digital receiver daughter board as a drop-in replacement for three ADC daughter cards.

5 Summary and outlook

The phase 1 upgrade of the CMS pixel detector has an impact on the readout scheme, as the data transmission will change from 40MS/s analog to 320Mb/s digital. The choice of the optical link is driven by the fact that the installed fibers cannot be changed and thus will have to operate at 1310nm wavelength.

We have shown that the existing analog optical receiver is not suitable for the upgrade due to its internal bandwidth limitation. A modified commercial device was identified, tested and found to fit for this application. Even though this is now only a single source, we will look out for other commercial devices which might emerge in the future.

In order to integrate those devices into the existing Pixel-FED boards, we have developed a plug-in board which replaces three ADC daughter cards. That PCB contains the new optical receiver and an FPGA which will be used for synchronization and deserialization of the incoming data in a way that is transparent to the subsequent electronics. Thanks to this modular approach, the other parts of the Pixel-FED do not require any hardware modification.

References

- [1] D. Kotlinksi, *Status of the CMS pixel detector*, [2009 JINST 4 P03019](#).
- [2] A. Bean, *The CMS pixel detector and challenges (prospectives) for its upgrade*, [Nucl. Instrum. Meth. A 624 \(2010\) 286](#).
- [3] M. Pernicka et al., *The CMS Pixel FED*, in *Topical Workshop on Electronics for Particle Physics*, Prague, Czech Republic, 3–7 Sep 2007, [CERN-2007-007](#), pp.487-491.
- [4] H.C. van der Bij et al., *S-LINK, a data link interface specification for the LHC era*, [IEEE Trans. Nucl. Sci. 44 \(1997\) 398](#).
- [5] H.C. Kästli, *A low mass pixel detector upgrade for CMS*, [arXiv:1001.3933](#).
- [6] V. Radicci, *CMS pixel detector upgrade*, [2009 JINST 4 P03022](#).