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The TOTEM T1 read out card motherboard

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ABSTRACT: This article describes the Read Out Card (ROC) motherboard, which is the main component of the T1 forward telescope front-end electronic system. The ROC main objectives are to acquire tracking data and trigger information from the detector. It performs data conversion from electrical to optical format and transfers the data streams to the next level of the system and it implements Slow Control modules which are able to receive, decode and distribute the LHC machine low jitter clock and fast command. The ROC also provides a spy mezzanine connection based on programmable FPGA and USB2.0 for laboratory and portable DAQ debugging system.

KEYWORDS: Optical detector readout concepts; Data acquisition circuits; Front-end electronics for detector readout; Digital electronic circuits

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1 Introduction

The TOTEM experiment [1] is designed to measure the proton-proton elastic and total cross section at the CERN Large Hadron Collider (LHC) and is composed of three sub-detector telescopes: T1 equipped with Cathode Strip Chambers (CSC), T2 with Gas Electron Multiplier detectors (GEM) and Roman Pots with silicon edgeless microstrip silicon detector. The T1 detector will measure the inelastic rate in the pseudo-rapidity region $3.1 \leq |\eta| \leq 4.7$.

The T1 telescope consists of four sets (quarters) of five equally spaced planes of CSC detectors which in turn generate about 11000 anodes (AFECs) and 16000 cathodes (CFECs) signals. Data from each of these must be processed and optically transmitted to the counting room.

A basic block diagram of the functional components of one quarter of the system is shown in figure 1. Three logically and physically separated regions make up the T1 electronic system [2]: the “*On Detector Region*” where the Front-End ASICs are located, the “*Local Detector Region*” where the data are collected and optically transmitted via the Read-Out Card motherboards (ROC) to the “*Counting Room Region*” where they are received by the TOTEM Front End Driver (TOTFED).

The charge readout of the detectors is based on the TOTEM front-end ASIC named VFAT [3]. The chip contains both analog and digital functions traditionally found on separate components. The VFAT is a very low noise 128 channels front-end amplifier with programmable internal calibration, intelligent “fast OR” trigger outputs, digital data tagging and storage, data formatting and data packet transmission with error protection.

Up to 16 VFATs, mounted on custom hybrids, are connected to each of the 36 ROC (9 per T1 quarter) via flexible connections.

Figure 1. T1 electronic system architecture.

Figure 2. ROC motherboard — top and bottom side.

2 General design specifications

The ROC which is the electric junction point of two CSC detectors must fit in the T1 telescope complex mechanics. It connects up to 16 hybrids on the anodes and cathodes cards and finally controls 2048 signals to and from the outside world. The connections to the detector ASICs are made by flexible shielded fine pitch flat cables while the other connections are performed by twisted pairs ribbon cables and single mode ribbon optic fibers.

The layout of the ROC, given the large number of connections and other size limitations, results in a very challenging 12 layers layout.

Besides the electrical functionality described in detail in the following, the design of the ROC is constrained by mechanics and radiation tolerance considerations.

In order to guarantee robustness to the large radiation doses the ROC will be exposed to, all the active components used in the ROC are design radiation tolerant components fabricated in the standard $0.25\ \mu\text{m}$ CMOS technology and employing radiation tolerant layout practices [4, 5]. Safety regulations imposed also fabrication of the board with halogen free material.

Figure 2 shows the two sides of the completed board with mezzanine cards mounted. The black connectors (top) placed along the long sides of the board are for detector signal connection; on the

Figure 3. ROC motherboard block diagram.

short sides one can see on the left the connectors for the Slow Control Ring (top), Tracking and Trigger Data (bottom). The Low Voltage connectors are on the bottom side on the right. Grounding and shielding connections can be made via several lugs close to the detector signal input connectors and on the metallic cover of the ROC (not shown in the figure).

3 The Read Out Card motherboard

The ROC motherboard functional block diagram is shown in figure 3. The blocks are described in detail below:

3.1 Tracking data conversion and transmission

This block is based on LVDS to CMOS converters and Gigabit Optical Hybrid (GOH) [6] module. The GOH performs data conversion from electrical to optical format and transfers the data streams to the next level of the system over an optic fiber through a 0.8-1.6 Gbit/s Ethernet 8B/10B parallel-to-serial encoder. One GOH mezzanine (figure 4) is used to send data from 16 VFAT hybrids to the Counting Room (CR). The GOH transmission, driven by the DATA Valid (DAV) signal generated by the master¹ VFAT, is enabled through MUX circuitry programmable via Slow Control Ring (SCR) [7].

The “Hit” information is coded in the form of binary channel data corresponding to the clock period selected by a first level trigger (LV1A) signal. On receipt of a trigger (generated after a given latency period), the binary data, the time stamps and other information (i.e. ChipID, CRC) are packed into a 192-bit data packet.

¹The master DAV can be selected from four available sources, respectively the first anode and the first cathode VFAT of each of the 2 CSC chambers managed by the ROC.

Figure 4. GOH mezzanine.

Figure 5. VFAT trigger mezzanine.

3.2 Trigger data transmission

This block is based on LVDS to CMOS converters, VFAT Trigger Mezzanine (VTM, figure 5) and two GOH modules for the optical transmission to the CR. The GOH transmission can be enabled via SCR and sourced by several devices.

Since the trigger signals are sent every clock cycle a time reference has to be included in the trigger data stream to facilitate recovering the correspondence between the event and the transmitted bits. This is done from the fast command Bunch Crossing 0 (BC0) by the VTM. The VFAT on board decodes the BC0 signal and provides this to a circuit which disables the GOH's DAV signal upon reception of the BC0 for the duration of one clock cycle. This will be recognized in the counting room providing the time reference.

3.3 Clock and fast commands

This block is based on a PLL25 chip [8], a QPLL and a number of clock and command distribution circuits. It provides synchronous clock and commands to each component on the board including the VFAT chips on the FE hybrids. It extracts and distributes a three bits coded fast command (LV1, BC0, Calib, Resync) from the LHC clock main system and set a programmable latency period (up to 6.4 μ s). The circuitry allows the equalization of the clock timing for the anode and cathode hybrids which are connected with different cables length.

Figure 6. CCUM mezzanine.

3.4 Slow control ring

This block is based on CERN Communication and Control Unit CCUM mezzanine [7] (figure 6). This module is connected to the control loop² (DOHM - FEC) via two 20 pins 3M high speed connectors. The control logic block provides 16 I²C interface channels and one 8 bit bidirectional parallel control port.

All the system parameters (i.e. FE hybrid values, clock latency) are sent to the devices via I²C, while GOHs power cycle, GOHs status, Data and Trigger GOH sources, Soft and Hard Reset are managed via the parallel port. A skip fault architecture for additional redundancy based on the doubling of signal paths and the possibility of bypassing interconnection lines between CCUM is also implemented.

3.5 Auxiliary debugging port

A spy test port is foreseen on the ROC board: all the front-end connections are routed to dedicated connectors to which one may plug a piggy-back programmable custom mezzanine (SPYME) equipped with a Xilinx FPGA type XC3S1500FG456. The FPGA emulates the DAQ system located in the CR and allows to remotely test all the ROC functionalities via a USB 2.0 port.

3.6 Low voltage distribution

The ROC needs to receive low voltage power at 2.5 V for its own operation, and for the operation of the hybrids. Independent PCB layers are used for the analog and digital low voltages distribution to the hybrids, both powered at 2.5 V. The total currents drawn are respectively 1.6A and 3.3A for the analog and digital voltages.

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²The TOTEM slow control system uses a ring topology configured as a local area network. The connections between ROCs are done electrically using differential lines (LVDS), the first and last CCUM of the chain are optically converted and connected to the master controller in the Counting Room.

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