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Switched capacitor DC-DC converter ASICs for the upgraded LHC trackers

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ABSTRACT: The High Luminosity Upgrade of the ATLAS Inner Tracker puts demanding requirements on the powering system of the silicon strip detector modules due to 10-fold increase of the channel count compared to the existing SemiConductor Tracker. Therefore, new solutions for the powering scheme must be elaborated. Currently two possible approaches, the serial powering and the parallel powering scheme using the DC-DC conversion technique, are under development. This paper describes two switched capacitor DC-DC converters designed in a 130 nm technology. For the optimized step-down converter, foreseen for the parallel powering scheme, power efficiency of 97% has been achieved, while for the charge pump, designed for the serial powering scheme, power efficiency of 85% has been achieved.

KEYWORDS: Analogue electronic circuits; Front-end electronics for detector readout

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1 Powering schemes considered for the upgraded ATLAS Inner Tracker

An upgrade of the LHC luminosity will require granularity of the silicon strip detectors in the Inner Tracker to be increased by about one order of magnitude compared to the present SemiConductor Tracker. Thus, using the present power distribution scheme with each detector module powered via a separate set of cables is not feasible at all. Therefore, two alternative powering schemes are being developed: serial powering of several modules on a stave, and powering of supermodules from a high voltage source with DC-DC converters on the detector modules. In either scheme some power management circuitry on the front-end ASICs will be required. In particular, switched capacitor DC-DC converters are the critical building blocks, which have to be implemented in the same technology as used for the front-end electronics, i.e. 130 nm CMOS as currently assumed.

In a possible serial powering scheme the supply voltage for each module in the serial chain is regulated by a shunt regulator with output voltage of 0.9 V. This voltage is used directly for supplying the digital part of the ABCN chip [1] and a higher voltage needed for the analog circuitry is obtained through a switched capacitor step-up converter (charge pump) and a serial voltage regulator.

In order to make the DC-DC scheme efficient the conversion factor should be high, at least about 10. Therefore the conversion is foreseen to be accomplished in two stages: the first stage, with a conversion factor of about 5, based on a buck converter with an air coil, will be implemented at the module level, and the second stage, with a conversion factor of 2, based on a switched capacitor step-down converter, will be implemented in the front-end ASICs.

In this paper we report on the designs of the switched capacitor step-down and step-up converters implemented in a 130 nm CMOS process.

2 Switched capacitor DC-DC step-down converter

The design of the switched capacitor converter is driven by the power efficiency. Thus, one has to analyze carefully the power losses occurring in the switching MOSFETs including conduction losses, switching losses, and gate charge losses. In the process of design optimization one has to find a proper balance between the three mechanisms of power losses. For example, since it is very important to keep the output impedance of the converter as low as possible and thus minimize

Figure 1: Schematic diagram of the switched-capacitor DC-DC step-down converter (a), and schematic diagram of the buffer used in step-down converter (b).

the conduction losses, the MOSFET switches have to be sufficiently large. However, increasing the dimensions of switches results in increase of the gate capacitance and thus in increase of the switching losses. Additionally, the switching losses are frequency dependent and the switching frequency is another factor to be considered [2].

A simplified schematic of the switched capacitor step-down converter proposed for the DC-DC powering scheme and optimized for the output current of 60 mA is shown in figure 1(a). The core of the design consists of four MOS transistors [3]. The dimensions of one p-channel transistor (M_1 ; $W/L_1 = 28.2 \text{ mm}/0.24 \text{ }\mu\text{m}$) and three n-channel transistors ($M_2 - M_4$; $W/L_{2/3} = 18.0 \text{ mm}/0.30 \text{ }\mu\text{m}$, $W/L_4 = 6.0 \text{ mm}/0.30 \text{ }\mu\text{m}$) have been chosen such that the conduction losses are minimized. The switching frequency is 1 MHz to minimize the switching losses. The flying capacitance C_X of 1 μF and the load capacitance C_L of 200 nF are implemented as external low-ESR SMD capacitors.

A practical circuit must include also four buffers, each one optimized for a given switching transistor, and a non-overlapping clock generator. Power losses in those circuits are not negligible and have to be taken into account as well in the overall power budget. A schematic diagram of the buffer is shown in figure 1(b). It consists of two separate inverter chains and a cross-coupled transistors M_1 and M_2 . This design allows us to prevent the conduction current in the last inverter (M_3 and M_4). Similar buffers were already used in the AMIS2 chip [4]. For the clock generator it is critical that the two complementary clocks are non-overlapping. In our design the two clock signals are separated by 3.5 ns, which has been found as an optimal value from the power efficiency point of view. The step-down converter is supplied with 1.9 V. For the nominal output current of 60 mA, the voltage at the output of the circuit is about 930 mV. This gives a power efficiency of 97%. A simulated transient response of the step-down converter is shown in the figure 2(a). The output voltage ripples are below 18 mV peak-to-peak. The presented results were obtained neglecting inductances of the bond wires. If a 1 nH inductance is included in the test bench one can observe fast voltage spikes of V_{p-p} up to 150 mV peak-to-peak.

The power efficiency and the output voltage as a function of the output current is shown in figure 2(b). For the given circuit parameters the power efficiency decreases with increasing output load current, but efficiency at a level of 97% can be reached also for higher output currents by proper design optimization. The output resistance extracted from the $V_{OUT}(I_{OUT})$ curve is less than 0.5 Ω . The corner analysis performed for the design shows that in the worst case the output voltage will be not less than 918 mV and the power efficiency will be at least 96% for the nominal

Figure 2: Time response of the DC-DC step-down converter (a), and dependence of the power efficiency and output voltage on the output current (b).

load current of 60 mA.

3 Switched capacitor DC-DC step-up converter

The step-up converter is based on the classical concept of a charge pump [5]. The concept can be implemented relatively easily in a CMOS technology and is employed for the generation of high voltage in battery powered devices. However typical required output currents in such circuits are very limited. In the serial powering scheme a charge pump with a low conversion factor of about 2, but a high output current, of a few tens of mA, should be implemented in the front-end ASIC.

A simplified schematic diagram of the developed voltage doubler is shown in figure 3(a) [6]. The core of the circuit is built of two low- V_t , cross coupled n-channel transistors (M_1 and M_2 , $W/L_{1/2} = 980 \mu\text{m}/0.15 \mu\text{m}$) and four p-channel transistors ($M_3 - M_6$; $W/L_{3/4} = 2000 \mu\text{m}/0.24 \mu\text{m}$, $W/L_{5/6} = 10 \mu\text{m}/0.24 \mu\text{m}$) of IO type i.e. allowing biasing up to 2.5 V. Three external, low-ESR SMD capacitors, 470 nF each, are used as the pumping capacitances ($C_{\text{PUMP}1/2}$) and the load capacitance (C_{LOAD}). These capacitors offer a good compromise between high capacitance value and relatively small package size (0603). Capacitors of higher values can be used in the future if they are available in small packages, like 0603. The capacitance C_{POL} is equal to 1 pF and is small enough to be integrated on a chip.

A critical aspect of this design is the driving capability of large serial p-channel switches M_3 and M_4 . In the classic charge pump maximum voltage available for switching transistor M_3 and M_4 would be the same as the input voltage, i.e. 0.9 V in our design. This limited voltage would result in relatively high ON resistance of switches M_3 and M_4 , and consequently in large power losses. A significant improvement of this aspect of the circuit has been obtained by introducing level shifter circuits [7]. A schematic diagram of the level shifter is shown in figure 3(b). Transistors M_1 through M_6 are 2.5 V transistors with a thick gate oxide. These transistors are potentially more sensitive to radiation effects, but they are required to cope with transient voltages across their gates exceeding 1.6 V. The circuit requires two supply voltages, 0.9 V and 1.55 V, later one taken from the output.

The load of the converter was simulated by two components: a resistor and a current sink (drawing 20% and 80% of the output current respectively), which represents in a first approximation typical behavior of the analog front-end circuit. The nominal output current was specified to be

Figure 3: The schematic diagram of the voltage doubler (a), and the schematic diagram of the level shifter used in the step-up converter (b).

Figure 4: Time response of the step-up converter (a), and the dependence of the power efficiency and output voltage on the output current (b).

about 30 mA. The voltage obtained at the output, for this current, is 1.55 V. The power efficiency of the circuit optimized for the nominal current is higher than 85%.

A transient response of the step-up converter is presented in the figure 4(a). In the simulation the input voltage was ramped up to 0.9 V during 50 μ s. The output voltage reaches its nominal value of 1.55 V after about 80 μ s. The measured voltage ripples on the output of the converter are less than 5 mV p-p if the inductances of the bond wires are ignored. Adding in the simulations a 1 nH inductance for each bond wire results in spikes up to 900 mV p-p.

The power efficiency and the output voltage as a function of the output current is shown in figure 4(b). Similarly to the step-down converter discussed before, there is a well defined dependence between the power efficiency of the converter and the output current. This effect is due to conduction losses, which depend strongly on the load current. The circuit has been optimized for a nominal current of 30 mA, but it operates well also for higher load currents, though with a lower power efficiency and a lower output voltage due to relatively high output resistance. The output impedance can be calculated from the $V_{OUT}(I_{OUT})$ curve of figure 4(b), and for this design is around 7 Ω . The corner analysis carried out for the switched capacitor step-up converter shows that in the worst case the lowest obtained power efficiency calculated for the nominal current (30 mA)

is not less than 81% and the output voltage does not drop below 1.49 V.

4 Conclusions

The designs of two switched capacitor DC-DC converters, step-down and step-up, have been worked out in a 130nm CMOS technology. Both designs have been optimized with respect to the power efficiency for the specific requirements driven by two possible schemes of powering detector modules in the ATLAS Upgrade Tracker. For the step-down converter a power efficiency of 97% has been obtained for an output current of 60mA and an output voltage of 930mV at switching frequency of 1 MHz. For the step-up converter a power efficiency of 85% has been achieved for an output current of 30mA and an output voltage of 1.55 V at switching frequency of 500kHz. The simulations including the inductances of the bond wire show that packaging of such circuit is very critical and packaging techniques like flip chip bonding, with small inductances should be considered for the future. The step-down converter occupies a silicon area of 0.12 mm^2 ($580 \times 200 \mu\text{m}^2$) and the step-up converter occupies an area of 0.04 mm^2 ($190 \times 200 \mu\text{m}^2$). In either case the area of the design is such that these blocks can be easily integrated on the front-end ASICs. The prototypes have been submitted for an MPW run.

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