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Status report on a MicroTCA card for HCAL trigger and readout at SLHC

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ABSTRACT: We present recent measurements performed using a prototype MicroTCA card for CMS-HCAL Trigger and Readout at SLHC. Our second generation prototype uses a Xilinx XC5VFX70T FPGA to perform the high-speed communication and data processing for up to eight Readout Module fibers that are streaming data at 4.8 Gbps each. The FPGA also uses two SFP+ optical interfaces at 6.4 Gbps each for data transfer to the Trigger System. A local DAQ interface in the FPGA communicates via Gigabit Ethernet with the MicroTCA MCH. Bit Error Rate Test (BERT) results and data integrity analyses are presented in challenging clocking environments including a legacy TTC system. In addition, the status of the IPbus concept for control of deeply embedded devices is presented.

KEYWORDS: Instrumentation for particle accelerators and storage rings - high energy (linear accelerators, synchrotrons); Hardware and accelerator control systems

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1 Upgrade requirements for CMS HCAL

CMS HCAL will require an upgrade of the instrumentation electronics to meet performance expectations of SLHC [1]. The proposed front end electronics upgrade will increase the ADC channel count by a factor of four (to approximately 36000 channels), but the number of fiber links will increase by less than a third. Since the HCAL front end readout modules transmit all ADC samples without compression, the current 1.6 Gbps data rate will have to increase to 4.8 Gbps. The University of Minnesota is performing research and development to achieve the required speed and stability of communication links in the CMS HCAL environment. Research into the use of the MicroTCA standard, including the appropriate controls architecture for such a system, has also been carried out.

The core component of the backend electronics will be a MicroTCA board which receives the data from the front end, calculates trigger primitives which are transmitted to the Level-1 trigger, and holds pipelined data for possible readout. The full upgraded system will require 150 of these cards. The MiniCTR2 is a MicroTCA board that evaluates the key elements of this concept but with reduced link counts and computational resources compared to the full requirements of the proposed upgrade.

2 MiniCTR2 architecture

2.1 FPGA

The basis for MiniCTR2 functionality is a Xilinx XC5VFX70T-1FFG1136C FPGA [2]. It supports 16 GTX [3] high-speed serial links. Although the datasheet states that the maximum data rate for the GTX links on parts with the slower “-1” speed rating is 4.25 Gbps, the FPGAs that we are using continue to perform well at 6.4 Gbps.

2.2 Fiber optics

Most of the high-speed inter-board communication takes place over multimode fiber at 850 nm optical wavelength. Electrical to optical conversion is performed with standard modules developed for commercial telecommunication and high-performance computing markets. Two SFP+ Optical Transceivers [4] are installed on MiniCTR2 and they can communicate at up to 6.4 Gbps. A SNAP12 transmitter [5] and a SNAP12 receiver are installed on MiniCTR2 and they can communicate at up to 4.8 Gbps on each of the 12 fibers in the SNAP12 package.

2.3 Clocks

MiniCTR2 has a flexible clock network that will support six different clock sources. One of the most important functions that the clock network must perform is the generation and distribution of the reference clocks for each of the GTX transceiver blocks on the FPGA. Communication performance of the FPGA is highly dependent upon the quality of the GTX reference clocks. A reference clock with high jitter will result in intermittent communication failures in the transmission of data from the front end, which in the HCal architecture will damage both the trigger and precision quantities reported by the calorimeter. MiniCTR2 uses a jitter-attenuating Si5319 any-rate clock multiplier/synthesizer from Silicon Laboratories [6] to generate a 320.64 MHz reference clock from a 40.08 MHz system clock. Although the phase of the reference clock relative to the system clock is not specified, the reference clock frequency is locked on to the system clock frequency, and the GTX transceivers use an internal data buffer to eliminate any dependence upon the reference clock phase.

2.4 PCB stackup

MiniCTR2 uses a relatively simple printed circuit board fabrication technology. Ten copper layers are used to create a board that has a thickness of about 0.062 inches, which conforms to the MicroTCA requirements. All vias in the board go through all layers of the board. Via holes are at least 0.010 inches in diameter. Minimum feature sizes on the board are 0.005 inches for lines and 0.004 inches for spaces. Top and bottom layers are configured with stripline traces that are 0.006 inches wide, supporting 6.4 Gbps communication without difficulty. Although this board fabrication technology is relatively mundane, the performance that has been achieved with MiniCTR2 seems impressive.

Figure 1. 40 MHz Clock Distribution for BERT.

3 Bit Error Rate Test (BERT) results

3.1 Clock distribution

In order to keep the number of link-induced errors in the HCAL system at a level which does not affect overall CMS data quality, a bit error rate of 10^{-15} will be required. The Xilinx IBERT design was used in the FPGA to perform Bit Error Rate Tests. IBERT data was exchanged between two MiniCTR2 boards that were supplied clocks from two different branches of a realistic clock distribution system. See figure 1. The two different clock distribution branches share the same 40.08 MHz TTCci generator, and therefore have the same mean frequency, but their clock jitter characteristics are different. The Si5319 clock multiplier on each MiniCTR2 board must lock onto the 40.08 MHz system reference and produce a low-jitter 320.64 MHz reference to the FPGA.

3.2 Clock jitter analysis

Clock period histograms for both 40.08 MHz clock distribution branches were created by a Wavecrest SIA-4000 signal integrity analyzer [7]. One of the branches had a well behaved distribution of clock periods with a peak-to-peak jitter of 135 ps. The other branch had a multiply-peaked distribution of clock periods with a peak-to-peak jitter of 516 ps. The peak-to-peak difference in clock periods between the two clock branches was measured to be 780 ps. These jitter levels, as delivered to the inputs of the Si5319, are very large and can be considered as worst-case for a clock delivered to the MicroTCA crate. The jitter levels are in particular much too large for stable high-speed link operation. The Si5319 part very successfully reduces the jitter, as is evidenced by the BER results described below.

3.3 BERT results

The Xilinx IBERT design for the FPGA used a 31-bit PRBS to generate the data streams. All four SNAP12 channels successfully ran for more than 24 hours without a single error at 4.8 Gbps, and both SFP+ channels ran for more than 24 hours without a single error at 6.4 Gbps. One of the SFP+ channels had a 10 dB optical attenuator installed and still performed without errors. See figure 2. The communication from board to board over the short MicroTCA backplane was also error free even at speeds above 6 Gbps. This signal path included two Molex right-angle MicroTCA connectors and traces about 7 inches long on the FR4 backplane. This result establishes an error rate better than 10^{-15} on these links taken as a whole.

Figure 2. Bit Error Rate Test Fixture.

Figure 3. Data Integrity Analysis Diagram.

Figure 4. PRBS-7 Eye Diagram at 4.8 Gbps.

4 Data integrity analysis

Data integrity analysis was performed on a 4.8 Gbps 7-bit PRBS SFP+ data stream from MiniCTR2 using a ScopemaX from Gigamax Technology [8]. A special board was constructed to interface the electrical inputs on the ScopemaX with an SFP+ receiver, which performed optical-to-electrical conversion. See figure 3.

An “Eye Diagram” for the data stream was created by ScopemaX for each of the two 40.08 MHz clock distribution branches that were discussed above. See figure 4. The “eye” has a large opening, but the diagrams clearly show some significant jitter on the rising and falling edges of the “eye”. The quality of the diagram was not very sensitive to the choice of the 40.08 MHz clock distribution branch.

The ScopemaX acts as a TDC, measuring the time between subsequent crossings of the differential signal for a large sample of transitions. This technique preserves short-term correlations more effectively than an estimate based on the average transition width. For one choice of the 40.08 MHz clock distribution branch, the data-dependent jitter in the 4.8 Gbps PRBS-7 data stream showed a maximum error of 17.73 ps and a minimum error of -13.31 ps. The peak-to-peak data-dependent jitter was therefore 31.04 ps. Data dependent jitter, however, is only one component of total jitter. For a 3086-bit sample of the 4.8 Gbps PRBS-7 data stream, the total jitter showed a maximum error of 36.27 ps and a minimum error of -31.88 ps. The peak-to-peak total jitter was therefore 68.15 ps, slightly more than twice the peak-to-peak data-dependent jitter. Once again, these values were not very sensitive to the choice of the 40.08 MHz clock distribution branch. The insensitivity to the choice of clock distribution branches is seen as a good sign that the Si5319 clock multiplier is not transferring jitter from the 40.08 MHz system clock onto the 320.64 MHz FPGA reference clock.

5 Control of MicroTCA cards

The MiniCTR2 is also serving as a testbed for research into control software and firmware concepts for use in a MicroTCA environment. In particular, the natural control path in MicroTCA is based on Ethernet, which is a very different protocol than the familiar bus-like protocols (e.g. VME) widely used in HEP. The bus paradigm is very natural to many hardware designers, more natural than packet-based concepts, which suggests the development of a standard technique for an application layer above Ethernet to provide a bus abstraction.

“IPbus” is a research and development effort in CMS that uses Ethernet to control deeply embedded devices such as FPGAs through the MicroTCA MCH Ethernet switch. The developmental standard is organized around the concept of a virtual A32/D32 bus inside each device. External applications can perform READ, WRITE, and RMW transactions on this bus by way of Internet Protocol (IP) packets. Applications can package multiple bus transactions into a single Ethernet packet to minimize communication latency and maximize communication bandwidth. An initial FPGA demonstration using UDP/IP has been completed, and can transfer about 20 MBytes/s of control/data to an FPGA when doing block transfers. The design occupies approximately 3% of the Xilinx XC5VFX70T in MiniCTR2. Although the user protocol supports TCP/IP, the demonstration FPGA firmware only supports UDP/IP transfers. This concept and implementation has been successfully demonstrated by the MiniCTR2 communicating via the Ethernet switch in the CMS-MCH (“DTC”) and a MicroTCA backplane.

In a related hardware effort, a modified MiniCTR2 has been designed to move the MMC management microcontroller to a mezzanine and study the use of on-board PHY-less Ethernet switch chips on MicroTCA cards. The addition of an Ethernet switch on a MicroTCA card would allow uniform IPbus access to multiple FPGAs and microcontrollers without one device acting a bridge to the rest. Such uniform access could improve communication bandwidth and system robustness compared to a system where the Ethernet is bridged by a programmable device onto a custom local bus.

6 Conclusion

A second generation prototype MicroTCA card for CMS-HCAL Trigger and Readout at SLHC has been evaluated. The Xilinx Virtex-5 FPGA, clock distribution components, and commercial fiber optic interfaces meet our performance expectations for communication at 4.8 Gbps and 6.4 Gbps even with low quality 40.08 MHz system clocks and relatively simple circuit board technology. In addition to the results from the hardware prototype, the results from initial usage of Ethernet to control deeply embedded devices has also been encouraging.

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