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2010 JINST 5 C12001

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TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2010,
20–24 SEPTEMBER 2010,
AACHEN, GERMANY

The ALICE Silicon Pixel Detector: commissioning and performance optimization

C. Cavicchioli¹

*CERN, European Organization for Nuclear Research
CH-1211 Geneva 23, Switzerland*

E-mail: costanza.cavicchioli@cern.ch

ABSTRACT: This paper describes the tests and measurements made during the final commissioning with beams of the ALICE Silicon Pixel Detector (SPD) in the first year of operation and the optimization of its performance. The ALICE Silicon Pixel Detector (SPD) is the innermost detector of the ALICE experiment and therefore plays a key role for vertexing and tracking. It consists of two cylindrical layers of pixel detectors, with a total of $\sim 10^7$ pixels. The detector provides a prompt trigger signal that contributes to the first level trigger decision in ALICE. The trigger signal has been extensively used in the first trigger level of the ALICE experiment for recording data of proton-proton collisions at energies of 900 GeV, 2.36 TeV and 7 TeV.

KEYWORDS: Particle tracking detectors (Solid-state detectors); Detector alignment and calibration methods (lasers, sources, particle-beams)

¹On behalf of the ALICE Silicon Pixel Detector project.

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1 System description

The ALICE experiment [1] at the CERN Large Hadron Collider (LHC) is optimized to study the properties of strongly interacting matter in heavy-ion collisions, at extreme temperature and energy density conditions. The Silicon Pixel Detector (SPD) [2], of which some details are shown in figure 1, is the innermost detector of the ALICE experiment, and it plays a key role for the vertexing and tracking capabilities: it is able to track particles with a precision of $12\ \mu\text{m}$ in the transverse plane over a wide range of transverse momenta ($100\text{ MeV}/c$ to $100\text{ GeV}/c$).

The SPD is a barrel detector with two layers at average radii of 39 mm and 76 mm from the beam axis and a length of 280 mm along the beam axis. It consists of 120 detector modules, called half-staves. Each of them includes two silicon pixel sensors, each sensor is bump bonded to 5 front-end readout chips made in $0.25\ \mu\text{m}$ CMOS process. The front-end chip contains 8192 pixel cells with a pixel size of $425 \times 50\ \mu\text{m}^2$ ($z \times r\phi$), organized in 32 columns and 256 rows; in total there are 9.83×10^6 pixels in the SPD. The 10 front-end chips of each half-stave are connected to a Multi Chip Module (MCM) that provides timing, control and trigger signals to the chips; it also performs the readout of the front-end chips, sending the data to the off-detector electronics housed in the control room (router boards).

Figure 1. SPD (right) and one half-stave (left).

Figure 2. Temperature distribution of the powered half-staves.

Each of the 1200 front-end chips of the SPD provides a prompt trigger signal, called Fast-OR, which is generated when at least one pixel inside the chip is hit by a particle. The PItel Trigger (PIT) system [3] processes the 1200 Fast-OR signals with 10 user-defined algorithms at the same time, and produces 10 trigger outputs according to these predefined algorithms that are sent to the ALICE Central Trigger Processor (CTP) for the first trigger level (Level 0) decision. The algorithms are based on multiplicity thresholds, and they are implemented using boolean functions.

2 System commissioning

2.1 Detector

The first phases of the detector commissioning, including the auxiliary services, have been presented in previous publications [4]. The overall power dissipated in the SPD front-end and MCM electronics is ~ 1.35 kW. Due to the low mass of the system, the material budget is only $\sim 1.1\%$ X_0 per layer, without any cooling the detector temperature would increase by $1^\circ\text{C}/\text{s}$. An evaporative cooling system based on C_4F_{10} allows to operate the detector at ambient temperature. The coolant runs in capillaries which are placed under each half-stave in thermal contact with them.

Since the installation in the ALICE cavern in 2007, the cooling system has been upgraded in order to improve its performance. The actions taken include the counter-flow-wise cleaning of all the lines, the re-routing of the input lines, the installation of heat exchangers and additional monitoring devices for temperature and pressure measurements. About 100 half-staves out of 120 are steadily operated, the others cannot be powered due to localized lower efficiencies of the cooling system; the average working temperature of the modules is 29.7°C (see figure 2).

To ensure a good detector performance (see also [5]), the response uniformity of front-end chip matrix has been checked, and the configuration has been tuned accordingly in order to reduce noisy and inefficient regions. This is done using an internal pulser that generates a signal of known amplitude sent to each pixel. The response has been optimized tuning a subset of the 42 internal Digital-to-Analog Converters (DACs), 8 bits each, in each front-end chip (namely current and voltage references), searching for the best compromise between detector performance and power dissipation of the chips. The matrix uniformity has also been analyzed with data coming from beam injection tests and p-p collisions. During this study the noisy pixels are also identified. A

Figure 3. Threshold distribution before (left) and after (right) the DAC tuning. Increasing the DAC value corresponds to lowering the analog threshold value.

pixel is defined noisy if it fires more than the 0.2% of the total number of triggers during a run in self triggering mode. After the optimization, the percentage of the noisy pixel cells is $\sim 0.09\%$, which is within the specifications of 0.1% .

The detector calibration procedure includes also the determination of the minimum readout threshold value. The threshold of the front-end chips is set by an internal DAC; an automatic scan procedure has been implemented inside the SPD Front End Device (FED) server to find the minimum threshold that can be applied to each of the 1200 front-end chips. The scan loops over the digital threshold values, checks the signal coming from the chips over a certain time interval, and finds the lowest value at which the chip can be operated without noise. The result of the optimization procedure is shown in figure 3. The threshold configuration has been monitored over time and found to be stable in the last 5 months.

In addition to the threshold optimization, the equivalent charge deposited in the detector has to be determined for each digital DAC value used. A scan has been implemented in the FED servers of the SPD: it loops through a range of amplitudes of the internal pulser, sending a predefined number of triggers per step, and it creates an efficiency curve per pixel calculating its mean and sigma values. The scan was performed on the full detector, and table 1 shows the results of 95 half-staves: for each threshold value it gives the corresponding number of chips and the average mean and sigma values of the efficiency curves. The equivalence between voltage amplitude of the internal pulser and the number of electrons is determined using a conversion factor of $66 e^-/mV$ found after tests in the laboratory using a ^{66}Fe source. The nominal threshold of 200 DAC units corresponds to about 2000 electrons, which is well below the charge released by a MIP in the $200 \mu m$ thick SPD sensor (~ 16000 electrons) and also below the minimum expected signal (~ 6000 electrons).

The same scan was also performed in the laboratory on a test station equipped with 6 half-staves. These half-staves were configured with the same settings of current and voltage references, and the threshold DAC was set at 200. With these parameters, the resulting mean threshold value and RMS are, respectively, 29.7 mV and 3.6 mV; this is well in agreement with the value found on the chips of the detector running in ALICE with the same settings.

Table 1. Mean threshold values and their conversion in corresponding electrons.

DAC [a.u.]	# chips	Mean thr [mV]	RMS [mV]	Mean thr [e^-]	RMS [e^-]
180	12	41.3	1.9	2730	120
185	29	37.8	2.0	2500	130
190	122	35.2	1.9	2320	120
195	233	33.0	1.9	2190	120
200	554	30.0	1.7	1980	110

Table 2. Trigger efficiencies for the four possible phases of collisions with respect to the SPD clock, before and after the SPD clock fine adjustment. The errors are of the order of 0.002%.

	Phase 1	Phase 2	Phase 3	Phase 4
before tuning	99%	99%	99%	80%
after tuning	99%	99%	99%	97%

2.2 Pixel Trigger

The overall latency of the Pixel Trigger system, from the particle interaction to the CTP input, can range from 780 to 880 ns depending on the phase relationship between the collisions and the clock; indeed, as the SPD clock has a frequency of 10 MHz while the LHC clock is 40 MHz, there are four possible time slots (phases) inside one SPD clock cycle when the collisions may happen. The trigger efficiency has been evaluated for each of the four positions of the particle interactions with respect to the SPD clock with data from 900 GeV and 7 TeV collisions. Table 2 summarizes the results.

The last position (Phase 4) is the closest to the SPD clock edge, thus small jitters can delay the Fast-OR signals to the subsequent clock cycle, resulting in a lower trigger efficiency. The alignment of the SPD clock with respect to the LHC clock has been studied moving the position of the SPD readout window, synchronous with the clock, with respect to the bunch crossing and so the p-p collisions. For each position of the readout window, the average number of hits was measured: from these measurements it was found that the optimal condition is obtained delaying the SPD clock by 8.5 ns. Applying the shift to the SPD clock, a substantial increase of the trigger efficiency for the last phase is observed.

After the optimization of the detector configuration, also the Fast-OR circuitry inside each readout chip had to be calibrated again. The calibration of the Fast-OR requires a tuning of 5 DACs per chip to maximize the efficiency and minimize the noise of the circuitry. An automatic calibration procedure has been implemented [6]: it scans the DACs values and checks the Fast-OR efficiency for each chip, identifying a subset of values with 100% efficiency and finding the optimum DAC combination in this region. The calibration requires the simultaneous operation of the SPD readout and control system, and the PIT system. To date, 98.7% of the powered chips are calibrated with this procedure.

3 Performance with beams and cosmes

Since 2008 the Pixel Trigger has been extensively used as a trigger detector during cosmic runs and with beams. The algorithm used to collect cosmic events is a top-bottom-outer-layer coincidence: the output of the PIT is active when a particle activates at the same time at least two chips, one on the upper half of the outer layer, and the other on the lower half of the outer layer. The tracks acquired with this algorithm show a trigger purity of more than 99.6%, and the average trigger rate is 0.18 Hz, in agreement with the expected cosmic flux in the ALICE cavern and with the MonteCarlo simulations [2].

During the cosmic runs, $\sim 10^5$ events were collected without magnetic field and $\sim 10^4$ events with magnetic field; these data have been used to study the alignment of the SPD active volumes [7]. The alignment was studied reconstructing the cosmic rays as back-to-back tracks starting from a pseudo-vertex around the nominal interaction vertex region along the cosmic ray trajectory. The distribution of the track-to-track distance on the transverse plane in the middle of the SPD after the alignment corrections has a spread of $49\ \mu\text{m}$; the resulting spatial resolution is $13\ \mu\text{m}$, that has to be compared with the intrinsic resolution of $11\ \mu\text{m}$ that was obtained from the simulations under ideal conditions.

The SPD trigger provides a fundamental contribution to the ALICE L0 trigger decision during p-p collisions. Two algorithms are used: the minimum bias algorithm, which generates a trigger as soon as at least one chip is activated by a particle, and a high multiplicity algorithm, which generates a trigger if at least a predefined number of chips is activated.

4 Conclusions

The Silicon Pixel Detector is successfully taking data with colliding proton beams and the Pixel Trigger system is providing ALICE with a L0 trigger contribution for event selection and background rejection. The detector performance has been optimized in several following steps: the cooling system was improved, calibration scans were developed and adopted to study the chip matrix response and to determine the optimal readout threshold. The timing of the clock signal was also studied and the detector efficiency optimized. About 98.7% of the powered chips are contributing to the trigger decision, with trigger efficiencies of $\sim 99\%$. The SPD is ready for the next long proton runs and for the forthcoming heavy-ion collisions.

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