EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

CERN-EP/79-25
27 March 1979

A FAST PROGRAMMABLE COINCIDENCE MATRIX

W. Flauger

DESY, Hamburg, Fed. Rep. Germany

ABSTRACT

The design and performance of a fast coincidence matrix of size 25×36 is described. The matrix is programmable either manually or by computer control via a CAMAC output register. The input-output delay is 28 nsec.

(Submitted to Nuclear Instrum. Methods)

1. INTRODUCTION

The specific physics aim of a high-energy physics experiment requires a fast preselection of event candidates of a special type. This preselection is normally based on the space correlation of signals from scintillation counter hodoscopes, wire chambers, Čerenkov counters, or shower counters. The time delay of such a trigger signal relative to the interaction time of the particles must be kept small. The possibility to fire spark chambers or streamer chambers and the cost of delays for counter and chamber signals disfavour trigger delays of more than about 500 nsec.

The correlations between the detector signals are performed either by comparing the content of fast memories with the bit pattern from the detectors, or by a combination of logic gates. With a fully decoded memory of 2^n bits a simple logic unit can be built up¹⁾, which provides any function of the form $OUTPUT = A_1 \cdot A_2 \cdot \dots \cdot A_n$. As the size of the required memory, however, is increasing exponentially with the number of inputs A_i , n is limited to 12 for present fast ECL memories^{*)}.

If the number of detector signals becomes considerably larger, only two- or three-dimensional correlations can be performed with a reasonable amount of electronics. A three-dimensional large system using memory integrated circuits is described elsewhere²⁾. The memory used had a size of $16 \times 16 \times 2$ bits with 16X and 16Y direct address lines and two data inputs. With this memory cell it was possible to build up a matrix of $128 \times 128 \times 2$ bits on one single printed board. As fast memories without decoding of the address lines exist only up to a size of 4×4 bits, the memory integrated circuit used for this purpose was a special development²⁾.

Combinations of electronic gates built up by diodes, transistors, ECL logic or PLAs are widely used to generate trigger signals. The matrices are either fixed-wired or they are programmable manually or by computer control. In this paper we describe a fast programmable coincidence matrix of size 25×36 . The matrix was developed as a part of the trigger system of the NA2 experiment at the CERN SPS.

*) Fairchild, F 10470.

2. GENERAL DESCRIPTION OF THE MATRIX

The block diagram of the matrix is shown in Fig. 1. The X and Y inputs are twofold with an OR behind the NIM-ECL converters. The X channels for which the coincidence conditions are fulfilled are repeated on double NIM outputs for further decisions. Two extra inputs ΣY and ΣX open all Y or all X inputs respectively. These inputs are used for test purposes only. A common OR of all 900 coincidences is available with a high fan-out capability. Each coincidence element consists of a threefold coincidence with one X, one Y, and one programming input. The status of the programming inputs is displayed on a LED matrix at the front plate. The programming unit consists of a switchboard of 900 dual in-line switches and of a 900-bit shift register which can be loaded via a commercial CAMAC output register^{*)}. With a single switch the programming mode is switched either to the manual mode or to the CAMAC mode.

3. SPECIAL DESCRIPTION

The distribution of electronic functions over several printed boards is shown in Fig. 2. The fast part of the coincidence matrix is built up with the ECL 10000 family. The terminating resistors of $51\ \Omega$ at the inputs and between the gate interconnections ($100\ \Omega$ resistor arrays to -2 V) are omitted in this drawing. All input and output signals are connected via Lemo RP.00 or RPL.00 connectors.

3.1 Card No. 1 and card No. 2

These two cards contain the NIM to ECL converters. They differ only by the number of input channels. Corresponding inputs are interconnected via a wired-OR at the outputs of the MC10190. All outputs from these two cards are connected to card No. 3 via Scotchflex flat cables. To ensure good propagation characteristics on the flat cable connections at least one strip between two signal strips is connected to ground.

3.2 Card No. 3

This card distributes the signals over 6 coincidence cards. The 36X inputs are divided into 6 groups of 6 inputs each. The channels of each group are directly

^{*)} SEN, OR2027.

connected via card No. 3 to the coincidence card. The 25Y inputs are fanned out individually on this card. The gates used as fan-outs are mounted on sockets. Thus differences in transit time of individual channels can be reduced by inserting either an MC10111 or MC10211 gate, which differ in transit time by about 1 nsec. The connections between card No. 3 and cards No. 4 are performed via 64-pin connectors*).

3.3 Card No. 4

The 6 coincidence cards contain mainly the fast threefold coincidences and the TTL shift registers. Each of the 6X inputs $X(n)$, $n = 1, 2, \dots, 6$, is fanned out by two MC10111 gates. The 6 outputs from these gates are driving the 25 inputs of the coincidences $X(n) \cdot Y(m)$, $m = 1, 2, \dots, 25$. Owing to space considerations on the printed board the coincidences $X(n) \cdot Y(m)$, $m = 1, 2, \dots, 25$, are built up by MC10121 gates and the remaining coincidence $X(n) \times Y(25)$ by MC10100 circuits. The OR of these 25 coincidences $\sum_{i=1}^{25} Y(i) \cdot X(n)$ is performed by MC10110 gates together with one wired-OR connection. From each coincidence card 6 signals of the form $\sum_{i=1}^{25} Y(i) \times X(n)$, $n = 1, 2, \dots, 6$, are fed to the ECL to NIM converter at card No. 6 via flat cables. In addition, there exists a common OR of all 150 coincidences of the form $\sum_{i=1}^{25} \sum_{j=1}^6 Y(i) \cdot X(j)$.

The programming inputs of the fast coincidences are connected to the individual bits of SN74164 shift registers. The ground input to the shift registers is connected to the ECL power supply of -5.2 V and the VCC input is connected to ground. In addition, all programming inputs are connected via flat cables to the front plate (card No. 5).

3.4 Card No. 5

The front plate contains 900 LEDs, 900 dual in-line switches, and 900 diodes. The dual in-line switches are mounted on wire-wrap sockets. The flat cable connectors arriving from the coincidence cards are directly connected to the wire-wrap pins of these sockets. The LED display of 25×36 LEDs is built up by yellow arrays** of 5 LEDs each. As diodes the 13 clamping diodes of SN74S133 Schottky gates were used.

*) Burndy PI64B20P00F00, Burndy PI64B20R00M00.

**) Siemens LD485

3.5 The programming mode selection

As shown on the left side of Fig. 2, the programming mode can be changed between the manual and the CAMAC mode with one single switch. In the manual mode point B at the front plate is connected to ground, the TTL power is switched off and point A at card No. 4 is connected to -5.2 V. In this mode the current from point A through the 620 Ω resistor will flow either through the LED, or by closing the dual in-line switch, through the diode to ground. As the forward voltages of the LED and the diode are close to the low and high levels of the ECL logic, this voltage can be directly connected to the ECL gate input. In the CAMAC mode a TTL bit in the low status will drive the LED via the 430 Ω resistor and will generate an ECL low level. The TTL bit in the high status represents a high impedance current sink for the current from point A. The voltage at A of -0.8 V will therefore generate an ECL high level.

3.6 Card No. 6

The ECL to NIM converters of the X outputs are shown in Fig. 3 for one channel. Each channel has two individual outputs. The unused outputs must not be terminated.

3.7 Card No. 7

This card contains the common OR outputs and the programming interface. Figure 4 shows the common OR together with the ECL to NIM converters. The OR signals of the 150 coincidences at each coincidence card are connected via flat cables to two MC10210 gates at card No. 7. The outputs from these gates are driving 8 ECL-NIM converters A-H via MC1660 gates. One of the ECL-NIM converters is shown in detail in Fig. 4. As the whole matrix is d.c.-coupled the pulse width of the outputs A, B, C, D is given by the time overlap of the input pulses. The outputs E, F and G, H are continuously variable in width with the two corresponding potentiometers within a range of 5-20 nsec. The two pulse-forming devices are built up by two MC1692 line receivers K and L, together with the corresponding MC1660 gates. Owing to the quite high current of the bias supply voltage VBB, this voltage is stabilized by the line receiver M.

The programming interface circuit is shown in Fig. 5. The clock signal arriving from the CAMAC output register is converted from NIM to TTL. The signal is delayed by 0.5 μ sec and shaped by the SN74123 monostable multivibrators. After an amplifier the clock signals are fed to all clock inputs of the SN74164 shift registers on card No. 4.

The data input is also converted to TTL and then fed to the bit corresponding to the coincidence $X(36) \cdot Y(25)$. For each X value the data string is shifted in the direction of decreasing Y inputs up to the bit $X(1) \cdot Y(1)$. The data output from this bit is available in both polarities as NIM levels.

3.8 Power supply

The power consumption of the matrix is 20 A on the -5.2 V line and 6 A on the -2.0 V line. For both voltages a common switched 40 A power supply was used. The -2.0 V are generated by 8 parallel MC7902CP voltage regulators driven by the -5.2 V*) power supply.

3.9 Housing

Figure 6 shows how the printed boards and the power supply are assembled inside a commercial chassis of 7 units height. The input cards Nos. 1 and 2 and the output card No. 6 are directly connected to the front card No. 5.

4. MATRIX PERFORMANCE

The intrinsic time propagation delay together with the double-pulse resolution of the matrix are shown in Fig. 7 for one single channel. A double pulse with a distance of 8 nsec between the two pulses was connected to one $X(n)$ and one $Y(n)$ input. The middle trace shows the output pulses at the repeated output $X(n)$ and the lower trace the pulses at the total OR output. The intrinsic delay for this coincidence channel is 24 nsec for the repeated output and 27 nsec for the total OR output. The double-pulse structure, corresponding to a frequency of 125 MHz, is well resolved by both outputs.

Owing to differences in the propagation delays of the ECL gates and to differences in the interconnections on the printed boards, the intrinsic delays for all

*) The recommended minimum input voltage given by the manufacturer is -7.2 V. The required stability, however, on the -2.0 V line was easily achieved with an input voltage of -5.2 V.

900 coincidences are significantly different. The distribution of the intrinsic delays between the inputs and the total OR output is shown in Fig. 8. Each of the 900 coincidence channels was fired 5 times, and the time spectrum between input and output was measured with a time-to-digital converter.

A summary of the electronic specifications is given in Table 1.

5. CONCLUSION

A large programmable coincidence matrix has been developed for use in high-energy physics experiments. The main requirements on the matrix were short propagation time delay and flexibility. With several matrices of this type it is possible to set up a trigger system either by a parallel or by a serial connection of matrices. For serial connection only those channels which fulfil the preceding coincidence conditions are transferred to the next matrix. As the bit pattern of the matrices in a trigger system normally shows up as a simple geometrical figure, the individual displays at the matrices ensure a rough continuous control of the trigger system status.

We are grateful to H. Weiss and G. Singer for their assistance concerning electronic tests and the mechanical construction.

REFERENCES

- 1) S.R. Amendolia, E. Bertolucci, U. Bottigli, C. Bradaschia, L. Foà, A. Fucci,
A. Giazotto, M. Giorgi, M. Givoletti, P. Lucardesi, A. Menzione, D. Passuello,
M. Quaglia, L. Ristori, L. Rolandi, P. Salvadori, A. Scribano, R. Stanga,
A. Stefanini and M.L. Vincelli, Nucl. Instrum. Methods 147 (1977) 587.
- 2) E.D. Platner, J.R. Bensinger, A. Etkin, K.J. Foley, J.H. Goldman, M.A. Kramer,
S.J. Lindenbaum, W.A. Love, T.W. Morris, S. Ozaki, A.C. Saulys, C.D. Wheeler
and E.H. Willen, Nucl. Instrum. Methods 140 (1977) 549.

Table 1

Electronic specifications

Minimum input pulse width	4 nsec
Operation frequency	d.c. to 125 MHz
Propagation delay to repeated outputs	25 nsec
Propagation delay to OR outputs	28 nsec
Time jitter between all channels (σ)	± 1.3 nsec
Total time jitter between all channels	± 3.5 nsec
Rise- and fall-times at the outputs	1-1.5 nsec

Figure captions

- Fig. 1 : Block diagram of the matrix.
- Fig. 2 : Distribution of the electronic function over the printed boards.
- Fig. 3 : One of the 36 ECL-NIM converters for the X outputs.
- Fig. 4 : The common OR outputs. One of the ECL-NIM converters is shown in detail.
- Fig. 5 : The programming interface.
- Fig. 6 : Housing of the printed boards and the power supply.
- Fig. 7 : Input and output pulses, a) input pulses, b) repeated X output, c) common OR output. The horizontal scale is 5 nsec/unit and the vertical scale 0.5 V/unit.
- Fig. 8 : Spectrum of the transit time jitter for all 900 coincidences between the inputs and the common OR output.

Fig. 1

Fig. 2

Fig. 3

Fig. 4

Fig. 5

Fig. 6

Fig. 7

Fig. 8