NEW DEVELOPMENTS IN TIME AND PULSE HEIGHT DIGITIZERS

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Abstract

Recent progress in LSI circuits has brought monolithic flash ADCs and RAMs, capable of operating up to 100 MHz. They open new possibilities to designers of time and charge digitizers. A simple technique to increase the dynamic range of a 6 bit/30 MHz low cost ADC has been developed. The transfer function is approximately logarithmic and covers a 9 bit dynamic range. An application of the same ADC to measure directly the charge division in a sense wire of a wire chamber is discussed. A fast 256 x 4 ECL RAM has been tested as a buffer memory of the ADC but also as the main element in time digitizers.

Introduction

The analogue-to-digital converters (ADC) and time-to-digital converters (TDC) used in nuclear physics research are generally based on converting the amplitude or the time of arrival of a fast signal to a charge on a capacitor and then digitizing this charge off-time. This digitizing may take several hundreds of μsec , depending on the system clock frequency and the required resolution. The process of conversion-storage-digitizing suffers from the classical problems of analogue circuits such as temperature sensitivity, non-linearity, pedestal, etc.

Since drift chambers¹ have started to be implemented on a large scale in high energy physics experiments, the application of TDCs have taken on a new dimension. In view of the high numbers of channels involved, economic solutions requiring minimal monitoring and calibration have become indispensable. It will be clear that direct digital or real-time converters offer the best solution. Systems based on ECL 10 K counters and memories are now in operation in many laboratories. In order to improve the resolution beyond the counter clock-period either multiphase clocks or interpolators are applied to obtain resolutions of a few nanoseconds.

In recent years a drastic increase has also occurred in the number of ADC channels in high energy physics experiments. There are often over a thousand photomultipliers in experiments with a calorimeter, where the signals from these photomultipliers have to be digitized. Another reason is the application of charge division in wire chambers for the measurement of a spatial coordinate. In both cases the required resolution is moderate, generally 6 to 8 bits. However, in the case of calorimetry, the energy loss due to ionization of various types of particles and particle showers has to be measured, which requires an ADC with a wide dynamic range. This can be solved by the brute force method of increasing the number of bits in the ADC, with its inherent complication of the circuit and a higher load on data processing and price. The resolution at the top end of the range also becomes unnecessarily high. Some other ways of solving the dynamic range problem while keeping the number of bits low are:

- two ADCs with moderate resolution per detector channel where one ADC receives only a small fraction of the signal, a costly method;
- give the ADC a non-linear response. For example,

by applying a non-constant discharge current in a Wilkinson type of ADC or by changing the discharge time counter clock frequency during the digitizing process;

- insert a non-linear (log.) amplifier in front of the ADC.

Recent progress in the domain of VLSI has made it possible to avoid the intermediate step of charge storage and do the conversion in real time, in tens of nanoseconds. Fully parallel "flash" ADCs and random access memories capable of operating up to 100 MHz are emerging and will completely change this branch of electronics. Alone or in combination they offer new and better solutions to the above-mentioned problems and a novel range of design possibilities. Some of them are described below.

The Fully Parallel or Flash
Analogue-to-Digital Converter

During this year, several video ADCs based on different principles have been described²⁻⁷ or announced.⁸⁻⁹ The fully parallel, multi-threshold or flash A/D converter (FADC) is, however, by far the most straightforward and the fastest converter of all.¹⁰⁻¹² Its speed is determined by the propagation delay of one comparator and a few logic gates. With the progress in VLSI technology it is now possible to put 255 fast comparators on a 261 x 264 mils area.⁵ Work is underway to make a 10 bit converter on one chip. Also the price level of this type of converter has gone down. A 6 bit version¹³ is now available for less than \$40.- in large quantities. This converter, the TDC 1014J, has been chosen as the basis for our development.

The flash converter TDC 1014J consists of 63 strobed differential comparators, a resistor string reference network, a 63 to 6 encoder, and an output latch (Fig. 1). One of the inputs of each comparator is connected in parallel to the signal input (VIN), while the other input of the comparator is connected to a reference voltage. The comparator has a bandwidth of 45 MHz and an acquisition time of 15 nsec. The reference voltages are developed in a resistor string between the terminals VRT and VRB. In the normal mode of operation, VRT is connected to 0 V and VRB to -1 V.

A clock signal (CONVERT) strobes the comparators on its rising edge. The 63 to 6 encoder is clocked by the falling edge of the convert signal and the coded output appears on the next rising edge. A clock rate of minimum 31.25 MHz is guaranteed for the best version.

The TDC 1014J has two components which contribute to the linearity errors: reference resistor non-uniformity and comparator offset voltages. The major portion of the non-linearity is contributed by the comparators producing a random code-to-code variation in threshold location.⁵

The specified linearity error is $\pm 0.4\%$ (≈ 0.25 LSB).

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$$H = 63 \frac{V_{IN} - V_{RB}}{V_{RT} - V_{RB}}$$

Dynamic Use of the Reference Voltage Chain of a Flash A/D Converter

It will be clear that linearity errors increase with smaller VRT-VRB, as the result of a measurement on a typical FADC in Fig. 2 shows.

An Adjustable Response Function for the Flash A/D Converter

$$H = 63 \frac{V_i}{aV_i + V_b} \quad (2)$$

(or in general mathematical terms $y = \frac{x}{ax+b}$).

$$V_i = V_{im} = \frac{V_b}{1-a} \quad (3)$$
$$X = \frac{1}{1-a} \quad (4)$$
$$R = \frac{6 \text{ bits}}{1-a} \quad (5)$$

It will be clear that for positive values of a a compressed response will occur, and for negative values an expanded one. Fig. 4a shows some normalized response functions for different values of a , obtained by a computer simulation.

Fig. 4a. Normalized non-linear response functions for different values of a .

For our application we have chosen $a = 0.92$ and $V_b = 0.16$ V. This gives a dynamic range of 1:776, and a response function as shown in Fig. 4b.

Fig. 4b. Non-linear response function for $a = 0.92$, $V_b = 0.16$ V and $V_{i_m} = 2$ V.

The general expression for the absolute bin or channel width can be derived from Eq. (2) and is given by:

$$\Delta V_i \sim \frac{(A V_i + V_b)^2}{63 V_b} \quad (6)$$

The resolution or relative bin width is given by:

$$\frac{\Delta V_i}{V_i} = \frac{(A V_i + V_b)^2}{63 V_b V_i} \quad (7)$$

The resolution when using a 6 bit FADC in the linear mode is shown in Fig. 5, which also shows the resolution of the same FADC for the values of $a = 0.92$, $V_b = 0.16$ V and $V_{i_m} = 2$ V. The expansion of the dynamic range from 6 to $9\frac{1}{2}$ bit clearly is at the expense of the resolution for high input values, which is generally acceptable.

Fig. 5. Curves showing the resolution of a 6 bit FADC in the linear mode and an applied non-linear mode.

Finally, a practical implementation is shown in Fig. 6 for negative input signals.

Fig. 6. The actual implementation to obtain non-linear response for negative input signals.

The above derived equations are applicable to any FADC of this kind; (3) and (4) are independent of the number of bits, while (1), (2), (5), (6) and (7) are proportional to this quantity.

The Flash A/D Converter as Analogue Divider

Because the reference voltage inputs can be driven by fast signals the FADC can be used as a fast voltage divider. In this application the normal signal input V_{IN} is connected to ground, and the input signals V_X and $-V_Y$ are connected to V_{RT} and V_{RB} .

For this input condition the output becomes according to (1):

$$H = 63 \frac{V_Y}{V_X + V_Y} \quad (8)$$

We have applied this method to charge division in wire chambers by making a bridge circuit of the chamber sense wire and the voltage reference chain (Fig. 7).

Fig. 7. Bridge circuit measuring charge division in a sense wire with a FADC, giving an output expressed in fractions of the wire length.

The sum of the left and right signal $Q_L + Q_R$ is fed to V_{RT} and also inverted to V_{RB} . The difference signal $Q_L - Q_R$ is connected to the normal input (V_{IN}) of the FADC. The response function is then according to Eq. (1):

$$H = 63 \frac{Q_L}{Q_L + Q_R} \quad (9)$$

where: $V_{IN} = Q_L - Q_R$, $V_{RT} = -V_{RB} = Q_L + Q_R$

The digital output will give the position directly (in 6 bits) along the wire in fractions of the wire length. This accuracy will be maintained for a dynamic range of 0.4 V to 2.4 V, or a factor of six in $Q_L + Q_R$ (see Fig. 2). The 6 bit resolution and dynamic range is fully available for the charge division, and the special bridge mode of using the FADC takes care of total signal amplitude variations of the chamber (due to gain, angle, etc.). The performance of the circuit is thus equal to that of a $8\frac{1}{2}$ bit conventional ADC scheme.

The Flash A/D Converter Complemented by Fast Random Access Memories

The data from a FADC is conveniently stored in random access memories (RAM). The memory address

counter is then advanced at the sampling clock rate, and successive time-shifted digitized samples of the input waveform are stored in consecutive memory locations.

Lately, fast RAMs have become available 14-15 or have been announced 16-17, which allow full exploitation of FADCs. Some have access times of less than 10 nsec and a suitable organization.

We have designed a powerful charge and time digitizer for image retaining drift chambers¹⁸ or classical drift chambers. A functional block diagram is shown in Fig. 8.

Fig. 8. Block diagram of a charge and time digitizer with FADC's, measuring total charge, time and charge division.

It contains a FADC circuit with non-linear response (with $a = 0,92$ and $V_b = 0,16$ V) for particle identification by measuring the total charge (dE/dx). A second FADC is connected in the described bridge mode for charge division to measure a spatial coordinate. The data from the FADCs is continuously clocked at a rate of 31,25 MHz into a fast RAM. A 3 bit interpolator¹⁹ measures the time of the input signal's leading edge (to 4 nsec) within the clock period. This information describing a second coordinate is also stored in memory. The system thus continuously records two dimensional complete multi track information and energy loss over a period of $256 \times 32 \text{ nsec} = 8192 \text{ nsec}$.

Other Applications

The FADC measures instantaneous values of its input signal, sampling it during fractions of a nsec. In most cases however, one wants to measure the charge produced during a short period, as is done by gated integrating ADCs. A typical arrangement as found in high energy physics experiments is shown in Fig. 9. Note that the detector signal has to be delayed (τ) to wait for the decision to open the gate of the ADC. This gate is also the most difficult part in the ADC.

Fig. 9. Classical implementation of an ADC in a high energy physics experiment for processing of photomultiplier signals.

The same processing, but then in real time, can be obtained from the circuit in Fig. 10

Fig. 10. Application of a FADC for processing of photomultiplier signals.

The collection time is set by the duration of the clipping time. The FADC continuously samples the clipped and integrated signal, its output being stored in consecutive memory locations. When a valid event occurs, the memory address counter is stopped. The stored information of interest is found by backward stepping of the memory address counter (ex: $\tau = n \times \text{clock-period}$).

Another domain in which we apply FADC is in trigger processors, where decisions are based on signal amplitudes and fast digitizing is essential.

For some applications it may be necessary to increase the resolution, this can easily be done by stacking FADCs or by feedforward or parallel ripple techniques. The latter at some expense in speed.

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References

1. See for example: F. Sauli, "Principles of operation of multiwire proportional and drift chambers", CERN Report 77-09, or G. Charpak and F. Sauli "Multiwire and drift chambers", N.I.M. 162, p. 405, 1979.
2. A.G.F. Dingwall, "A monolithic expandable 6-bit 15 MHz CMOS/SOS A/D converter", ISSCC Dig. Techn. Papers, Feb. 1979, pp. 126-7.
3. R.J. van der Plassche, E.J. van der Grift, "A 7-bit A/D converter", idem, pp. 132-3.
4. J.G. Peterson, "A monolithic fully parallel 8-bit A/D converter", idem, pp. 128-9.
5. W.K. Bucklen, "Monolithic video A/D converter", Digital Video, Vol. 2, SMPTE, Scarsdale, NY 10583, March 1979.
6. U. Fiedler and D. Seitzer, "A high-speed 8-bit A/D converter based on a gray-code multiple folding circuit", IEEE Journal of Solid-State Circuits, Vol. SC-14, No. 3, June 1979, pp. 547-551.
7. Berthold G. Bosch, "Gigabit Electronics - A Review", Proc. IEEE Vol. 67, No. 3, March 1979, p. 346 (340-379).
8. MC 10317L, "A high speed 7-bit analog-to-digital flash converter", Motorola Semiconductor Product Review, 1979.
9. Advanced Micro Devices AM 6688.
10. H. Schmid, "Electronic analog-digital conversions", Van Nostrand Reinhold Company, p. 296, New York 1970.
11. D. Dumortier, "Digital/analog and analog/digital conversion handbook", Motorola 1979.
12. Bernard M. Gordon, "Linear electronic analog/digital conversion architectures, their origins, parameters, limitations, and applications", IEEE Trans. Circ. Syst., Vol. CAS-23, p.391, July 1978.
13. Electronics, Vol. 51, No. 17, p.33, Aug. 1978. "TRW brings out 6 bit A/D converter for nonbroadcast video".
14. K. Kawarada, M. Suzuki, H. Mukai, K. Toyoda and Y. Kondo, "A fast 7.5 nsec access 1K-bit RAM for cache-memory systems", IEEE J.S.S.G., Vol. SC-13, No. 5, Oct. 1978, pp. 656-663.
15. Fujitsu MB 7071, MB 7072, 256 x 4 ECL RAM.
16. Fairchild 100422, Motorola, National.
17. Ulf Buerker and Hans Glock, ISSCC Dig. Techn. Papers, Feb. 1979, p.102-103, "An ECL 100K compatible 1024 x 4 RAM with 15 nsec access time".
18. C. Rubbia et al, "A 4% solid angle detector for the SPS used as a proton-antiproton collider at a centre of mass energy of 540 GeV, CERN/SPSC/78-06, Jan. 1978.
19. C. Engster, L. van Koningsveld, H. Verweij, to be published.