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THE DRIFT TIME AND CHARGE DIVISION ELECTRONICS SYSTEM
FOR THE AXIAL FIELD SPECTROMETER VERTEX DETECTOR

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ABSTRACT

The electronics system of the AFS vertex detector permits the unambiguous determination of space points by drift time and charge division measurement (bigger than 10.000 electronic channels). Facilities are included for reordering of the raw time and pulse height information for optimized preprocessing and off-line analysis. Programmable processors permit trigger decisions and spatial correlation with calorimeter information.

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1. INTRODUCTION

The Axial Field Spectrometer Vertex Detector has already been described elsewhere [1,2,3,4]. Basically it is a cylindrical drift chamber composed of 82 radial sectors each with 42 drift cells, thus giving a total 3444 signal wires. Left/right ambiguity is removed by staggering the signal wires 0.4 mm left and right of the axis.

2. THE LINEAR CHAIN

Fig. 1 shows a block diagram of the linear electronics.

2.1 The preamplifier

The circuit is based on a design by Radeka and Rehak [5]. Briefly the described circuit is a three transistor current to voltage amplifier constructed around a monolithic array of transistors (RCA CA3127) where gain, noise and rise time have been optimized for charge decision read out on a drift chamber. Initial trials using the standard DIL package proved unsatisfactory from the point of view of rise time due to a too high parasitic capacitance at the active collector. In addition it was clear that the total package size could not be accommodated in the available space on the chamber, so it was decided to miniaturize, and to modify the circuit so as to provide a balanced output signal, thereby minimizing cross-talk between channels and providing a basis for subsequent common mode rejection circuitry. A small number of CA 3127 chips packaged locally in beam lead style packages were obtained and the circuit layout remade for use with chip resistors and capacitors. This arrangement proved satisfactory performance-wise, but too difficult for large scale production. Production circuits were commercially hybridized.

2.2 The time pick-off

This circuit is a discriminator to provide start signals to the time measuring electronics. The inputs spy on the balanced signals coming from the preamplifiers. Signals from the two preamplifiers associated with a sense wire are added and amplified, a balanced amplifier being maintained throughout thus providing good common mode rejection. A simple discriminator follows with a fast recovery and a balanced output. Final circuits were

hybridized two circuits per hybrid. Six hybrids were mounted in a camac style unit with a 6-layer circuit board. Four layers are used to provide a through input to output for the linear signals from the preamplifiers in a completely screened transmission system so that cross talk and pick-up would be minimized. The remaining two layers are used for the digital part of the circuit, the ground planes of the two parts being connected only at the edge connector.

2.3 Shaping amplifier

This is a four stage amplifier. Common mode Rejection with gain adjustment, Integrator (T_c 0.5 μ s) Double clipping with a single delay line (150 ns) and buffer amplifier. Output signal is bipolar ± 4 volts. The circuit is hybridized in two packages. Final mounting is 24 amplifiers per camac style unit. The motherboard of the unit is a four layer circuit, providing fully screened balanced input wiring up to the hybrid so that cross talk is minimized. A test facility allows signals to be injected into all inputs simultaneously.

2.4 The fast OR

This circuit is mounted in the Time Pick-off units. It is a linear amplifier with 12 inputs, one from each digital output of the time pick-off circuit. The resultant pulse amplitude being a measure of the number of simultaneous hits in the 12 associated wires. This information is used to provide pointers to chamber sectors where tracks are present. These sectors are read out and preprocessed.

Performance of the linear chain.

Sensitivity: 2.6 volts peak out of the Shaping amp/pC input at the Pre-amplifier;

Linearity: Worst case deviation from a best fit line = 0.1%

Threshold: Minimum 6×10^4 el

Typical operating conditions 2×10^5 el.

Noise: δ Noise 4×10^3 el.

3. THE DATA ACQUISITION SYSTEM

3.1 General

A block diagram is shown in Fig. 2. The 6888 linear channels are read-out from the chamber in a radial fashion and are connected to the ADCs in this way. Pulse height measurement is made by the Lecroy 2280 ADC system using Peak reading 2281 ADCs. At the pick-off circuit level, the digital time signals are rearranged so as to present a read-out of the chamber wires in azimuth, except 16 wires in 4 groups of 4 wires per sector which remain in radial read out form. Thus there are 2 chains of time measuring electronics. The reasons for reordering the time measuring channels in azimuth are two fold. First, the maximum drift time is not the same in all cells of a sector, so stop signals common to a crate can be organized to cover these differences. Secondly, by not having all the drift times of successive sector wires in one measuring module quantizing errors are minimized. Keeping the 16 selected wires in one measuring module is a convenience for preprocessing to establish valid tracks. Time measurement is made by the CERN DRIFT Time Recorder (DTR) System [6].

3.2 Drift chamber fast OR logic

Signals from the fast OR are discriminated, 4 or more simultaneous hits in a group of 12 wires setting the discriminator. A network of gates determine in which sectors of the drift chamber possible track candidates have passed. This information is available directly or it may be correlated to information coming from the calorimeter. Output information is stable in less than 1 μ s.

3.3 P.C. Ram logic

This logic locates tracks in the planer proportional wire chambers [7]. the information being combined with the fast OR logic output, to provide selective read out pointers to the DTR units which are reading wires in radial fashion.

3.4 The ESOP trigger system [8-12]

Information from fast OR and RAM logic is used in the selective read-out system. It will point to DC sectors which are likely to contain the triggering particle. Only DTRs of those sectors will be enabled for a fast read-out, via a routing unit and a bi-directional interface, into the programmable processor ESOP. Here, a track reconstruction and momentum calculation will be executed. If the momentum exceeds a preset level, typically 3-5 GeV/c, the rest of the data will also be read out of the DTRs and the online computer will be asked to read the full event. Processing time in ESOP for one event is currently in the region of 200 μ s.

3.5 The Reformatter [13]

Acceptable events are fully read into the reformatter from the ADCs, the two chains of DTR and from the buffer of ESOP. The Reformatter is a group of Camac units which reorder the data into blocks associated with each wire i.e. time information plus 2 ADC measurements, thus providing an optimum format for off-line analysis. Data transfer from the reformatter to the PDP 11/60 computer is via camac.

3.6 Read out interconnections

Read out interconnections of ADCs and DTRs are made using Romulus/Remus camac controllers [14,15,16] or units compatible with these systems.

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Fig: 1 -

Fig: 2 -