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Design and characterization of an SEU-robust register in 130nm CMOS for application in HEP ASICs

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ABSTRACT: A new SEU-robust D-flip-flop register structure was designed in 130 nm CMOS for implementation of front-end detector ASICs. The register was tested in a heavy ion beam facility and showed a cross section lower than 10^{-10} cm²/bit in the LET range 1.2–62.0 MeVcm²/mg, representing an improvement of more than 10^3 times over previously studied standard library cells. No errors at all were observed at LETs below 30 MeVcm²/mg.

KEYWORDS: Radiation-hard electronics; Digital electronic circuits; Radiation damage to electronic components; Front-end electronics for detector readout

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1 Introduction

The design of High Energy Physics (HEP) experiments often requires the development of ASICs, which are vulnerable to Single-Event Upsets (SEUs) in their digital storage cells. This work focuses on the development of a SEU-robust register cell compatible with the radiation environment present in the tracker sub-detectors of the experiments based on the Large Hadron Collider (LHC).

Whilst Triple Modular Redundancy (TMR) is a typical solution to the vulnerability of flip-flops in digital logic, its backdraw is a $3\times$ increased power consumption and area requirement. This is contrary to the current trend of power reduction needed with the LHC upgrade, which will require an increase of the number of detector channels by one order of magnitude with respect to the present setup.

The solution proposed in this work is a SEU-robust cell which presents $2\times$ redundancy of the circuitry with respect to a standard D-flip-flop (D-FF), and it is based on the Dual-Interlocked Cell (DICE) scheme. Additional layout techniques are employed to protect the upset-sensitive nodes of the circuit avoiding loss of area.

The register circuit proposed was designed in CMOS 130 nm technology, and prototyped in a chip containing a shift-register of 4096 register cells.

Samples of these prototypes were irradiated in a heavy-ion beam facility in order to assess the register SEU tolerance. Results are presented and compared to a standard library register available in the same technology and previously tested in the same facility.

Irradiation test was conducted at two different orientations of the chip with respect to the beam in order to assess the sensitivity to multiple-node hits (tilted chip and beam transverse/normal

Figure 1. Fully $2\times$ -redundant SEU-robust latch implemented in this work. The latch has 2 inputs, 2 outputs and 2 local clock buffers. A register is made of two cascaded latches (a master and a slave).

to standard cell rows). No significant difference in the behavior of the circuit was found in the two orientations.

Total Ionizing Dose (TID) tests were conducted with an X-ray beam and results are presented.

2 Radiation hardening techniques

This section describes the measures taken during the design in order to protect the circuits from radiation effects. These are divided into techniques to enhance TID tolerance and strategies to increase SEU robustness.

The results published in [1] suggest that our $0.13\ \mu\text{m}$ CMOS commercial technology does not require special transistor layouts for digital logic in order to be TID-tolerant up to 100 Mrad(SiO_2) and above. In addition, the authors of [1] show that the only requirement to achieve high total dose resistance is that all the devices have width bigger than $0.3\ \mu\text{m}$. This condition is respected in the present work.

2.1 The SEU-robust register

The SEU-robust register is made of two identical cascaded latches, the first being the master and the second being the slave. The two latches are a modified version of the DICE, introduced in [2], which is intrinsically insensitive to single-node particle hits.

The SEU-robust latch circuit topology was introduced in our previous work [3]. The schematic is presented in figure 1 and it has 4 critical nodes. These nodes (A,B,C,D) have two stable logic configurations. These are (1,0,1,0) and (0,1,0,1), and any other configuration settles to one of these two states. The circuit topology is such that a charge injection on one of the cell's nodes would affect only one of the two nodes immediately connected to it, preserving the data in all nodes. As soon as the charge collection ceases, the unaffected nodes then propagate the correct logic value in the two nodes affected by the upset, making the cell settle to its original state.

As can be seen in the figure, the gates of the p-channel transistors are connected to the memory node on their left, and the gates of the n-channel transistors are connected to the memory nodes on their right. It follows that a negative charge collection by a memory node affects only the memory

Figure 2. Duplicated combinational logic style: two independent data paths are created for redundancy. Each one of the two data paths ends driving one input of the SEU-robust register. In turn, each one of the two data paths is fed by one of the two redundant outputs of the previous register stage.

node on its right, while a positive charge collection by a memory node affects only the memory node on its left. Since on each stage the logic value is inverted, no upset can propagate for more than one stage in the same direction. For instance a negative charge collection by node B would propagate to the right through the p-channel transistor which can pull-up node C to a high level, but this does not affect node D; conversely, a positive charge collection by node B would propagate to the left through the n-channel transistor which can pull-down node A, but again this does not affect node D.

Nevertheless, the DICE cell is not robust anymore at very high clock frequencies (above ≈ 500 MHz); if the charge collection lasts more than $T/2$, where T is the period, the data stored in the cell is compromised. For high speed applications it is still necessary to turn towards TMR.

The original DICE latch has a single local clock buffer. If the clock buffer is upset, the operation of the entire cell is compromised. This upset mechanism is expected to be pronounced in advanced technologies with small feature sizes due to the tiny capacitance of the circuit nodes. In order to alleviate this upset mechanism, our SEU-robust latch features two independent terminals for the input, output and clock signals, driven by separate signal buffers.

Under normal operating conditions, the two inputs are identical. When a particle hits one of the two input (data or clock) buffers, the transient upset will affect only one of the four memory nodes, which are intrinsically immune to this mode of upset.

2.2 Protection against SETs

In a typical ASIC the combinational part of the logic can be hit by a particle and generate a Single-Event Transient (SET) [4]. If the logic is fast enough to propagate the induced transient pulse, the SET can appear at the input of the latch following it, where it can be sampled, erroneously, as a valid signal. Whether or not the SET is stored in the latch depends on the temporal relationship between its arrival time and duration, and the falling or rising edge of the clock.

A way of protecting the combinational part of the circuitry is redundancy, exploiting the double input and double output of the SEU-robust register. The combinational blocks can be duplicated, like in figure 2, in such a way to have two redundant copies of the logic connected to the two redundant inputs of the flip-flops. This protection technique is also referred to as dual-rail logic.

The two inputs of the register have normally the same value and can differ only because of an SET. When the two inputs of the register are equal the value is stored in the latch, while if the two inputs disagree the (master) latch keeps the value which was stored just before the SET.

Figure 3. Layout view of the SEU-robust register bank. The figure is divided into the areas which affect the corresponding nodes in the network (drain areas). The master latches nodes are MxA , MxB , MxC , MxD , while the slave latches SxA , SxB , SxC , SxD ; where x indicates the two registers in the bank ‘0’ or ‘1’. Clock buffers are indicated with $CKxa$ and $CKxb$, while output buffers with Qxa and Qxb .

The maximum propagation delay of the combinatorial logic block must be calculated taking into account the duration of SETs:

$$t_{prop,max} = T - t_{setup} - t_{SET}, \quad (2.1)$$

where t_{SET} is the expected time duration of an upset (worst case), T is the clock period and t_{setup} is the setup time of the SEU-robust register. If this condition is respected the data is always ready at the input of the register with enough slack to load the correct data into the register before the SET. This timing constraint limits the maximum operating frequency for a duplicated-logic circuit. However, a stronger limit is imposed by the SEU robustness of the register which needs $T/2 \geq t_{SET}$.

In this work, the combinatorial part is limited to the inverters/buffers between each element of the shift-register of the test chip.

2.3 Protection against multiple-node particle hits

As explained above, because of its circuit topology, the latch is intrinsically insensitive to single-node particle hits on its network. Nevertheless, the latch is vulnerable to a particle that hits multiple and correlated nodes, an event also referred to as multiple-node charge collection. It should be noticed that once one of the nodes of the DICE is hit, the other nodes are in a weaker high-impedance state.

Ionizing particles that travel along the circuit deposit most of their energy in the first microns of trajectory in silicon, thus in order to reduce the probability of this mode of failure, a layout topology which increases the distance of the sensitive correlated nodes is employed.

In order to achieve spacing of the nodes with no loss of area, the devices of two registers are interleaved. The cell obtained is therefore a bank of 2 logically independent registers, which are interleaved in layout. Figure 3 depicts the layout of the $2 \times$ SEU-robust register bank. The register bank layout size is $29.2 \times 3.6 \mu\text{m}^2$ therefore a single register occupies a area of $14.6 \times 3.6 \mu\text{m}^2$, giving a storage density of 19 kbit/mm². The area of the SEU-robust D-FF is about $2 \times$ the area of a D-FF cell from a commercial library.

Each one of the 2 registers is composed of two latches (master and slave), for a total of 4 latches which are independent each from the other. Every latch has 4 memory nodes whose mutual distance must be maximized. For instance node S0C in the figure must be far away from S0A, S0B and S0D, which belong to the same latch, but it’s independent from the rest of the circuit. In the

Figure 4. Test chip microphotograph.

Figure 5. Photo of test card into vacuum irradiation chamber during targeting.

presented layout (figure 3) the minimum (weakest) distance between correlated nodes is $4.5 \mu\text{m}$ and it is found between nodes M0A and M0B.

Each input gate in the circuit needs a tie-down diode for fabrication issues of this technology (antenna). This diode could possibly degrade the SEU performance. The presented layout takes into consideration the presence of these diodes in order to avoid multiple-node charge collection.

Maximizing the distance between devices implies longer and denser wiring. In the proposed layout, most of the routing space of the first 3 levels of metal is used. This represents a limitation for the use of the cell in metal stacks with few levels.

The overall penalty of these techniques is that the logic occupies twice the area of non-SEU-protected logic and consumes twice the power. The speed of the FF is also affected due to the longer internal wiring, but this is negligible in practical applications which are anyway limited by the typical duration of the charge-injection. Table 1 summarizes the characteristics of the cell in this work with respect to previous designs [3, 5] and to a commercial library register.

2.4 Test chip

A test chip containing 4096 SEU-robust registers (2048 banks of 2 registers), organized in a shift-register, was fabricated in a CMOS 130 nm technology with 8 metal layers (3 thin, 2 thick, 2 RF). The chip size is $1 \times 1 \text{ mm}^2$, while the core size is approximately $510 \times 470 \mu\text{m}^2$. A picture of the chip is visible in figure 4.

The test chip has a dual clock tree, providing timing to the registers through two clock pads. Having a dual clock tree avoids SEUs due to hits on the clock buffers. Two input pads and two output pads are present for the datapath in order to avoid SETs coming from the I/O pads.

Two test chips were packaged in PGA100 for irradiation in order to get higher statistics, hence 8192 registers were exposed to the beam at once.

3 Heavy-ion irradiation tests

The chips were tested using the high-penetration heavy-ion beam at the Heavy-ion Irradiation Facility (HIF) in Louvain-La-Neuve, Belgium.

Table 1. Comparison among several tested versions of the SEU-robust register and a commercial cell.

		DFFR2006	DFFR2007	DFFR2010	(commercial)
Technology feature size	[μm]	0.25	0.13	0.13	0.13
Cell type		SEU-robust	SEU-robust	SEU-robust	standard
Number of interleaved latches		2	2	4	n.a.
Cell width (1 register)	[μm]	68	14.5	14.6	7.6
Cell height	[μm]	11	3.6	3.6	3.6
Minimum distance between memory nodes	[μm]	10.0	2.4	4.5	n.a.
Number of metal levels used		2	2	3	1
Enclosed layout transistors		yes	no	no	no
Minimum device width	[μm]	3.23	0.30	0.30	0.20
Typical inverter input capacitance	[fF]	25	1	1	1
Core power supply voltage	[V]	2.5	1.2	1.2	1.2
LET threshold	[MeVcm ² /mg]	> 79.6	≈ 4.7	≈ 31.0	< 3.3

3.1 Test procedures

The test setup consisted in a test board placed in the vacuum chamber and connected with a host computer outside the chamber. Figure 5 shows a picture of the irradiation chamber during targeting.

The test board comprises a socket for the Device Under Test (DUT), a Xilinx Spartan-3 FPGA, a USB interface, some glue logic and linear power regulators. The USB interface is provided for the connection with the host computer, which runs a control program. The test board and the software were developed specifically for this application.

The Spartan-3 applies a checkerboard pattern to the shift-register in the DUT, while acquiring its output signals and comparing them with the expected values. All the tests were run at a 30 MHz frequency. Only dynamic tests were performed, therefore the clock input of the DUT was always running during the irradiation.

The SEU cross-sections are derived by dividing the total number of errors observed at each LET by the total fluence of the ion beam. The ions used in the test were $^{22}\text{Ne}^{7+}$ at 235 MeV energy giving an LET of 3.6 MeVcm²/mg, $^{40}\text{Ar}^{12+}$ at 372 MeV giving an LET of 9.95 MeVcm²/mg, and $^{83}\text{Kr}^{25+}$ at 756 MeV giving an LET of 31.0 MeVcm²/mg. All other LET points are obtained by tilting the beam with respect to the chip surface (45° and 60°).

3.2 Test results

The present work's SEU-robust register (DFFR2010) fabricated in CMOS 0.13 μm technology proved to be SEU immune in the tests up to an LET of 31 MeVcm²/mg, since no errors were observed below this LET. Figure 6 illustrates the results of the tests.

The register showed a cross-section of $6.09 \cdot 10^{-11}$ cm²/bit at an LET of 62.0 MeVcm²/mg, representing a more than 2000 $\times$ soft-error rate improvement with respect to a commercial standard cell register available in the same technology [3]. Considering the whole LET range explored, the cross-section of the DFFR2010 is always below $1.13 \cdot 10^{-10}$ cm²/bit (upper bound given with 95% confidence level).

Figure 6. Results of the heavy-ion beam test on the 0.13 μm technology SEU-robust register (DFFR2010) compared to two previously studied cells (DFFR2007 and a commercial standard library D-FF). Error bars represent the upper/lower bound cross section given with 95% confidence level (only for DFFR2010).

Compared to a previously designed register (DFFR2007), presented in [3], the present flip-flop also shows a big improvement (much higher LET threshold, cross-section 150 $\times$ lower). The DFFR2007 suffered from multiple-node charge collection, since the cross-section showed to be strongly dependent on the angle of incidence of the beam. With the new layout stile in DFFR2010 the issue is greatly alleviated. An especially important result is that the LET threshold of DFFR2010 is above the maximum LET of particles in the LHC environment [6].

Tests with tilted beam (at 45° and 60°) at two orthogonal beam orientations with respect to the register layout (along short side, along long side) were performed in order to assess a possible dependence on this parameter but the results show no significant pattern.

4 Total ionizing dose test

A test chip was irradiated in an X-ray beam up to 100 Mrad(SiO_2) in order to measure the variation in leakage current of the core shift-register. The test was conducted keeping the chip powered but not clocked (static). Results are shown in figure 7. A maximum increase of the leakage current of 80 $\times$ with respect to its pre-rad value is visible in the data around 1 Mrad. After reaching this peak, the leakage current settles back to a value close to the pre-rad, with increasing irradiation steps. Annealing for a week at 100°C reduces further the leakage current below the pre-rad value.

These results are consistent with the findings reported in [1]: the trapping of charge in the STI oxide of NMOS transistors competes with the slower process of creation of interfaces states, giving the rebound effect.

A second test chip was irradiated in dynamic mode (clocked, checkerboard pattern data). Functionality and supply current were monitored during beam exposure. The chip was functional throughout all the test.

Figure 7. Core leakage current versus TID obtained by X-ray irradiation on the SEU-robust register (DFFR2010). Chip was irradiated up to 100 Mrad(SiO_2); only the initial part of the irradiation is plotted to emphasize the rebound effect.

5 Conclusions

An SEU-robust D-FF structure designed for implementation of front-end detector ASICs was presented. The register was tested in a heavy ion beam facility and showed a cross section lower than $10^{-10} \text{ cm}^2/\text{bit}$ throughout a wide LET range explored ($1.2\text{--}62.0 \text{ MeVcm}^2/\text{mg}$) and represents an improvement of more than $2000\times$ over previously studied commercial standard library cells. No errors at all were observed at LETs under $30 \text{ MeVcm}^2/\text{mg}$.

TID test results show a limited increase in operating current with irradiation with no change in the functionality.

The LHC environment comprises ionizing particles with LETs up to $17 \text{ MeVcm}^2/\text{mg}$ [6]. Hence, from our irradiation test results it is evident that the DFFR2010 SEU-robust register is suitable to be used in LHC applications.

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