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Front end electronics for silicon strip detectors in 90nm CMOS technology: advantages and challenges

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ABSTRACT: We present a 16 channel front end prototype implemented in 90nm CMOS IBM process and optimized for 5pF input capacitance. The primary motivation for this project is to study the usefulness of the CMOS technologies below 130nm for front end amplifiers optimized for short strip silicon detectors in Super Large Hadron Collider (SLHC) experiments [1]. In the presented design we show critical aspects of the front end stages implemented in the deep submicron technologies. Particular effort has been put into minimization of the power consumed by the front end electronics. The nominal power consumption providing Equivalent Noise Charge (ENC) level below 1000e⁻ for the chip loaded with 5pF input capacitance is around 220μW per channel.

KEYWORDS: Front-end electronics for detector readout; VLSI circuits

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1 Introduction

The delay of the schedule for the Super LHC experiments postpones the design and production of the front end ASICs for the upgraded detectors. It is not obvious if the 130nm CMOS technology currently used in many research upgrade programs will still be a competitive technology for High Energy Physics (HEP) at the moment of Super LHC. It is therefore reasonable to start evaluation of CMOS technologies below 130nm from the point of view of usefulness for front end electronics for future detectors. One of the challenging applications is the development of the front end electronics for silicon trackers, where the important issue is very high occupancy impacting final granularity of the system and number of electronic channels [1]. The primary concern is the minimization of power consumption keeping the rest of the analog parameters like speed, noise and dynamic range as well as radiation tolerance at the required levels.

Although technology scaling offers many advantages related to increased transconductance and higher f_t of the devices, the short channel effects and lower intrinsic gain of the transistor present challenges for the input stages designed for detector capacitances of the order of few pico Farads. In this paper, using a prototype front end implemented in IBM CMOS 90nm process, we identify critical points of such a design and give some solutions to obtain desired performance of the circuit.

2 Architecture of the front end channel

The schematic of a single channel of the front end is presented in figure 1. The preamplifier stage has been optimized for 5pF input capacitance and it is built with NMOS input transistor M1 employed in a regulated cascode structure and loaded with a regulated cascode current source. An extra regulated cascode current source directly supplying the input transistor and built with transistors M5 and M6 enlarges the bandwidth of the input stage. Using this configuration, with the intrinsic gain of the single transistor around 18V/V, we were able to obtain roughly 70dB open loop gain together with 3.5GHz Gain Bandwidth Product (GBP) with a power consumption of 120 μ W.

Exploiting mechanism to optimize these parameters is important not only to maintain a low preamplifier input impedance, but also to improve Power Supply Rejection Ratio (PSRR). At low

Figure 1. Schematic diagram of the preamplifier, shaper and comparator stage.

and medium frequency ranges the simulated input impedance of the presented preamplifier is in the range of 50Ω . For frequencies above 1MHz this starts to degrade reaching 250Ω at 10MHz — still low enough for detector capacitances in the range of 5pF.

The PSRR (complete channel) for low and medium frequencies is around 45dB. This degrades to between 8 and 1dB at 20MHz for capacitive loads at the preamplifier input of 1 and 5pF respectively.

The cascode input stage is buffered with a simple source follower and enclosed with active feedback [2] using transistor Mf1 working in saturation region. The preamplifier stage works in transimpedance mode forming the first stage of the signal processing chain.

The main difficulty in using fully telescopic cascodes in the presented technology with 1.2V supply voltage is setting the proper operating point i.e. putting all transistors into saturation and still leaving some margin for dynamic range of the signal. The use of the weak inversion operation region of the transistors helps this problem (saturation voltage in the range of 125mV) however brings other troubles to the input stage. The transconductance of the transistors working in weak inversion and used in active loads are the same as the transconductance of the input device. Therefore its noise contribution to the equivalent series noise of the preamplifier will be the same as from the input transistor. The problem and the solution are well known from the past when the bipolar transistors were in common use [3]. By introduction of resistors R2 and R4 we effectively degenerate the transconductance of the current sources limiting its noise contribution to a negligible level.

One should stress that in 90nm technology the intrinsic gain of the transistor is so low that a single amplifier stage cannot provide sufficient open loop gain to keep a reasonable PSRR after closing the feedback loop. This problem also concerns source follower buffers which can be considered as unity gain amplifiers with a feedback transfer function equal to 1. In order to optimize the PSRR we have maximized the open loop gain of all stages avoiding use of the source followers working outside feedback loops. Consequently the second stage, which serves for amplification and integration of the signal charge, is built as a cascade of two cascode amplifiers enclosed by resistive and capacitive feedback defining the pulse gain of this stage. Although the DC operating point of this stage is stabilized through the voltage VF applied to the gate of Mf1, the relatively

Figure 2. Response to 3fC signal charge for channel loaded with 5pF input capacitance (persistence mode).

Figure 3. ENC as a function of input capacitance for various bias currents of the input transistor.

high DC gain of this stage (12V/V) together with possible parameter mismatch might create DC output variation in the range of tens of mV. In order to limit the problem of mismatch to the discriminator circuit the next stage is AC coupled. It is a folded cascode circuit performing final voltage amplification and integration. Although its open loop gain is limited by a resistive load, the good PSRR is kept because of its fully differential architecture. The regulated cascode current sources supplying the control current directly to load resistors are used for DC separation of the output signal (discriminator threshold). The DC voltage drop on the load resistors i.e. bias current of the folded cascode also defines the dynamic range of this stage which is approximately 600mV differential and good linearity is kept up to 400mV. The differential pulse gain at the output of this stage is 100mV/fC and the peaking time is around 22ns (input not loaded).

The last stage of the front end channel is the leading edge comparator with swing limiter to speed up the response timing, and hysteresis to limit the noise hit rate during the threshold crossing.

For noise optimization purposes the input transistor can be biased with currents between 80 and 120 μ A. The nominal current consumption of the remaining stages of the front end channel is about 80 μ A.

3 Results from the front end prototype chip

The sixteen channel front end prototype consisting of preamplifiers, shapers and discriminators readout through a digital output multiplexer allowed detailed study of the gain, noise and speed parameters as well as the examination of discriminator matching. In addition we have implemented a test channel permitting direct analog measurements of signals at the output of the preamplifier, shaper and discriminator stages.

Figure 2 shows the response of the analog channel biased with 100 μ A input transistor current and loaded with 5pF input capacitor (signal as seen by the discriminator input) to a 3fC signal charge. The peaking time is around 24ns (as simulated for 5pF input capacitance) and the ENC is around 1000e-. More detailed characterisation of ENC as a function of input transistor bias and detector capacitance can be found in figure 3. The measured value of the ENC for channels not

Figure 4. The amplitude responses of the front end amplifiers (two samples) loaded with various input capacitances.

Figure 5. S-curves collected for 1fC signal. Channel #4 (wider waveform) connected to external 5pF capacitor. DAC code equivalent to 0.2mV.

Figure 6. Distribution of channel gains across one chip. Nominal bias conditions.

Figure 7. Distribution of channel offsets across one chip. Nominal bias conditions.

loaded with any capacitance is, as simulated, around $470e^-$. The measured value of ENC at 5pF is roughly 10% higher than expected, around $1000e^-$, for nominal $100\mu A$ input transistor current bias.

Figure 4 shows the amplitude transfer function of the front end channel loaded with various input capacitances. The pulse gain of the front end channel is, as simulated, around $100mV/fC$ and good linearity is kept up to $4fC$ signal range ($400mV$ as expected). Keeping in mind that the power supply used is 1.2V and practically all of the amplifying stages work in cascode configuration, the obtained dynamic range is very satisfactory.

Figures 5 to 9 show measurement results from the full chain done by scanning the threshold voltage of the comparator for several values of input charges chosen from the linear range of the front end. Obtained turn-on curves (see figure 5) have been fitted with the error function which allowed for further extraction of gain, offset and ENC for each channel of the tested chip. During these measurements the chip was biased with the nominal values (input transistor current set to $100\mu A$).

Figure 8. Distribution of ENC across one chip. Input of channel number 4 connected to external 5pF capacitor. Nominal bias conditions.

Figure 9. Time walk of comparator for channel number 4 connected to external 5pF capacitor. Threshold set to 1fC, nominal bias conditions.

Although the mean values of gain and offset (see figure 6 and 7) are close to expectations (respectively 100mV/fC and 0mV) the observed mismatch of gains and discriminator offsets are roughly four times higher than simulated. The origin of this discrepancy is still not fully understood.

Figure 8 shows the distribution of ENC across one particular chip. The input of channel 4 has been connected to an external 5pF capacitor. Taking into account the spread of the ENC across the chip (figure 8) the values measured for open channels as well as for a channel loaded with 5pF agrees well with measurements made on the analogue test channel (figure 3).

Figure 9 shows the time walk of the comparator connected to a full front end channel loaded with a 5pF external capacitor and biased with nominal values. The threshold of the discriminator was set to 1fC. The time walk measured for signals ranging from 1.2fC to 10fC is about 12.5ns. This is compatible with the measurements of the peaking time made on the analogue test channel (figure 2).

4 Conclusion and prospects for the future

We demonstrate that a 90nm CMOS process can be used for front end designs optimized for short silicon strip detectors at Super LHC. Analog parameters of the front end namely gain, speed and noise are close to simulated values. The power consumed by front end channel loaded with 5pF detector capacitance and ENC below 1000e- is in the range of 220 μ W. This value shows that power and current consumption savings are possible in this technology compared to older processes [4].

Thanks to a higher f_t and the increased GBP of the preamplifier, the PSRR parameter is improved with respect to older processes [4].

Although the mismatch of the comparator offsets and channel gains is higher than expected, these remain at a level correctable by a per-channel trimming DAC. Nevertheless the problem of the mismatch is going to be investigated further. Total dose irradiation tests are planned for the near future.

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