The Erigone Bus Study

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ABSTRACT

A study has been made of some factors determining the performance and cost-effectiveness of microcomputer bus systems implemented in Europa crates. An experimental system has been specified and a number of modules constructed in accordance with the specification, in order to test the validity of some of the ideas proposed. It has been demonstrated that the bus interfacing logic can be simple and inexpensive, while maintaining a high degree of processor independence and also a high degree of transparency in operation. The number of pins required by the bus is minimized by multiplexing address and data. A series termination for the drive of the multiplexed lines permits cross-talk to be reduced to insignificant levels: this technique is recommended for wider application. The experimental bus is proposed as a basis for the construction of simple microcomputer-based instrumentation systems.

A short version of this report was presented to the ESONE Annual General Assembly in Zurich, in September 1981.
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CHAPTER I

AIMS OF THE STUDY

I.1 Introduction of Eurocard standards at CERN

In 1979 studies were initiated at CERN of the possibility of adopting the Europa standard card frame to replace the CERN chassis systems such as CIM 8905 and CIM 25543. It became clear that these studies would have a positive outcome, and that adoption of the new standard was only a matter of time. In view of the likelihood that the Europa mechanics would be employed for a large proportion of the electronic equipment of the LEP project [1] a serious investigation was made of potential microcomputer bus standards compatible with the Europa mechanics.

The application area for control systems is primarily the integration of microprocessor modules into some item of apparatus requiring to be controlled or monitored by an embedded microprocessor. Most modules connected to the bus will be of a specialized nature and will frequently need to be designed specifically for the application. The possibility of making a minicomputer is a very real and important consequence of the work, but it is not the primary objective.

I.2 Survey of existing bus systems

The first stage of the study was to investigate features of existing systems and to try to understand the reasoning behind them. The bus systems seemed to fall into two main categories. By far the largest was a class derived from specific microprocessor circuits. The specifications made no attempt to provide computer-independent features, and normally derived the bus timing from the particular microprocessor first used on the bus. This practice has a very simple explanation. The integrated circuit manufacturer normally designs a compatible range of integrated circuits, including the processor, and these circuits are generally designed to interconnect directly, so as to allow single-board systems to be of minimum cost (Figure 1a). When a larger system, using a bus in a card cage, is required, the modules are readily designed if the same signals are used and appropriate line drivers and receivers added to make the bus operate correctly. It is important to note, in this context, that the same LSI circuits will be used in the modules as were designed for the single-board environment (Figure 1b). The additional logic for the bus interface is generally kept to a minimum complexity, and made as transparent as possible in operation.

A very few bus structures had been designed, either to be computer independent, or at least in anticipation of a future extension of the range of characteristics offered by a single supplier.

If the commercial aspects of standards are considered, it becomes apparent that major manufacturers will rarely consider them to be in their interest [2]. Standards make it difficult for equipment suppliers to lock their clients into a particular range of equipment, and they
encourage competition. By making it possible for users to obtain system components from a variety of suppliers, most of whom have been able to avoid the expense of development of a full range of equipment, such competition will act to reduce profit margins and thereby make future development more difficult to finance.

At the time, the most promising candidates in the class of computer-independent bus systems were the Eurobus, Multi-bus and Q-bus [3]. The Eurobus resulted from a joint development between Ferranti, Ltd., and the Ministry of Defence in the UK. This was aimed at providing a military version of the Argus 700 series of computers, but had been designed with a computer-independent structure. It is implemented on Eurocards, employs a 64-pin connector, and multiplexes address and data lines to achieve this. The Multi-bus, although planned by Intel to meet the requirements of the 8080 series, is readily adaptable to other types of processor. It did not exist on Eurocard, and in fact requires very many bus lines, so that the Eurocard version later developed needed to use both upper and lower connectors of a double Eurocard. The Q-bus, developed by Digital Equipment Corporation for the LSI-II microcomputer series, has remarkably few features specific to the LSI-II and is a highly professional engineering product, showing the experience of the design team since the original Unibus development for the PDP-II. This bus uses multiplexing and could be fitted onto a 64-pin DIN connector quite easily, although specified for a connector with two 36-pin sections.

1.3 The Erigone study

It was decided that engineering studies should continue along two lines. The first was to participate in discussions of potential bus standards at an international level, in the ESONE Simple System Study Group as it was then named. The second was to develop and implement a bus system of the required characteristics, so as to explore some of the technical possibilities, and have some direct experience with which to compare other potential bus standards in the international discussions. It was hoped that this experience could be used, later on, to influence the discussions at the international level. A further aim of the study was to provide a cost-effective local bus standard for use in the LEP project if no acceptable international standard were to emerge in the LEP time scale.

Specific aims of the study were to answer the following questions:

i) Can a versatile microcomputer bus be fitted onto a 64-pin connector, together with power supply and ground lines?

ii) If the data and address lines are multiplexed, how much time would be added to each elementary bus transaction in order to deal with the multiplexing?

iii) How fast can such a bus run, and need it limit the speed of the present generation of microprocessors?

iv) What is the minimum hardware required for connecting the bus to the typical LSI peripheral-control circuit?

v) Would specially designed LSI circuits or uncommitted logic array circuits make the bus interface more economical or easier to handle than the standard circuit elements one would otherwise use?

vi) How much equipment can be fitted onto a double Eurocard of 160 mm x 233 mm dimensions? Is such a card too small, or too large, for modern microcomputer-based systems?

vii) Can a back-plane bus of simple and inexpensive construction give adequate performance in terms of operating speed versus cross-talk and noise sensitivity?

viii) What would a complete 21-station crate look like, and how much equipment can be readily installed and powered? If such a crate were to replace a CAMAC crate in a typical application, how would it compare as regards performance and cost?
The bus system which was developed is described in the following sections. Although the design is firmly based on the concept of avoidance of novel architectural features, some specific aspects of the system are worthy of note. The arbitration scheme allows single or multiprocessor systems to be set up using the same processor modules, and without requiring a separate arbiter station. The arrangements for 8-bit and 16-bit operation are such as to allow easy interfacing of differently structured processors. Finally, the electrical specification for the multiplexed address/data lines combines the best features of tri-state and of open-collector standards, and in this way permits the inherently high bandwidth of the bus lines to be effectively utilized.
CHAPTER II

FEATURES OF THE ERIGONE BUS

II.1 Design principles

The essential features of the bus system developed in order to answer the above questions are outlined in this part of the report. A detailed specification is included as Appendix A to the report.

The most important and original aspect of the design is that original features are almost totally avoided. Any designer will be strongly tempted to incorporate novel and interesting features in a new design. Typical examples in this field are: coded function lines to replace the otherwise numerous control lines in a bus; interrupts directed to specific processors; and elaborate, distributed bus mastership arbitration schemes.

After a close study of the characteristics of many integrated circuits intended to be connected to various microprocessors, it became apparent that novel features of the bus would complicate the design of typical modules.

There is a large measure of agreement regarding the way in which basic reading and writing operations are performed, both for data and for control/status registers. Interrupt systems vary, but frequently rely on an interrupt request bus (of one or several lines) and an acknowledgement mechanism. Many LSI circuits are available which can supply an interrupt vector pattern in the "interrupt acknowledge" operation, and it is common to employ a daisy-chain system of some sort for arbitration of multiple interrupts. Similar considerations apply to circuits intended to exploit direct memory access (DMA) capabilities.

The design of the typical microprocessor also seems to imply an acceptance of certain design principles which were established for minicomputers in the previous decade. Interrupt and DMA systems show marked similarities of approach despite the differences in detail. It is obvious that, if one can select a given microcomputer, the most efficient bus system will merely reflect its characteristics, while on the other hand a bus system with novel features requires additional hardware to support them on the processor module. A further problem of novel features is that they make it difficult to use or adapt software modules supplied for use in "standard" systems. Adaptation, by changing addresses and altering status word formats, can frequently be feasible, but complete revision of the algorithms for control of peripherals is a very much more serious undertaking. Furthermore, it seemed that collection of such novel features into a specially designed LSI circuit would not solve the problem, and might well aggravate it.

The Erigone bus specification is aimed at simplifying the use of LSI circuits available now or in the near future for microcomputer interfacing. It is designed around the "de facto" standards which, although undeclared, seem to represent a general consensus at the present time.
II.2 The crate and bus

The basis for the range of experimental modules which have been constructed is the double-height Europa chassis, taking 21 modules of 20 mm width, each 233 mm x 160 mm. The bus uses the lower connector; the upper connector is available for wiring to external equipment.

As the number of stations on the bus is not a factor affecting the arbitration process, a short bus with, say, 5 or 10 stations, may also be used where appropriate. This feature of the design allows specific implementations so as to make use of the crate-division feature of the Europa chassis, and to house, for example, a mixture of single- and double-height modules in the one chassis.

A double-sided printed-circuit board (PCB) is used, rather than a multilayer board, so as to minimize the cost of the crate. One side of the PCB is used for a ground plane. Most power distribution is included in the PCB but the 0 V and +5 V distribution has been augmented by means of a pair of power bus strips. In order to reduce costs in volume production, it would be possible to use the press-fit assembly technique to install the 64-pin connectors on the bus.

II.3 Data and address multiplex lines

Twenty-four bus lines (M0 to M23) are used to transfer address and data. In the first part of a bus cycle the address is transmitted, and this is followed by the data.

The bus address extends to 24 bits, and is a byte address. In order to ease the problems of mixing processor types, the byte selection is achieved by means of two independently controllable data strobes, LBS for the less significant byte and HBS for the more significant byte. Line M0 is consequently superfluous, in the addressing cycle, as an address bit. It is used to identify a special short-address mode: if M0 is set to a "1" during the address phase, then only lines M1 to M12 inclusive indicate a valid address, conventionally used for addressing peripherals. Processors with special input/output (I/O) function codes will use this feature to perform programmed I/O operations, while those employing memory-mapped I/O will decode an appropriate address field.

The bus data transfers are oriented on 16-bit transactions, employing lines M0 to M15. Byte transactions can be achieved by suppression of either data strobe, but the task of selecting one particular byte from 16 bits is left to the controller initiating the byte transaction.

Systems using parity are recommended to take lines M16 and M17 for parity control of lower and upper bytes.

Lines M16 to M23 could also be used for a 24-bit data cycle, although such a possibility is not part of the bus specification. All memory modules are expected to support byte and word transactions, while peripheral modules (not using DMA) are recommended to employ only the lower byte of data, for simplicity. It should be noted that the bus design permits processors with different byte numbering conventions to be employed in the same crate.

Multiplexing of address and data in this way allows a full 24-bit address to be employed without exceeding the design aim of a 64-pin connector. In fact, the active part of the bus will fit a 50-pin flat cable connector, which is of interest for multicrate bus segments. Multiplexing also minimizes the number of line drivers, thus saving board area and power consumption. Although multiplexing must clearly reduce the bus bandwidth to a certain extent, the practical reduction is slight. In some cases, as when dealing with a dynamic RAM, there is no penalty at all.
II.4 Bus arbitration

Bus mastership is achieved by a request/grant system similar to the CAMAC ACB, using a daisy-chain scheme for the granting of the bus. Arbitration is controlled by the extreme left-hand station. This is the position of the "central processor" in a single processor system. Other processors may request the bus and act in a similar way to DMA devices on the typical minicomputer bus.

Processors used in the left-most position and in other positions may be of identical design as regards the bus control logic. A pin on the bus connector is grounded at all stations except the left-most one. This feature can be used to select the appropriate mode of the arbitration logic in the module.

II.5 Interrupts

A multilevel priority interrupt scheme is employed. Six interrupt request lines are provided. These lines may be connected to one processor or shared between two or more, as required in the system. A daisy-chain acknowledge system is used, and implies that a processor generating an interrupt vector cycle will be to the left of the module which generated the interrupt requests. The interrupt vector cycle is indicated by means of a daisy-chain signal which propagates through each module until it reaches the first one which had set an interrupt request on that level. The level is indicated by means of a signal on lines M18 to M23, corresponding to the six request lines. It is conventional to supply an 8-bit identification code in the interrupt vector cycle, on the lower 8 M lines.

The reasoning behind the adoption of this well-established and hardly original interrupt system is based on the existence of peripheral control integrated circuits which operate in just about this way, and processors which expect interrupt-driven peripherals to respond to just this sort of vector cycle. Although there is no consensus about the precise details of interrupt action in different microprocessors, the essential features are sufficiently similar to permit a very straightforward Ergone interface design in each case.

II.6 Timing

At the start of a cycle, addresses must be presented on the M lines for a minimum period of 90 ns. An address strobe signal, AVE, is set in the address phase and remains set while that address is valid. After the address phase, a data transfer is requested by either HBS or LBS or both. For Write operations the data must be presented before the strobes. The slave device responds to the strobe (or strobes) by setting DACK, signifying that it has either accepted data on a Write cycle or has put data on the lines in a Read cycle. The bus timing specification allows a Read or Write operation to take place in about 260 ns, although implementations using currently available integrated circuits will typically slow down operations by a factor of 1.5 to 3 or more from this figure. A Read-Modify-Write cycle is permitted while AVE is set.

It might seem inconsistent to use synchronous timing for the addresses and to change to asynchronous timing for the data. This is understandable when one considers that the Ergone bus is not intended to be completely independent of the circuit technology in which it is implemented. At present, low-power Schottky logic is in general use, and the TTL interfacing levels on the bus could not be changed to, say, ECL. Gradual development of TTL compatible logic, the introduction of CMOS logic compatible with low-power Schottky, and the wider use of logic arrays, will not have a significant effect on the bus timing. It is therefore possible to impose a strict timing requirement on the recognition of the address and storage of the internal sub-address field. Data transfers must be allowed a certain latitude in response time, so a "hand-shake" is adopted in that case. By avoiding hand-shake operation in the address phase, that phase can be kept very short, and the effect of multiplexing on over-all speed is then
almost negligible.

II.7 Signal standards

The essential choice has to be made between open-collector and tri-state signal standards. In the open-collector system, the bus must be provided with biasing networks which establish the "high" quiescent state. If the signal transmission speed is to be balanced in the two cases of positive and negative edges, a high pull-up current is required, and a driver has typically to sink at least 40 mA to set the line to the "low" state. Twenty-four drivers will have to sink, jointly, 1 A or more. This introduces unfortunate effects such as cross-talk between bus lines, power supply noise, earth-line noise, and excessive crate power requirements. These parasitic effects limit the achievable bus speed, even though the bus lines are terminated in an impedance close to their characteristic impedance, and are thus able to support very high speeds if used singly.

In contrast, tri-state lines, allowed to float when inactive and pulled to high or low levels by active drivers, are able to offer a better match between the bus timing and the inherent propagation delay along the length of the bus. High peak currents may still occur, but they are of short duration and may be reduced by the effect of dispersion in delay of the driver circuits. A major problem with tri-state operation can be that of a faulty element. A fault which develops in one module can cause drive circuits in other modules to overheat and perhaps fail. This drawback is a prime reason for avoiding tri-state in systems where high reliability and short repair times are essential.

A mixed solution has been adopted in Erigone. The 24 multiplexed lines are essentially tri-state and the other lines are open-collector. The tri-state drive circuits are, however, connected to the bus through series matching resistors, nominally 39 Ω. These resistors have a double effect. In normal operation they limit the surge current when a large number of lines is set to a given logic level, and in this way the parasitic effects are almost eliminated. The choice of 39 Ω is a compromise. Computer simulations have indicated that the optimum value for achieving the highest speed and minimal overshoots will be about 33 Ω in a fully loaded crate. A slightly higher value was chosen so as to improve the matching in a partly equipped crate: this gives an over-damped bus in the fully equipped crate.

The second feature is that in case of a fault, in which two drive circuits are in conflict, the dissipation in each driver is limited to a low and tolerable value. The bus voltage in the fault condition clearly indicates the nature of the fault, and could be detected by a diagnostic instrument. In the normal condition the voltage drop induced by the series resistors will only reduce noise margins by a negligible amount.

This series-termination technique permits the inherent bandwidth of the bus lines to be utilized, on account of suppressing the parasitic effects often associated with the simultaneous use of many lines.

The non-multiplexed lines, used for control and timing, are driven by open-collector drivers and are terminated at one point by a resistive divider, fixing the "high" level at about 3.3 V, in the conventional manner.

II.8 Power supplies

A multiple supply is specified, generating 5 V and 12 V rails of positive and negative polarities. Although there is an increasing trend to drive purely digital circuits from single 5 V rails, there are still many circuits which require other voltages and it was considered advisable to make some provision for them.

The prototype crates are fitted with 150 W switching-mode power units with the four outputs as specified: such power units are not expensive.
CHAPTER III
PRACTICAL TESTS

III.1 Modules developed

III.1.1 Q-bus bridge module for LSI-11

The first module to be developed was a driver from the LSI-11 (DEC) Q-bus to the
Erigone bus, whereby the LSI-11 could operate modules in the Erigone test crates.

A standard flat-cable extension unit was installed in the LSI-11 chassis, and this was
plugged into the Eurocard module in the Erigone crate. A simplified protocol was employed,
without multiprocessor capability. The communication possibility was not fully symmetrical, in
that a controller on the Erigone bus could not perform DMA operations in the Q-bus segment.
Interrupts were arranged to allow four of the Erigone request lines to map onto the four lines
of the LSI-11/23.

The module required only 25 integrated circuits to deal with all bus control and data
transfer functions, including the interrupt system, and performed to our total satisfaction. The
differences in concept between the Q-bus and Erigone are not great, so that no serious design
difficulties were encountered. The Erigone bus naturally has to run at the Q-bus speed, which
is appreciably lower than the Erigone limit.

The design exercise was limited in scope, as the intention was merely to provide a facility
for testing the bus concepts and some of the modules. Nevertheless, the module which has
been provided is one which could readily be used in straightforward applications, and the
added complication of multiprocesing bus arbitration could, now that it has been proven on
other processor modules, be applied to a future version.

III.1.2 128 kbyte dynamic ram

This module contains 72 dynamic RAM circuits, each of 16-kbit capacity, so making up a
128 kbyte memory (Figure 2). The Erigone bus features are fully supported. A parity bit is
available for each byte, for use with processors such as the LSI-11 which are equipped to deal
with parity. The address area may be located in any 128 kbyte block by means of an internal
switch setting for the most significant 7 bits. The access time of the integrated circuits used is
below 200 ns, and the typical cycle time on the bus, i.e. the duration of the AVE address
strobe pulse when a fast processor is used, is 700 ns. There are several reasons for the length
of the cycle. At the start, there must be a totally reliable arbitration between access from the
bus and the refresh function, so that the memory cycle does not start before the data strobes
are set. At various stages in the operation, timing margins must be provided with respect to the
limits in the specification. Finally, the Erigone Read cycle is specified such that data is
presented with or before the data strobe, while the MC68000 processor used for the tests has
a very long internal de-skew delay on DACK, before it accepts the data and allows the cycle

to terminate.

Since the RAM module was designed, prices of 64k RAM circuits have fallen more rapidly than we expected, so the next version of the module has been designed to accept either 64k or 256k circuits. It will then have a total capacity in the range 512 to 2048 kbytes.

III.1.3 The MC68000 microcomputer

In order to be able to test operation of the Ergone bus at high data rates, a processor card using the MC68000 has been designed (Figure 3). This is a complete computer in its own right, as it contains a local memory and a peripheral interface. A pair of PROM circuits (typically 2716 or 2732) provides adequate storage for an initialization routine, a small monitor, and other routines such as a communications package using the CERN "INDEX" facilities to communicate with the central computers. A set of 16 dynamic RAM circuits provides local volatile storage of either 16384 or 65536 16-bit words. This storage is not accessible to other devices in the crate. The PROM zone is located at addresses from 0 up, so as to take the restart vector. This zone overlays the RAM area, and data are always written to RAM although initially read from PROM. A programmed command switches the Read process to RAM, and by this means the interrupt vectors may be programmed at will when the system has been correctly initialized and/or boot-strapped.

The peripheral device address zone is decoded as a 4k block for use by the internal devices and also the Ergone peripheral zone. These addresses are restricted to be in supervisor data space, so peripherals will not be directly accessible to a user program. The address decoding may be altered to meet specific requirements.

Prototype versions of the module have been constructed using both the 16k and 64k RAM circuits, and with processor clock frequencies of 6 MHz and 8 MHz. In the latter case the internal RAM is run with 500 ns Read or Write cycles and does not slow down the processor at all. The use of the external RAM via the Ergone bus imposes a significant timing penalty of about 250 ns. This is partly the result of an accumulation of timing margins and partly caused by the long MC68000 internal de-skew delay which causes it to wait after receiving DACK. The control logic is programmable to deal with various combinations of processor and memory speeds, up to a 10 MHz processor clock frequency.

Full multiprocessor arbitration has been implemented in the design, and has been tested in practice. Power consumption of the module is between 5 W and 7 W depending on RAM activity.

III.1.4 The F-100L microcomputer

A processor card has been designed for the Ferranti F-100L 16-bit microprocessor (Figure 4). Provision is made for up to eight 24-pin memory circuits to be installed on the circuit board: these may be either PROM (such as 2716 or 2732) or static RAM circuits, and each pair of circuits can contain either 2048 or 4096 words of memory of either type. The most significant bits of the bus address are taken from a dual-in-line switch, and are therefore not alterable dynamically.

The module does not contain any peripheral drive circuits. Decoding functions and bus control functions are implemented by PROM and PAL circuits, so the total number of integrated circuits on the module is remarkably low. Only 22 integrated circuit packages of 14-pin to 20-pin size are used on the module, in addition to the microprocessor and the eight memory packages.
III.1.5 Dual serial line interface module

This module contains two serial-line communications drivers, and was designed to explore the techniques for interfacing LSI peripheral control circuits to the Ergione bus.

The module (Figure 5) may be considered as split into three functional sections: the bus interface, the LSI circuits, and the line interfaces. The basis for the design is the Zilog Z-80A-SIO circuit, which controls two channels in asynchronous or synchronous mode. This integrated circuit has quite advanced functions incorporated, and is able to support transmission protocols such as HDLC. It does not have an internal baud rate generator, so a Z-80A-CTC quadruple timer circuit is installed alongside the SIO circuit.

These circuits, designed specifically for the bus of the Z-80 microprocessor, are not immediately compatible with the Ergione bus system. For example, the Z-80 interrupt daisy-chain system is unusual in concept. Furthermore, all control signals are specified in relation to a CPU clock signal, and a fully synchronous operation is assumed. A crystal oscillator running at 4.9152 MHz is used as a master timing source, and the LSI circuits are operated at a clock rate of 2.4576 MHz. The address block, in peripheral mode, is selected by means of a dual-in-line switch. A wired plug defines the interrupt level to be employed.

The total number of integrated circuits required to support the Ergione bus interface and to provide the control and timing logic is 16, and the total cost is modest.

For each channel, the installation of a wired plug defines operation of a V.24 interface or a 20 mA current loop. In the case of V.24, each channel may be configured as Data Communications Equipment (DCE) or as Data Terminal Equipment (DTE) by use of the correct plug, and the pin connections at the rear connector are laid out to permit a flat cable to be wired directly to a 25-pin plug or socket. In current loop operation, the plug wiring permits the loop power to be obtained either from the module or from the external circuit, and in the latter case galvanic isolation is provided.

An option for synchronous operation (X.21 bis) is provided for one channel, and this can also be adapted for X.21 operation at high speeds, in which case a 15-pin connector to ISO-4903 mounted on the front panel is employed.

The power consumption of the module is about 2 W.

III.2 Bus performance tests

The bus was constructed as a double-sided PCB with a ground plane covering most of one side. The signals on the bus were monitored during the operation of various test programs and were found to be very close to ideal in nature.

The control signals, with open-collector drivers, had rise times of about 25 ns and fall times of about 15 ns. Very little interference between data lines and control lines was observed, the worst case being a negative pulse of amplitude 200 mV on the AVE line at the end of the cycle. This particular effect occurred at the time of disabling the data drive circuits.

Similar pulses were observed on other control lines, but as their amplitudes were not greater than 200 mV, starting from a level of about 3.2 V, they were of no consequence.

The multiplexed lines themselves were very clean in operation, with no apparent mutual coupling and no significant overshoots.

Figure 6 shows a typical Read cycle, under the control of a CPU type MC68000. A multiplexed line was selected to show the timing of the address and data phases clearly: the address is at "1" for about 125 ns before the start of AVE and for about 100 ns afterwards. The memory cycle starts at the end of the address phase, and the memory access time, of about 200 ns, is clearly shown. The memory produces the DACK pulse about 80 ns after the data, and the MC68000 waits for rather a long time, 330 ns, before clearing AVE.

Figure 7 shows a Write cycle, in this case using a 6 MHz processor, and in this case the M line is changing from "0" in the address phase to "1" as data.
Figure 8 shows a sequence containing a Read-Modify-Write operation. The first cycle is a Clear command to a byte in memory. It is closely followed by a Test and Set operation, in which two data stokes LBS are seen. The M7 line is at "1" in the address phase in both cycles. In the test part M7 remains at "1" while the memory is accessing the data, and then, as a result of the initial Clear operation, falls to "0". After the end of the LBS pulse the M7 tri-state driver is obviously disabled and the voltage on the line is slowly rising. In the "Set" phase of the Test and Set operation, the data line is driven to "1" and the Read line (not shown) cleared.

We may conclude that the timing on the Erigone bus is very conservatively specified, and that the unconventional signal standards for the address and data lines have been very successful in controlling parasitic effects. It would be possible to operate the bus at significantly higher speeds than presently specified, as long as the module designs permitted such higher speeds.

III.3 Multiprocessor operation

Only one processor module has so far been designed to implement the specified bus mastership protocol. This is the module described in Section III.1.3 above, using the MC68000 CPU circuit.

This module, if installed in the left-most station, takes the bus whenever it requires it, unless an access request is generated by another station. The same module, with no design change, can be installed in any position provided that the daisy-chain is established between it and the left-most station. It was possible to implement the complete protocol in two integrated circuits, one being a programmable array logic (PAL) circuit.

There are many different ways of implementing multiprocessor systems in a single crate. Those which rely to any extent on shared memory frequently have private memory on each processor module, either as a cache or a strictly local memory. In this way each processor can operate at full design speed for most of the time, with no significant loss either from the bus timing overhead or the arbitration process. In the solution chosen, the private memory of the MC68000 can be as large as 65536 words. This memory is not directly accessible from the bus, so that the design implies that in a multiprogramming environment it might be necessary to permit each processor to take programs and data directly from a shared module such as a disk store controller. If such action were to be controlled by a small supervisor, programmed in ROM, and using the peripheral mode on the Erigone bus, then the disk sub-system would be protected from corruption by programs running in "user mode".

The Erigone specification does not impose the use of non-accessible local memory, and it would be quite feasible to arrange for such memory to be accessible from the bus. In such a case it would be desirable to employ a memory management system so as to control and restrict access. One could even go so far as to permit access to the local RAM only when the CPU was in the "halt" state.

III.4 Software

No specific software has been developed for the bus operations, as the transparent nature of the bus definition is intended to permit standard operating systems and device driver techniques to be employed. Most software used in the tests was written for the MC68000, and to facilitate development work two items of software were loaded into the EPROM circuits. A small monitor routine is used for diagnostics and also for initialization. A communications package allows connection to the CERN computer centre, or any other suitable host computer, so that software may be prepared, assembled, or compiled on a remote computer and easily loaded into the MC68000. This package permits the user to use one terminal to communicate either via the MC68000 with the remote computer or directly with the local system.
CHAPTER IV

CONCLUSIONS

IV.1 Specific questions answered

At the present stage of the Erigone project we feel that we can propose answers to the questions raised at the start of the study: Section I.3 above.

i) The three processor designs which have been carried out so far, together with studies of requirements for some 8-bit processors, indicate that a 64-pin connector is adequate for supporting a versatile bus structure meeting a wide range of system requirements.

ii) Multiplexing of address and data in a bus based on TTL circuits can be achieved with an address phase lasting about 100 ns, half of which may be used for actions which would need to be performed if there were no multiplexing. The over-all time penalty could be reduced below 50 ns if desired, provided that the noise-avoidance measures described in this report are taken.

iii) It would appear feasible to run such a bus on a Read or Write cycle of much less than 400 ns, but conservative choice of margins coupled with the maintenance of a high degree of processor independence will impose practical limits at about this value of 400 ns.

iv) The bus driver circuits, receiver circuits, and control logic for Erigone modules total 12 to 16 small integrated circuit packages (14 to 20 pins) in a range of practical designs. They occupy about 20% of the area of a 160 mm x 233 mm double Eurocard and cost about SF 15 to 50 (depending on the use of PAL circuits).

v) It is clear that a special integrated circuit would allow space to be saved on the Erigone module. At the present stage of technology, such a circuit would be far more expensive than a discrete logic implementation. Furthermore, it would restrict progress in some ways, as improved technology could not be introduced in easy stages. (One example of this is the line drivers, which take appreciable power supply current even when disabled. It is our intention to use modern CMOS devices in the near future, as they become available and economically priced.) There are no special difficulties in interfacing to a multiplexed bus, but in order to avoid minor pitfalls it is always useful to copy the essential features from a previous design!

vi) A double Eurocard measuring 160 mm x 233 mm will accommodate a minicomputer that is very powerful by present-day standards, and such a card size is adequate for holding a half megabyte of RAM. The card size is really too large for the typical small peripheral controller, and a single Eurocard (100 mm x 160 mm) would be adequate were it not for the problem of fixing the output connector. In view of the progress being made towards ever larger scale integration, and the imminent introduction of the new JEDEC LSI packages, there seems little need to use the 220 mm card depth.
vii) A very simple and cheap back-plane design is adequate for the Erigone bus, and could operate at higher speeds provided that the series termination technique is adopted for the multiplexed lines. Such a backplane may be designed to have bus lines of high characteristic impedance, and thereby a good tolerance of bus loading, which would be much more difficult to achieve with a multi-layer PCB.

viii) It is hard to imagine that the typical user of a small instrumentation system will require a full crate containing 21 double Eurocard modules. The typical user may very well be satisfied with a split crate, as allowed for in the commercial hardware now available, containing 5 to 10 full-scale Erigone-size modules. The rest of the crate might contain specialized electronics (in single Eurocard format), small disk stores, and power supplies. If the replacement of a CAMAC crate is considered, then it could be assumed that one or two processors would be required, in addition to a communications module of some sophistication, and perhaps one memory module. About 16 stations would be available for modules such as multichannel scalers or specialized controllers. The Erigone cycle time would be about half that of a CAMAC cycle, and would approach a practical limit of about 400 ns. Design of "intelligent", i.e. microprocessor based, modules would be very much easier than in CAMAC on account of the asynchronous nature of the cycle, coupled with the clear indication of its start. The cost of a powered crate to the Europa standard is significantly less than for a CAMAC crate. This is partly caused by less critical mechanical tolerances and partly by the competition in a large market. Module costs cannot, for a given surface area, be very different from one system to another in small-scale production.

IV.2 General remarks

The Erigone study has been a great success in two respects. Firstly, a series of modules has been designed and commissioned, with no serious problems and with a significant potential utility. Secondly, and this was the real aim, we are able to compare Erigone with other systems, and to evaluate its strengths and weaknesses.

We consider that it is quite unrealistic to define a complex and high-performance bus system around LSI circuits which implement special features of the bus, as such an approach renders the use of other, widely available, LSI circuits very difficult. It is preferable to adopt a bus design in which the bus interface logic is, as far as possible, transparent in its operation. The Erigone designs establish that a bus interface need not be expensive in either board area or component cost, despite multiplexed operation. In particular, a straightforward design for a peripheral driver is readily implemented, and a simple module can dissipate less than 2 W over-all.

One of the reasons for use of multiplexing in Erigone was to avoid large numbers of signals on the bus, with the attendant complication and the high dissipation of the bus drive circuits. Now that CMOS drivers are becoming available the latter point is losing its relevance, but the simplicity of the bus, together with the relative ease of monitoring and fault-finding with fewer signals, still favours the multiplexed solution.

Further development of Erigone modules is likely to continue for a while at CERN, but unless outside interest in simple systems is such as to encourage wider adoption of the Erigone standard, it can only last a few years, having served its original purpose. Much will depend on the ultimate acceptability of other standards now being developed, such as the IEEE P-896 project or the VME bus (which was announced after the completion of the work described in this report).

We hope that some of the ideas which have been tested in the project can find application elsewhere: an interesting possibility would be to develop a compatible low-cost subset of the FASTBUS [4] system. We consider that the Erigone bus system combines simplicity of
concept with high performance, in both single and multiprocessor implementations, at low cost, and would therefore be able to meet the original requirements of the ESONE Simple System Study Group [5] very well indeed.

Acknowledgements
We are indebted to Rob Parker for the design of the F-100L processor module and for several useful suggestions regarding the bus specification. The software for communication with the CERN computing centre was written by Jean-Yves Hemery. Bernard Amacker and Jean-Claude Freze have constructed much of the prototype equipment used in the project, and have made some useful suggestions.

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Fig. 1a  Single-board microcomputer

Fig. 1b  Bus-organized microcomputer system
Fig. 2  Memory module using dynamic RAM circuits
Fig. 3  Single-board computer using MC68000 processor
Fig. 4  F-100 processor module
Fig. 5  Dual-channel multi-protocol serial line interface module
Fig. 6  Bus waveforms: READ cycle
Fig. 7  Bus waveforms: WRITE cycle
Fig. 8  Bus waveforms: READ-MODIFY-WRITE
APPENDIX A: ERIGONE SPECIFICATION

A.1 Basic features of the system

A.1.1 Mechanical
A crate to CERN Specification FIN/MAG/T/LS/lf No. 385 shall be used. (This specification incorporates elements of DIN 41494 and of publication SC48 D12 of the IEC in order to permit CERN to purchase common Eurocrate parts from multiple sources.) Modules will have 4T width (20.32 mm pitch) and shall be either single or double height. In the latter case, the bus must fit the lower connector.

Indirect 64-pin form B connectors to DIN 41612 are used for the bus connections. In the case of double-height modules the upper connector is not defined in this specification.

A standard crate will have 21 usable stations, but it is permissible to use a shorter dataway in cases where special requirements are to be met. Preferred sizes for short dataways are such as to accommodate 5, 10, or 15 stations.

The bus can be extended over more than one crate and has been laid out to facilitate the use of a 50-wire flat cable for this purpose. Recommendations and restrictions on multicrate operation are not included in the present version of this specification.

A.1.2 Layout and master/slave relationships
The arbitration schemes for interrupts and for DMA cycles use daisy-chaining, with the modules at the left of the crate (seen from the front) having highest priority. In a single processor system this processor will be located at the left and will deal with bus management. In a system with two or more processors, these will normally be grouped to the left of any sources of interrupt.

A.2 Pin allocation

A.2.1 Address/data lines
Twenty-four lines, M0 to M23, are provided for address and data transfers, multiplexed in time. In the address part of a data transfer operation the address of the slave data item is specified on these lines, M1 being the least significant line and M23 the most significant one. Byte operation is implemented by means of two data strobe signals, which select either or both bytes. Thus the M0 line is not significant as an address, and it is used for another purpose. The line M0, if set during the address phase, will specify "peripheral mode", in which only the address lines up to and including M12 are significant.

Data transfers are in principle 16-bit transfers, with an option of byte operation, and use the lines M0 to M15. Lines M16 and M17, in the data transfer phase of a cycle, are available for parity of the two bytes, in those systems equipped for parity checking and with 18-bit memory modules.

Lines M18 to M23 are used to identify interrupt response levels, outside data transfer cycles, as explained in Section A3.3 below.

All these 24 lines are driven by tri-state circuits and are positive logic: logic one is the "high" level.
A.2.2 Data transfer cycle control

Five lines in addition to the address/data lines described above are required in order to control data transfer cycles. All these lines are intended to be driven by open-collector drivers, and are negative logic.

Signal AVE indicating address valid is set by the master when it has set the address on the address lines, and stays set through the complete transaction, which may be Read, Write, or Read-Modify-Write to a particular address. The master waits a certain time, removes the address, places data on the address lines in case of Write, or sets READ in case of Read, and requests the slave to perform its part of the data transfer by setting either or both data strobes HBS and LBS.

The slave responds with DACK when it has either supplied data in Read operations, or accepted data in Write operations. This causes the master to remove the data strobe(s) and to either stop the cycle or proceed with another phase (such as Write after Read).

A.2.2.1 DMA-type controllers

A signal BBSY indicates to all stations that a master is using the bus. When another station wishes to acquire the bus mastership to perform a high-priority operation such as a DMA access, it asserts BREQ and it will pass this to the bus arbitration station. The arbitration station or bus control module, located to the left of the requesting station, will generate a grant signal. This line on the bus is daisy-chained. It arrives at each station as BGIN and may be sent onwards (to the right) as BGOUT.

When a station receives BGIN it then tests its internal logic to see whether it has itself set BREQ. If not, it transmits BGOUT to the next station. If the test is positive then BGOUT is not sent on, and the station waits for the end of a cycle, indicated by release of BBSY by the current master. It can then initiate BBSY, subject to timing rules, and take over bus mastership.

These arbitration lines take up four pins at each station. All these lines are negative-logic.

A.2.2.2 Processors

In a single-processor system the processor grants the bus mastership to other stations in response to BREQ. When BBSY is released by such masters, in the absence of a new BREQ, the processor takes bus mastership and of course withholds BGOUT so that no other stations may be active.

In a multiprocessor system the processor in the extreme left-hand position is regarded as the main processor and has lowest priority in bus access. Other processors are regarded, for bus access, as DMA devices. Physically the two types of processor may be identical, as an indication is available on the bus by means of the signal LMS at pin a12. In most stations this pin is at 0V, but in the left-hand position it is open-circuited. Modules which do not need to act as processors should ground this pin.

A.2.3 Interrupts

Interrupt requests may be made on any of six lines, INT1 to INT6. When a station sets an interrupt request line, the processor which must deal with the interrupt must take the bus mastership and then perform a bus cycle of a special nature. It will set a daisy-chained response line, INTIN arriving at each station and INTOUT being transmitted from each station to the next one. At the same time the appropriate line of M18 to M23 will be set to indicate to all stations which request is being processed.
A.2.4 Global control signals

DCFAIL and ACFAIL are generated by the system power supply and are used to indicate and control power-up/power-down sequences.

RESET is a signal which provokes complete initialization of all equipment connected to the bus.

INHIBIT will cause selected stations to pause in their operation, and is used typically to stop processors while not inhibiting DMA operations, at the discretion of the system designer. Modules which might respond to INHIBIT must be able to ignore it, under control of an internal switch, a bit in an internal register, or both. If a register is used, RESET must cause this bit to set the processor to pause during INHIBIT.

Four lines are used for this group of signals.

A.2.5 Power supply lines and earthing

The signal lines described in sections A2.1 to A2.4 above occupy 46 of the pins of the 64-pin indirect DIN 41612 connector. Eight ground lines are included in the bus so as to control electrical transmission at high speed with minimal signal coupling, and the remaining pins are occupied by power supply rails including 2 pins for 0 V and 2 pins for +5 V. Other power rails are specified for −5 V, +12 V, and −12 V. Two pins are available for special power supplies (not mandatory), such as battery supplies for memory circuits.

A.3 Bus operations

A.3.1 Data transfer operations

A.3.1.1 Read cycle (Figure A 1)

The bus master, wishing to read data from a unit (which we shall call the slave) anywhere on the bus, will present an address on M1 to M23 (see A3.1.4 below for peripheral mode). After a minimum settling time of 60 ns the master will assert AVE to indicate that the address is stable. The master must also assert READ during this phase. After an address hold time of 30 ns the master removes the address and asserts data requests HBS and LBS for the upper and lower bytes, respectively. READ must be established at least 60 ns before HBS or LBS are asserted.

The slave module must store the address at the time of assertion of AVE, and use HBS/LBS together with READ to cause the Read data to be placed on the M lines. There will be an access delay which depends on the characteristics of the slave module. When the data have settled on the M lines, the slave module asserts DACK to signify that the master may take the data. The master uses DACK delayed by an extra anti-skew delay of 30 ns to take the data, and when this has been done the master removes HBS and/or LBS. AVE may be cleared at the same time as HBS/LBS. The slave, seeing the removal of HBS/LBS, removes the data from the M lines and negates DACK. When the master sees that DACK is negated it can proceed with the next operation, by setting up the next address, or it may relinquish bus mastership. The slave must remove data from the bus before clearing DACK. The master cannot re-assert AVE less than 120 ns after having cleared a previous AVE.
A.3.1.2 Write operations (Figure A 2)
Write operations start in the same way as Read operations, for the address phase. When
the master removes the address from the M lines it can immediately place the data on these
lines. The data are given 60 ns to settle, READ is not set, and HBS/LBS strobes are ascered.
The slave, on detecting HBS/LBS with READ=0, accepts the data from the M lines and
generates DACK when it has done so. The master then clears HBS/LBS and removes the
data. The slave clears the DACK line when it has finished its writing operation and is ready
for a new address to be presented.

A.3.1.3 Read-Modify-Write operations (Figure A 3)
It must be noted that separate Read and Write operations, as described above, may be
performed if convenient. In the case of a composite operation the address is only specified
once, at the start of the Read operation.
When the master has accepted the data and cleared HBS/LBS, it maintains AVE asserted
to indicate that a further phase will follow. When the slave has cleared DACK on the
termination of its Read operation, the master may at any time, up to a bus time-out limit of
the order of 10 to 20 μs, place data on the M lines, followed after a delay of at least 60 ns by
a HBS and/or LBS data strobe, with READ=0. READ must be cleared 60 ns before
HBS/LBS, and is preferably cleared immediately after the previous HBS/LBS are cleared. The
operation then continues in exactly the same way as for the Write operation described above.

A.3.1.4 Peripheral mode
When M0 is set to 1 in the address phase it signifies that a special short address field is
used, and that M13 to M23 have to be taken to be all in the 0 state.
Processors in which I/O instructions have special instruction codes and/or bus signals
may generate M0=1 to indicate such operations. Processors using a special zone of memory
will decode this zone to generate M0=1.
Repetitive transfers to the same address are permissible in peripheral mode, by maintaining
AVE asserted and repeating HBS/LBS the required number of times.

A.3.1.5 Parity
Systems in which parity checking is implemented use M16 and M17 to indicate odd parity
of lower and upper bytes of data, during data transfer operations. It is strongly recommended
to arrange for all memory modules to deal with the full 18 bits, not including any further
error-checking or correction facilities built into the memory module. Parity is disabled in
peripheral mode operations.

A.3.1.6 Byte operations
The basic data element on the bus is the 16-bit word, which is split into a high byte
transmitted on lines M8-15 and a low byte transmitted on lines M0-7. The address of a byte is
contained in M1 to M23 in the address phase, combined with the selection of either HBS or
LBS. A processor which is equipped to deal with bytes must specify its internal byte address
A0 to A23 and use A0 to select the byte. Nevertheless, high bytes will always be transmitted
on M8-15 and low bytes on M0-7, and the connections between the processor and the bus
must deal with the required positioning of the data in Read and Write operations. These
remarks apply with equal force to processors designed to deal with 8, 16, or 32 bits internally.
Peripheral drivers operating with 8-bit data only are recommended to use LBS only. The
byte addresses will be odd or even depending on the type of processor handling the
transaction.
A.3.1.7 Multiple cycles

It should be noted that the bus mastership and BBSY line are not directly involved in the individual data-transfer cycles. Consequently a master may hold on to the bus for many cycles, without requiring a new arbitration. Good practice in system implementation will limit the number of bus cycles which a master will perform, after BREQ has been asserted (by another station), to a small number, typically the size of a multiword data element.

A.3.2 Arbitration process

A.3.2.1 DMA operations (Figure A 4)

A station needing to acquire bus mastership with priority, e.g. for a DMA-type operation, will assert the bus line BREQ. If another station is already established as a bus master at this time, it will indicate this by assertion of BBSY and/or AVE.

Arbitration is performed by a module to the left of any station which might generate a request. This station may be a special unit dealing with arbitration and other systems functions, or it may be a processor requiring bus mastership itself from time to time. The arbitration module waits until BBSY is cleared and replies to BREQ by asserting a bus grant signal BGOUT. BGOUT must be delayed 100 ns or more from the time BBSY is cleared. BGOUT is connected to the next station as BGIN.

Stations receiving BGIN must pass the signal on as BGOUT, unless they themselves have asserted BREQ, in which case they should withhold BGOUT and so stop the propagation of the grant signal along the bus. Arbitration occurs in each successive station when it receives BGIN. A decision is taken at that time, and a station must either proceed to become bus master or renounce such action until the next arbitration cycle occurs.

Each potential bus master station not requiring the bus will pass on BGOUT after a certain time delay from reception of BGIN. This time delay must be sufficient to reduce arbitration errors to a negligible rate, and 30 to 40 ns is recommended in cases where the internal decision is made by a flip-flop of the 74S series.

In order to save time in arbitration, it is recommended that a bus master should clear BBSY during the last cycle, well before AVE is cleared. No new master may place its address on the M lines until AVE has been cleared from the previous cycle, and it may not assert AVE until DACK has been cleared.

A.3.2.2 Processor arbitration

A single processor, in the left-hand position, will control DMA arbitration by means of its generation of BGOUT in response to BREQ. If no stations are generating BREQ the processor may take bus mastership for itself, asserting BBSY and obeying the standard rules for transactions.

Other processors in the crate will request bus cycles, as needed, in the manner of a DMA request, as explained in the preceding section. In order to avoid overloading the bus in a multiprocessor configuration, each processor module should have adequate internal memory for local operations independent of the bus. If necessary, such memory could be arranged as a cache.

The left-most station could be occupied by a simple arbitration module if that were desired, rather than by a processor.
A.3.3 Interrupts (Figure A.5)

Interrupt requests may be made on any of six lines, INT1 to INT6. In a single-processor situation, these lines might correspond to different priority levels. In a multiprocessor situation the lines might be assigned to two or more processors, either permanently or dynamically. When a station sets an interrupt request line, the processor which must deal with the interrupt must take the bus mastership and then perform a bus cycle of a special nature. It will set a daisy-chained response line, INTIN arriving at each station and INTOUT transmitted from each station to the next one.

At the same time the appropriate line of M18 to M23 will be set to indicate to all stations which request is being processed. After a delay, strobes HBS and LBS are asserted by the processor dealing with the interrupt. Each station receiving INTIN must check whether it has itself originated a request on the particular INT1 to INT6 request line; if not, it must pass on INTOUT. Otherwise, it will respond to HBS/LBS by placing an interrupt identification code (or vector) on the 16 less significant multiplexed lines M0 to M15. At the same time DACK is asserted. The timing is similar to that for a bus Read cycle, in which AVE is replaced by M18 to M23, and the access time is dependent on the INTIN/INTOUT daisy-chain delays. INTOUT must be delayed from INTIN in a similar way to the bus grant BGIN/BGOUT delays: minimum 30 ns.

A.3.4 Reset and inhibit

Any station may assert RESET at any time, and the effect will be to cause all equipment to initialize in accordance with the rules for the specific system. All bus requests, interrupt requests, and handshake signals will be cleared, and the bus will not be driven in any way apart from the RESET line itself. The duration of the RESET signal must be greater than 25 μs.

The RESET signal will normally be generated by the processor in single-processor situations.

The use of the INHIBIT line is at the discretion of the system designer in most respects. INHIBIT must be able to stop the action of background processors unless disabled by an internal control register or switch. It is recommended that INHIBIT be arranged to prevent any station from acting as a bus master.

The INHIBIT signal may be asserted at any time for a minimum duration of 1 μs. Devices subject to INHIBIT may complete the current bus cycle before taking the defined action, up to a time limit of 25 μs.

A.3.5 Power supply sequencing

When power is first applied to the system, the two signals ACFAIL and DCFAIL must be asserted (held at the low logic level) by the power supply sequencing logic. When the d.c. power lines have been stable for at least 1 ms, DCFAIL is cleared; and when DCFAIL has been cleared for at least 100 ms, and the mains input is such as to assure a reserve of at least 10 ms of d.c. power, ACFAIL is cleared. RESET must be asserted before DCFAIL is cleared, and must stay asserted until at least 10 μs after ACFAIL is cleared.

Stations on the bus must take no action until ACFAIL is removed.

When a mains power failure occurs, the power supply unit will assert ACFAIL to indicate that only 20 ms of power is available in the power supply energy storage. This time may be extended at the discretion of the system designer if a very long power-down sequence is desired, and if adequate energy storage is provided in the power unit. Processors will detect ACFAIL and initiate the appropriate sequence so as to shut down safely. This sequence must be completed before DCFAIL is asserted. DCFAIL is asserted by the power unit at least 12 ms after ACFAIL and at least 2 ms before the d.c. power supplies have fallen outside
specification limits. DMA operations cease when DCFAIL is asserted, unless previously stopped by the power-down sequence or by a RESET pulse.

A.3.6 Bus errors

In any transaction on the bus a fault may occur, and a mechanism must be available for detecting and perhaps recovering from such faults.

For data transfer operations, a slave module must respond to HBS/LBS strobes by means of DACK. If DACK is not generated within a time limit after the start of the strobe, the bus master may assume that a fault has occurred and abort the cycle by removing HBS, LBS, and AVE.

In the bus arbitration mechanism, when a processor or bus control unit responds to BREQ by asserting BGOUT it will expect to see a new master assert BBSY within a short time after completion of the previous bus operation (AVE and DACK cleared). It is recommended to apply a time-out rule to this situation wherever possible.

The same rules apply with respect to interrupt response. After an interrupt arbitration, DACK is expected at the bus master within a time-out period. The time-out period may be chosen by the system designer, and indeed may be imposed by a component supplier. It is recommended that the time-out interval be in the range 5 to 25 μs.

Arrangements for monitoring the operation of the bus in other respects, by means of a special module which detects blockage or violation of rules, are not defined at this stage. It is strongly recommended that a standard test unit be installed in the crate, and that facilities in this module permit the data transfer, interrupt, and arbitration mechanisms to be verified.

A.4 Electrical signal standards

A.4.1 Multiplexed signal lines

The data/address lines M0 to M23 are tri-state lines with no termination components on the bus backplane. Each driver/receiver assembly on the individual plug-in modules must be connected to the bus through a series 39 Ω resistor (10% tolerance) for each M line.

Logic states for the M lines are positive. The logic "1" is represented by a level in the range +2.4 to +5.0 V, while logic "0" is represented by a level in the range 0 to +0.8 V.

Driver circuits must be able to sink at least 20 mA at 0.4 V in the "0" state, and provide at least 10 mA at +2.4 V in the "1" state. No station must load the bus with more than 200 μA in the "0" state or with more than 50 μA in the "1" state.

The series 39 Ω resistors will alter the "0" level on the bus by 0.16 V if 20 stations are being driven, each with a leakage current of 200 μA. A multicrate bus with 60 stations would be at the limit of the specification, as the 0.4 V at the driver circuit would be transformed to 0.8 V on the bus line. In a later edition of this specification the leakage current limit may be lowered, and this would imply the use of CMOS or similar circuit technology.

A.4.2 Other bus lines

Apart from the M lines specified in the preceding section, all signals on lines connecting all stations in parallel in the crate are negative logic, with open-collector drivers. The bus in the crate is terminated at one end with a resistor network, fixing the "0" level at +3 to +4 V, and requiring that a driver sink 18 to 24 mA in the "1" state at +0.4 V. A suitable termination for each line will be made up of a 470 Ω resistor to 0 V and a 220 Ω resistor to +5 V.

Drivers must be able to sink 24 mA at +0.5 V. The drivers must not have more than 50 μA leakage current in the "0" state at bus voltages in the range +2 to +5 V.

Line receivers at each station must not draw more than 50 μA from the bus in any circumstances.
Assuming a maximum of 21 stations, each with drivers and receivers, the load caused by leakage current in the "0" state may reach \(21 \times 2 \times 50 \mu A = 2.1\) mA, while the sink current required of the driver may reach 23 mA at +0.5 V.

The LMS pin should be connected to ground in modules which will never act as bus arbiter in the left-most station.

A.4.3 Daisy-chain signals

The resistive termination networks for BGIN and INTIN have to be installed in the modules rather than on the bus backplane. In each station acting on interrupt or bus grant signals, the BGIN and INTIN signals must be biased to the "0" state by means of a 1000 \(\Omega\) resistor to +5 V. The BGOUT and INTOUT signals must be generated by totem-pole driver circuits with at least 8 mA current sink capability, or by open-collector driver circuits. In the latter case there must be a pull-up resistor of not more than 500 \(\Omega\) to +5 V at each output.

At any station which has no need of either bus mastership or interrupt facilities, BGIN will be linked to BGOUT and INTIN linked to INTOUT so as to maintain the integrity of the chain. In this case no termination resistors will be required.

A.4.4 Bus wiring

The bus wiring should be arranged so that the characteristic impedance of the signal lines is in the range 100 to 150 \(\Omega\), neglecting capacitive loading effects which will reduce this impedance.

Bus wiring must be able to withstand signal currents up to 500 mA on each signal line.

A.4.5 Power supply lines

The total power dissipated in any one station in the crate is limited to 10 W. Individual supplies are limited to 2 A for the +5 V line and 1 A for all other power rails.

The recommended minimum power supply for a complete 21-station crate will deliver 20 A at +5 V, 2 A at +12 V, 2 A at −12 V and 2 A at −5 V. This gives a total power consumption of 158 W, averaging 7.5 W per station.
### A.5 Pin allocation chart

<table>
<thead>
<tr>
<th>Signal</th>
<th>a</th>
<th>b</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ground</td>
<td>1</td>
<td>1</td>
<td>Ground</td>
</tr>
<tr>
<td>BGIN</td>
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<td>2</td>
<td>INTIN</td>
</tr>
<tr>
<td>BGOUT</td>
<td>3</td>
<td>3</td>
<td>INTOUT</td>
</tr>
<tr>
<td>INT6</td>
<td>4</td>
<td>4</td>
<td>INT5</td>
</tr>
<tr>
<td>INT4</td>
<td>5</td>
<td>5</td>
<td>INT3</td>
</tr>
<tr>
<td>INT2</td>
<td>6</td>
<td>6</td>
<td>INT1</td>
</tr>
<tr>
<td>Ground</td>
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<td>7</td>
<td>AVE</td>
</tr>
<tr>
<td>Ground</td>
<td>8</td>
<td>8</td>
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<td>M15</td>
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<tr>
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<td>+5 V</td>
</tr>
<tr>
<td>0 V</td>
<td>32</td>
<td>32</td>
<td>0 V</td>
</tr>
</tbody>
</table>

Connect corresponding pins at all stations, except for BGIN/BGOUT and INTIN/INTOUT which are daisy-chain connections, and LMS which is Ground at all stations except the left-most, where it is to be open-circuit. BGOUT is wired to BGIN of the adjacent station to the right, INTOUT to INTIN of that adjacent station. Common return of power unit wired to pins a32 and b32, linked to Ground pins on the bus backplane.
Fig. A 1  Read cycle

Fig. A 2  Write cycle
Fig. A.5  Bus arbitration timing.