An Early Slice Prototype for the Upgraded Readout Electronics of TileCal

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Requirements / Components

As a possible solution for future readout and trigger electronics the slice prototype has to provide a general structure for communication and data readout between on- and off-detector electronics.

General requirements:

- Global clock distribution from off-detector to on-detector side using FPGAs
- Data transmission using FPGA built in gigabit transceivers (GTX) and the GBT-protocol
- User interface for programming, monitoring and debugging
- High throughput data readout

Schematic of the test slice structure

For usage within TileCal this was extended and the following components were used

- PCIe Gen2 evaluation platform from HiTech Global equipped with a Virtex6 LX240T (off-detector electronic emulation)
- ML605 evaluation platform from XILINX equipped with a Virtex6 LX240T (on-detector electronic emulation)
- Prototype MainBoard for the TileCal readout including the following main components
 - 4 x ADC – 12 bit (LTC2264-12)
 - 2 x ADC – 14 bit (LTC2264-14)
 - 2 x DAC – 12 bit (LTC2634-12)
 - 1 x Clock distributor (LMK01010)

Introduction

Upgrade plans for ATLAS hadronic calorimeter (TileCal) include full digital readout of all data to the counting room. This concept uses modern FPGAs containing large amounts of logic resources, generous connectivity and built-in multi-gigabit serial transceivers for communication. We have developed a slice prototype of the full readout chain based on prototype modules and off-the-shelf components. As different module prototypes are developed and become available they can be exchanged with earlier prototypes or emulators in the chain. Due to its modular and flexible structure, the prototype can be modified to reflect changing requirements. It will also allow most of the final functionality to be developed and tested before the hardware design is finalized.

The present application logic structure

Data acquisition unit:

- Serializes the data stream from every ADC with 480 Mb/s and send it to the GBT-tx logic to be transmitted with 4.8 Gb/s to the off-detector electronics

SDI program unit:

- Full automatic program unit for SDI and μ Wire interfaces.
- Adaptable using a programmable BRAM accessible via the control unit

Control unit:

- State machine that receives data /commands from the GBT interface and sends it to the corresponding logic part.
- Also used to transmit the status of the System back to the off-detector side

Clock manager:

- Clocking unit that allows to perform frequency synthesis as well as phase shifting of dedicated clock signals

Pipeline – derandomizer memory:

- Receives the raw data stream and stores it until a Level 1 accept is received
- Programmable with TTC commands via a compatible interface

Test slice controller:

- Controls the whole test slice
- Accessible via PCIe and a user program running on the host PC and TTC commands

TTC:

- FPGA implementation of the TTC decoder (so far only Level 1 accept and broadcast signals implemented)

PCIe BMD unit:

- Logic implementation of a PCI express Gen2 Bus Master Design (BMD) using Direct Memory Access (DMA) to transmit data between the Host PC and the evaluation Board
- No embedded system is needed

The prototype hardware

Current firmware test platform

Next firmware test platform

- 1 XILINX ML605 evaluation platform:
 - Off the shelf FPGA evaluation platform used during development of the test slice firmware
- 2 3in1 Front End electronics:
 - Developed at the University of Chicago
 - Used to generate analog test pulses using a built in calibration mode
- 3 Prototype MainBoard:
 - Custom data acquisition board developed at Stockholm University to Sample incoming analog pulses and transfer them to a processing FPGA board
 - Compatible with off the shelf evaluation platforms through an FMC-HPC connector
- 4 Prototype DaughterBoard:
 - Custom evaluation platform developed at Stockholm University to evaluate special requirements for redundancy
 - At the moment in debugging phase
 - The final platform on which the test slice firmware should be implemented

Results / Conclusion

The complete data path outlined was successfully implemented and tested including:

- Clock distribution and recovery
- SDI programming of peripheral components (ADCs, DACs, ...)
- Test pulse creation, sampling and transmission to the off-detector evaluation platform
- Data storage in pipeline and derandomizer memory including reception of Level 1 accept
- Control and readout using user software running on the host PC housing the off-detector evaluation platform

Test pulse stored on host PC

- Possible to use the recovered clock for testing the high speed data transmission of one GTX
- Test slice firmware was proven to be easily scalable and adaptable to new environments
- Test slice firmware will be moved from ML605 to DaughterBoard after hardware debugging

40 MHz recovered clock signal (on-detector)

- When bit error tests are performed using the DaughterBoard we expect acceptable bit error rates (ML605 does not support SFP+)