An Upgraded Front-End Switching Power Supply Design for the ATLAS TileCAL Detector of the LHC

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Abstract—We present the design of an upgraded switching power supply brick for the front-end electronics of the ATLAS hadron tile calorimeter (TileCAL) at the LHC. The new design features significant improvement in noise, improved fault detection, and generally a more robust design, while retaining the compact size, water-cooling, output control, and monitoring features in this 300 KHz design. We discuss the improvements to the design, and the radiation testing that we have done to qualify the design. We also present our plans for the production of 2400 new bricks for installation on the detector in 2013.

I. INTRODUCTION

THE Tile Calorimeter (TileCal) of ATLAS is designed to measure the energy, time of arrival, and energy of secondary particles that are produced in the detector from proton-proton collisions at the CERN Large Hadron Collider (LHC) [1-2]. The calorimeter is composed of alternating layers of steel absorber and scintillating tiles as the active media. Light produced in the scintillators is routed to photo-multiplier tubes (PMTs) using wavelength-shifting (WLS) fibers. The photo-detector (PMT) used in the calorimeter is a Hamamatsu 7877. It is a single anode tube with 8 dynodes. The PMTs reside in a part of the detector called “drawers,” which also contain the front-end electronics, digitizers, and read-out electronics. In general, the front-end electronics that reads out the PMTs are located very close to the PMTs. Generally, there are ~45 PMTs in each drawer, although the number varies depending on location. The Tile Calorimeter is designed as two long barrels and two extended barrel sections. Each barrel section is built of 64 independent wedges along the azimuthal direction, constructed as a mechanical unit. This results in 256 wedges in total. The barrel covers the region $-1.0 < \eta < 1.0$, and the extended barrels cover the region $0.8 < |\eta| < 1.7$. A picture of a drawer is shown in Fig. 1.

Fig. 1. View of a TileCal Drawer, fully extended for servicing.

The drawer electronics are powered by full-custom switching power supplies, called the Finger Low Voltage Power Supply (fLVPS or just LVPS) [3]. Each power supply provides power to one module, and resides on the outside of the drawer in a special metallic shielding called a “finger,” as shown in Fig. 2. Each supply is a package that consists of eight power modules or “bricks,” providing a range of currents and voltages as needed for each detector wedge. There are three types of circuitry in each wedge: mother board (MB), high voltage generation (HV), and a digitizer board (DIG), hence the need for different voltages and currents. A summary of the different voltages and currents is shown in Table I. (Note that individual drawers vary slightly.) The different bricks all use the same topology and basic design, including the same printed circuit board design, but each type is configured specially for the particular load that it services. A picture of a full power supply unit is shown in Fig. 3 (the cover is removed.) An end view of the box is shown in Fig. 4. A picture of an individual brick – our prototype drop-in replacement design – is shown in Fig. 5. There is a cold plate that runs laterally through the middle of the box that is water-cooled, and provides the thermal cooling for the box, as shown in Fig. 4. The bricks attach to the top and bottom of the cold plate, 4 per side. The high-power components of the brick, including the transformer, have thermal connections to the cold plate. The LVPS also has an interface board called the ELMB-MB. This board contains an ELMB chip which has analog-to-digital converters (ADCs), digital-to-analog converters (DACs), other digital I/O, and an interface to CAN-BUS, which is the slow-controls system for the

Manuscript received November 11, 2011. This work was supported in part by the U.S. Department of Commerce under Grant No. BS123456 (sponsor acknowledgment goes here).

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calorimeter. The ELMB-MB is the board on the bottom side of Fig. 4, where the yellow cables attach.

Fig. 2. View of a TileCal Finger Low Voltage Power Supply, mounted onto the end of the Drawer.

TYPE	Nominal Voltage	Nominal Current
DIG+3	3.45V	4.74A
DIG+5	5.3V	5.6A
MB-5	-5.3V	5.6A
MB+5	+5.4V	11.1A
MB+15	+14.5V	0.45A
HV-15	-14.5V	0.3A
HV+5	+5.0V	0.18A
HV+15	+14.5V	0.29A

TABLE I. SUMMARY OF VOLTAGES AND CURRENTS FOR EACH BRICK TYPE

Fig. 3. View of a LVPS box with cover removed.
Photo courtesy of Ivan Hruska.

Fig. 4. End view of a LVPS box with cover removed. The cooling plate can be seen through the center, with bricks mounted to it top and bottom.
Photo courtesy of Ivan Hruska.

Fig. 5. View of an individual brick.

There are several aspects of this project that are significant. Since the supplies reside on the detector, they must be capable of operation in a magnetic field. Because of this, it is not possible to use linear supplies for this application since the transformer cores would saturate. The use of switching supplies for analog front-end electronics that processes low-level signals poses a challenge to keep the conducted and radiated noise low. The bricks switch at 300 KHz, and produce harmonics through the entire spectral range of interest in the front-end electronics. Because the supplies reside on the detector itself, they will be exposed to radiation, including gamma radiation, protons, and neutrons. The compact size of the box and the fact that it is closed represents a challenge in cooling. The use of the cold plate, along with judiciously-placed thermal contacts between the bricks and the plate addresses this. Lastly, access to the detector is very difficult; there may be only one opportunity per year to perform maintenance and repair operations on the detector. This means that we require very high reliability for the overall design.

Fig. 6. Block diagram of the LVPS brick.

II. MOTIVATION FOR THE REDESIGN PROJECT

The current power supply bricks for the detector, V6.5.4, were produced and installed in 2007, and have been operating on the detector since then. Generally, the supplies have functioned well, meeting the challenging requirements needed to function in this environment. However, in the last year the system has shown sensitivity for trips at a rate that scales with the luminosity of the beam. A plot of the observed trips versus luminosity is shown of Fig. 7. In these cases, an individual LVPS box trips off, but is restarted after a period of ~ 2 minutes. Most often the recovery is automatic through software control, but sometimes the recovery requires human intervention. These trips are usually not debilitating, but do cause a loss of data from that particular module for several minutes. Since the luminosity of the LHC will continue to increase in time, it is desirable to address this problem in the near term. Also, a great deal has been learned about the low-voltage power system and the performance of the bricks, and we will take this opportunity to implement other improvements to the design. For these reasons, we have designed a new version of the brick, V7, which will be described.

Fig. 7. LVPS Trips versus Luminosity

III. OVERVIEW OF THE DESIGN

The basic topology of the brick is a transformer-coupled buck converter. Each brick receives 200VDC at low current, and converts it using switching techniques to low voltage at moderate currents. The requirements for the different types of bricks are shown in Table I. A block diagram of the circuit is shown in Fig. 6.

The basic components of the design are as follows: The heart of the design is the LT1681 controller chip [4]. It is a pulse width modulator (PWM) that operates at a fundamental frequency of 300 KHz. The output duty factor can vary from a few percent up to a maximum of 45%. The pulse width is controlled by two inputs: the “slow” feedback path, which monitors the feedback voltage with a bandwidth of ~ 1 KHz; and a “fast” feedback path which monitors the current through the low-side transistor on the primary side. Both must be designed properly to ensure continuous-mode operation at the nominal voltages and currents for each brick type.

The LT1681 provides an output clock to the FET Drivers, IR2110 [5]. These are transistor drivers that have sufficient current and voltage drive to drive the high-side and low-side power Field Effect Transistors (FETs) that perform the switching on the primary side. The design uses synchronous switching, i.e. both the high-side and low-side transistors turn on and conduct for the duration that the output clock is in the high state, and both are in the off state when the clock is low. When the FETs conduct, current flows through the primary windings of the transformer, which transfers energy to the secondary windings. The transformer is a custom planar design, with turns-ratios of 14:1 and 14:3 for the 5V and 15V transformers respectively.

The buck converter is implemented on the secondary side of the transformer. The output side also contains an additional LC stage for noise filtering. Voltage feedback for controlling the output voltage is provided by the Avago opto-isolators HCPL-7800 [6]. The design also incorporates a shunt resistor for measuring the output current, the voltage for which is also fed back using an opto-isolator. Note the relatively simple

circuitry on the secondary side, one of the changes in the redesign project to improve reliability. The secondary side is completely floating with respect to the primary side, to facilitate grounding isolation of the front-end electronics with respect to the primary side of the power distribution system.

The value of the output voltage is controlled by a reference voltage that comes from the central controller in the LVPS box, the ELMB. The feedback circuit uses LM6142 operational amplifiers [7].

The brick has three types of protection circuitry built in as part of the design. There is over-voltage protection (OVP) and over-current protection (OCP). Both of these circuits are on the primary side, and both are configured for each particular type of bricks. Generally, the OVP circuits are set at 10-20% above nominal voltage, while the OCP circuits are set at 25-50% above nominal current. The controller has a “soft-start” feature that limits the in-rush current for cold-starts. The brick design also incorporates over-temperature protection, which monitors the temperature of the primary side switching transistors.

Lastly, the brick has monitor circuits. These send facsimile analog voltages to the ELMB that represent the input and output voltage, the input and output current, and readings from two temperatures located on the brick.

IV. NEXT-GENERATION DESIGN IMPROVEMENTS

Having the benefit of working with a large operating system, a critical study was carried out to determine how the design might be improved. We also provided repair and technical support for the early running period of the bricks, 2007 – 2009, and have the repair records and experiences from that effort. These were used to formulate specifications and goals for the redesign project. Some of these improvements are described below.

A. Noise Improvements

As mentioned earlier, one of the motivations for this project is the spontaneous tripping that is occurring in the detector as a function of luminosity. A study of average trip rates as a function of luminosity measured from January – September, 2011, as shown in Fig. 7. Although this was not known when the redesign activity began in 2009, it became the primary reason for the redesign.

It was observed early in the performance study that the noise of the current bricks was quite large, of order 0.9 volt peak-to-peak, as shown in Figure 8a. It was also observed that the magnitude of the noise was a function of load, which is a general feature of switching power supplies. Note that these noise peaks are very sharp, with high dV/dt values. Because the OVP and OCP circuits generally had to process voltages with this noise superimposed on them, the circuits have a certain sensitivity to the load currents in the front-end electronics.

Clearly the best way to reduce the sensitivity to tripping from noise is to reduce the noise. In the redesign, special attention was given to how currents flow in the different sub-circuits, especially the high-current circuits. A careful analysis was performed to determine the primary current

loops. The new brick was designed with tight loops and small areas. The board was designed with interleaving ground planes. Differential techniques were used in processing the feedback signals, beginning at the output of the secondary, carried through the opto-isolators, the analog processing circuitry on the primary side, and to the monitoring circuits on the ELMB_MB. In particular, the OVP and OCP circuits are fully differential up to the final comparator. Finally, additional filtering was added to the output stage, and also to the opto-isolator inputs and power pins.

These techniques have resulted in significantly better noise performance, as shown in Fig. 8b, achieving an approximate improvement of a factor of 5 at the highest load currents when measured single-ended. (When measured with a differential probe, the improvement factor is X10–X20.)

Fig. 8a. Output voltage noise of V6.5.4 brick under load.

Fig. 8b. Output voltage noise of V7.3.1 brick under load.

Fig. 8. Comparison of output voltage noise for old version and new version of the brick. Both are +5MB bricks, operating at 6A loads, measured single-ended at the output of the brick.

We had an opportunity to install five prototype boxes onto the detector, four of which were installed in the long barrel, in the December, 2010 shutdown. One measure of the noise improvement is shown in Fig. 9, where the pedestals of the electronics channels for one of the drawers were read out, both with the old bricks and with the new bricks. The improvement at the right side of the plot is due to there being less radiative noise in the new bricks.

Fig. 9. Plot of pedestal noise of the electronics channels in a drawer, comparing the noise from the old supplies and with the new prototype supplies. Plot courtesy of Luca Fiofina.

Another measure of the noise improvement is the spontaneous trip rate. During the 8 months of collisions with the new boxes installed, there was only a single trip of the new supplies compared with approximately 15 trips/module on average for all others in the long barrel. This is shown in Fig. 10. The one trip in the new supplies is consistent with single event upset (SEU), which will be described in Section V.

Fig. 10. Total trips in the Long Barrel for the period February-September, 2011. The four new boxes are in red.

B. Protection of Opto-Isolators

In bench tests, we observed a type of errant behavior in the opto-isolators. When fast noise pulses of sufficient amplitude were superimposed onto the analog inputs (the secondary side in this design), the differential output of the device (the primary side) would become negative (negative output goes to the positive rail.) In the V6.5.4 design, this would cause several events to occur. First, when this occurred on the voltage feedback path, the negative differential value of feedback voltage would cause the LT1681 controller to respond by increasing the output voltage to the maximum

possible value (the clock duty factor of the PWM would go to 45%.) This generally caused the OVP circuit to trip off the brick. Furthermore, subsequent attempts to restart the brick after this occurred would generally fail. Curiously, the brick could remain in this failed state for a long period of time. It was found that short circuiting the primary and secondary grounds together on the bench would “repair” this stuck state. There appeared to be no permanent damage afterward. In fact, this phenomenon was similar to a certain class of failures observed on the detector during the first two years of running, where LVPS boxes would trip off and remain off for an indeterminate amount of time, sometimes weeks. This “stuck state” problem was dubbed the “Lazarus effect” due to the propensity for the circuit to return to working order after an intermediate time. In subsequent discussions with the manufacturer, it was learned that the device needs to be protected from fast spikes, both on the differential inputs and on the voltage supply pins to the chip, using a recommended RC filter of ~ 1 mSec [8]. Of course, in this design, the nature of the switching circuitry produces fast spikes of noise. The filtering was tried on the bench, and was shown to prevent the stuck state from occurring. This has been incorporated into the new design. It was also applied to a small number of boxes on the detector during the December 2010 shutdown. To date, none of the boxes with the improved filtering has exhibited the Lazarus effect.

C. Protection of Integrated Circuits

In careful reading of the manufacturers’ data sheets for the parts used in the design, there were warnings about exceeding the voltage rails on inputs and outputs, especially for the FET driver chip. In the repair and support operations during the 2009 period, records were kept of all failures and what was repaired. The failure of the FET driver chip was among the most prevalent of failures. Under normal circumstances, the voltages are compliant. However, in a large system with floating grounds and distributed power, and limited diagnostic capabilities, it is difficult to ascertain if voltage compliance is met under all conditions, especially when there are power cuts, which does happen occasionally in the experiment. While we were unable to reproduce errant behavior on the bench, we nonetheless followed the manufacturer’s recommendation, and installed external protection diodes on all inputs, outputs, and power pins for the FET driver. A similar analysis was performed on all parts in the design, with appropriate protection also added on the LT1681 chip.

D. Thermal Management

As mentioned above, we recorded all repairs on bricks during the 2009 – 2010 operating period. The two most frequent failures noted were that of the LT1681 controller chip and the FET driver. In bench studies, it was noted that these two parts got very hot. While there is a cold plate in the box, in the V6.5.4 design there was no heat sinking for these parts. In the redesign, we ensured that these two parts had coupling to the cold plate. The parts were placed on the

bottom of the brick (toward the cold plate), and a 0.2" piece of Berquist Gap-Pad [9] was applied to the tops of the chips – just the correct amount of material to provide thermal coupling to the cold plate. A picture is shown in Fig. 11. In addition, there are 13 ceramic posts used in the design to couple the heat from the primary and secondary switching transistors, the power inductors, and the transformer to the cold plate. We changed the material, from Aluminum Oxide to Aluminum Nitride [10], providing ~X9 better thermal coupling of these parts to the cold plate. The results of the overall improvement in the cooling are shown in the thermal images in Fig. 12.

Fig. 11. Use of Berquist Gap Pads to couple ICs to the cold plate.

Fig. 12a. Thermal image of V6.5.4 brick under load.

Fig. 12b. Thermal image of V7.3.1 brick under load.

Fig. 12. Comparison of thermal images for old version and new version of the brick. Both are +5MB bricks, operating at 6A loads.

E. Design for Manufacturing

In the redesign of the brick, we performed a Design for Manufacturability (DFM) analysis, assisted by one of our trusted electronics assembly vendors. Improvements were incorporated into the design, including strict adherence to IPC specifications, placement and size of vias, trace width and spacing constraints, etc. We also developed a formal quality specification for both the printed circuit board fabrication as well as the assembly. Generally, our quality specifications fall under Class 2 IPC specifications. While we did not require Class I, our experience with trusted vendors is such that Class 2 manufacturing is sufficient when coupled with in-house optical inspection, a thorough checkout procedure, and a short 8-hour burn-in. These steps are all being incorporated into our program.

V. RADIATION STUDIES

While the V6.5.4 bricks that are currently installed on the detector had been tested for radiation susceptibility and tolerance in 2004 [11], and despite the fact that a priority in the new design was to use the same parts, it was decided that the new design should be retested for radiation tolerance. These tests began in December, 2010, and continued through May, 2011. The program included tests with neutrons, protons, and gammas.

The radiation limits established for the TileCal LVPS are given in Table II [12]. The table shows the expected dose for 10 years of running at a luminosity of $\mathcal{L} = 10^{34} \text{ cm}^{-2} \text{ sec}^{-1}$, and also the safety factors imposed on the electronics by ATLAS project management. The interpretation of these limits is that there should be no hard failures in irradiation up to these limits, although changes in overall performance may be acceptable depending on the severity and the ability of the overall system to continue to perform at an acceptable level.

10 Years of Running, $\mathcal{N} = 10^{34} \text{ cm}^{-2} \text{ sec}^{-1}$	NIEL Fluency (neutrons/cm ²)	TID (Grays)	SEE Fluency (protons/cm ²)
2005 Requirements	2.74×10^{11}	3.78	6.74×10^{10}
LVPS Survival Limit	5.5×10^{12}	265	1.3×10^{12}
Safety Factor (comp. w/2005 Est.)	20	70	20

TABLE II. SUMMARY OF RADIATION SPECIFICATIONS FOR THE TILECAL LVPS IN THE LONG BARREL REGION. THE DOSE RATES FOR THE EXTENDED BARREL REGION ARE ~AN ORDER OF MAGNITUDE SMALLER. NIEL = NON-IONIZING ENERGY LOSS; TID = TOTAL IONIZING DOSE; SEE = SINGLE EVENT EFFECTS. 1 GRAY = 100 RADS

Of particular interest in these studies was the performance of certain critical parts: the LT1681 controller chip; the IR2110 FET driver; and the HPCL-7800 opto-isolators. The functions of these parts in the circuit were described in Section III.

Facility	Location	Radiation Type	Radiation Source & Test Type
Massachusetts General Hospital	Boston, MA	188 MeV Protons	Cyclotron for cancer therapy; Test for SEE
University of Massachusetts – Lowell	Lowell, MA	1 MeV (equiv) Neutrons	Neutrons from decay of U235 in a research nuclear reactor; Test for NIEL
Brookhaven National Laboratory	Upton, NY	1 MeV Gammas	Decays from a ^{60}Co source; Test for TID

TABLE III. SUMMARY OF RADIATION FACILITIES USED FOR TESTING THE LVPS BRICKS.

For our radiation tests, since the specifications were differentiated by radiation type, we chose three facilities for which there were relatively pure sources of particles. This seemed prudent in order to clearly understand the sources of radiation damage, since the mechanisms are different for each type of radiation. The three facilities that we used and their respective radiation facilities are shown in Table III. We performed six sets of radiation susceptibility measurements in total to test the new LVPS brick design using a combination of new bricks, old bricks, and component test boards for each test. The following is a summary of these studies.

A. Measurements of TID using 1 MeV Gammas

There were no hard failures of bricks during the TID irradiation study. There was a general degradation of performance observed as the total dose increases. Most notable are:

- An increase in clock jitter
- An increase in output noise
- An increase in the clock frequency
- Slow deviations of the monitored voltages
- A tendency of the opto-isolator to eventually fail at very high dose rates. The nature of the failure was such that the brick failed to restart after being turned off in a normal way.
- A tendency of the FET driver to eventually fail at very high dose rates
- A tendency for the overvoltage protection to increase the trip level

We note that these effects for the most part showed up at very high dose rates. We conclude that the design is sufficient for the next decade of running, given the high safety factor imposed on the TID specification.

B. Measurements of NIEL using 2 MeV Neutrons

There were no hard failures during the irradiation studies that were attributable to radiation damage. There was a small degradation of performance observed as the total dose increases. The primary effects noted were:

- Slight decrease in stability
- Small changes in offset voltages.

Since these changes are small, we conclude that the design is sufficient for the next decade of running, given the high safety factor imposed on the NIEL specification.

C. Measurements of SEE using 180 MeV Protons

The measurements of the brick performance to **SEE** showed the following:

- There were hard failures during the irradiation studies. However, these failures are attributed to the exceptionally high total dose that devices under test received from the protons, compared to the TID dose specification (88 krad vs. 44 krad.) The post-radiation study showed consistent component failures as observed with the gamma irradiation tests.
- A significant Single Event Upset (SEU) problem was discovered with the LT1681 controller chip. The problem was traced to a flip-flop in the soft-start circuit inside the chip

The controller chip is at the heart of the design of both the new V7.3.1 bricks and also the existing V6.5.4 bricks. Since this SEU susceptibility exists in the current system, an attempt was made to correlate the trip rate observed from the proton measurements with the trips currently observed in the detector. The conclusion is that the trip rate on the detector is much higher than what would be predicted by SEE in the controller chip.

The soft-start circuit inside the LT1681 controls both the rate at which the brick starts for a cold start, and also the time delay in attempting to restart after a fault. In this design, the latter is not used. When the brick trips from a fault, the circuit is designed to shut down completely, requiring a manual restart. A fix to the SEU problem was found so that the soft-start circuit inside the LT1681 chip operates normally for a cold start, but operates at a faster rate when an SEU occurs. In the latter case, the LT1681 restarts after a time of order two clock cycles, for which there is no observable degradation in performance. All other fault conditions operate normally. This should provide adequate immunity to SEU effects in the higher luminosity running to come in the next decade.

VI. PROJECT STATUS

The redesign effort began in June of 2009. The first prototype LVPS box was constructed in March 2010. It was operated in a test stand at CERN almost continuously until September, 2011, approximately 1.5 years. There were no trips in this time, and the monitored outputs were stable. In November, 2010, we built five boxes, and installed them on the detector during the December, 2010 shutdown of the LHC.

They have been operating on the detector since then.. There has been only one trip in the new boxes through October, 2011. This one trip is consistent with the expectation for SEU-induced tripping described earlier due to the susceptibility within the LT1681 chip. Note that the fix described has not been implemented in these five boxes. We have now launched a production effort to rebuild all 256 of the LVPS boxes on the detector.

VII. PRODUCTION PLANS

The production will take place in two stages. The first stage began in August, 2011, in which we will build 40 boxes for installation onto the detector during the December, 2011 shutdown. The second stage will begin in December, 2011, in which the remaining boxes will be produced. These will be installed on the detector during the long shutdown of the LHC in 2013. In all, we will build 300 boxes, 2400 bricks, to operate the 256 detector modules plus spares. The production effort will be an international collaborative effort from the Atlas Tile Institutes.

VIII. SUMMARY

We have undertaken a project to redesign the LVPS bricks for the Atlas Tile Calorimeter front-end electronics. The primary goals are to improve noise performance, reliability, and tolerance to single-event upset, while retaining the physical layout, interface to the detector control system, and other infrastructure. We have built and tested a new design, and are currently in a production phase. We currently have 5 boxes installed on the detector, which have been operating since February, 2011. We have performed extensive testing on our new supplies, including noise studies, radiation tests, and long-term monitoring. We have begun a production project to replace all of the bricks in the system, and plan to install 40 new boxes on the detector during the December, 2011 shutdown period of the LHC. The complete installation on the detector will occur during the 2013 shutdown of the LHC.

ACKNOWLEDGMENT

The design of this low-voltage power system began in 2001, under the guidance and inspiration of Ivan Hruska of Prague. This was a difficult and challenging system, and we follow from his original design work. We thank the contributions from the Tile Calorimeter physics community for the many hours of data taking, testing, and analysis that contributed to this work. We thank the contributions from the Tile Calorimeter Institutes for the technical help in building and testing the new prototypes. Finally, we thank the staff of the Argonne Electronics Support Group for the technical expertise in assembling and testing the new prototypes.

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