CERN/EF 83-6
21 February 1983

PROPOSAL FOR A FAST, ZERO SUPPRESSING CIRCUIT FOR THE DIGITIZATION
OF ANALOG PULSES OVER LONG MEMORY TIMES

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ABSTRACT

This report describes the design principles of a fast (100 MHz) time and pulse height digitizer that can record up to 15 analog pulses over 10 to 80 μ s memory times. Unlike other triggered circuits prepulse samples are recorded without the help of an analog delay line. The low power requirements of the circuit as well as its fast read-out characteristics make it very attractive for detectors with many digitizing channels.

Conventional circuits are described as a reference for the evaluation of this new design. An ECL 10K implementation of the circuit is presented in the third section.

Submitted to Nuclear Instruments & Methods

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1. INTRODUCTION

Image chambers, for example, drift chambers, jet chambers, track projection chambers, nowadays appear in many high-energy physics (HEP) experiments. They are mostly used for the measurement of particle trajectories with time digitizers which calculate the time differences between the particle interaction and the pulses on the wires (or the pads) of the detector. It is also well known that these pulses carry a lot more physics information than simple, timing and several running spectrometers are equipped with pulse shape digitizers which allow for energy loss measurements and, in some cases, improved double track resolution.

Two basic electronic circuits are used for pulse shape digitization: they are i) the Charge Coupled Device (CCD) analog shift register, and ii) the Flash Analog to Digital Converter (Flash ADC). Unlike the CCD, which has a built-in memory, the Flash ADC output must always be fed into a fast memory buffer which must be sufficiently deep to store all the data produced during the sensitive time of the detector. Moreover, Flash ADC sampling rates have been continuously improving since 1978 as the components became cheaper. Nowadays 100 MHz time and pulse-height digitizers may be considered for use in HEP experiments. Hence, attention needs to be paid to the design of the fast memory buffer as it requires fast, still expensive and power consuming components.

A typical electronics channel might have the following characteristics:

- number of Flash ADC data bits: ≤ 7
- maximum sampling rate: 100 MHz
- memory time: 10 μ s
- buffer size: 1024 words $\times$ 8 bits (note that 1024×10 ns = 10.24 μ s).

Assuming a 10,000 channel detector equipped with the above electronics, a single HEP event would produce 10 megabytes of data which, obviously, could not be analysed and filtered with conventional hardware and software techniques.

In fact, most of the data stored into the fast memory buffer are pedestal (or base-line) values which are not all used by the data analysis programmes and which may (must) be skipped for most physics events:

- i) the buffer size;
- ii) the read-out and processing times; and
- iii) consequently the power per channel

can therefore be significantly reduced if Flash ADC data below a given threshold is not written into the fast buffer. The idea is not new and various circuits have already been proposed and/or designed. Unfortunately, it will be shown in the next section that it is then necessary to match the time and pulse height information for each sample (or, at least, for a set of time contiguous samples). This leads to extra circuitry and the power savings are often negligible. Moreover it is necessary to add an analog delay line in front of the Flash ADC in order to:

- i) compensate for the propagation delay of the circuit that controls the write cycle into the buffer memory;
- ii) record a few samples before the leading edge of the input pulse for base-line monitoring purposes.

The Gray Addressed Time and pulse Height record ER (GATHER) circuit described in the third section of this report does not have the above-mentioned drawbacks. Its proposed ECL 10K implementation has been

optimized for a possible use with the OPAL¹⁾ central detector at CERN and its main characteristics are:

- i) Buffer size: 256 words $\times$ 8 bits.
- ii) Sampling rate: DC to 100 MHz.
- iii) Sensitive time: ∞ to 10 μ s.
- iv) Maximum number of pulses within sensitive time: 15 for a maximum width of 13 time bins, for example, 130 ns at 100 MHz -- (or $\sim$ 10 pulses for an average width of 130 ns).
- v) Dead time: none.
- vi) Analog delay line: none.
- vii) Number of samples before the leading edge of the pulse: 3 or 30 ns at 100 MHz.

2. THREE CONVENTIONAL FLASH ADC DATA BUFFER CIRCUITS

The three circuits described in this section have already been proposed, designed or used by other authors (see Refs. 2 to 4). It is however useful to describe them so that a fair comparison can be made with respect to the proposed GATHER circuit. The following specifications will be used as a quantitative basis for the comparison:

- i) Maximum frequency: 100 MHz.
- ii) Sensitive time: 1024 bins or 10.24 μ s.
- iii) Percentage of non-pedestal data: $\leq$ 25%.

The three circuits are shown in Figs. 1a-c, and they make use of two or more 256 words $\times$ 4 bit ECL bipolar random access memories RAM (Fujitsu MB7071/H or equivalent which offers, for the time being, the best

compromise between speed and organization for this type of application).

The Flash ADC can be the SIEMENS SDA 5010 or SDA 5200.

2.1 The straightforward sample and store circuit

This circuit is shown in Fig. 1a. Eight RAMs are used to form a 1024 words $\times$ 8 bit buffer which is continuously addressed by a 10-stage synchronous binary counter. All pulse height samples are written into memory and therefore available for read-out whenever the event trigger stops the 100 MHz clock generator. (The circuit uses the RAM as a shift register as described in Ref. 5.) If the fast clock is synchronously stopped there is a direct relationship between the memory address and the time at which the pulse height sample was digitized (and stored). Thus, time and pulse shape are easily available for read-out and the main advantages of the circuit are:

- i) Simplicity (especially at low sampling rates (< 20 MHz) where MOS memories can be used);
- ii) Pedestal data are preserved and the physical behaviour of the detector can be fully monitored;
- iii) The address counter can drive several channels.

On the other hand:

- a) A thousand bytes must be read-out per channel and per event thus leading to excessive dead time.
- b) The power dissipation exceeds 10 Watts per channel (for the 100 MHz design).
- c) The "cascading" of the memory chips is technologically difficult and the buffer depth cannot be increased without a significant redesign of the channel electronics.

(In fact the individual memory chips must be fed in parallel with the Flash ADC data as they do not behave as conventional shift registers.)

From a physics point of view, item (ii) is of utmost importance as image chambers are not yet fully understood and the behaviour of the detector may unexpectedly change during its operation. However, one may have some doubts about the possibility of making a per event monitoring of base-lines drifts over several million bytes of data.

2.2 The flagged sample and store circuit

The previous circuit can be improved with some hardwired digital logic on the read-out side to subtract the pedestal and skip the data samples that are below a given threshold. Another method is shown in Fig. 1b: it consists in using a time-over-threshold discriminator and a spare memory bit to flag the pulse height samples which exceed the discriminator threshold. In this way, base-line data can be easily skipped at read-out time and item (a) (Section 2.1) of the sample and store circuit is no longer a problem. Moreover, the whole buffer can be read whenever one suspects a base-line drift.

From a pure physics and data-processing point of view this circuit may be considered as the best one. Nevertheless, the high power requirement and the memory cascading problems remain, especially at high sampling rates.

2.3 The triggered circuit

The only way to reduce the power consumption is to prevent writing base-line samples in which case the buffer depth can be limited to (typically) one fourth of the sample and store circuit. There is no longer a direct

relationship between the memory address and the time at which the pulse height sample was digitized. It is therefore necessary to record the arrival time of each sample (or of a set of time contiguous samples).

Various bit-saving techniques have been proposed to prevent recording the time (10 bits wide) in another fast buffer (see Ref. 4). It is felt that the circuit shown in Fig. 1c is as good as the others with the advantage that it will help the reader to understand the functioning of the GATHER circuit described in the next section.

In a very similar way to the flagged sample and store circuit described in Section 2.2, a discriminator and a flag memory are used to record the arrival time of the pulse height samples which are above threshold. The address of a given flag bit is thus directly related to its arrival time. Whenever a flag bit is set in the flag memory, the Flash ADC output is written into the pulse height memory and the binary counter which addresses it is incremented by one. A pulse height sample is associated with each set bit in the flag memory, but one must still prevent any source of mismatch between the two blocks of data, i.e. pulse heights and flags. This is why a derandomizing circuit is used to synchronize the discriminator output to the 100 MHz clock. Moreover, it is necessary to record a few samples before the leading edge of the input pulse in order to have (after read-out) a good pulse shape analysis. This also applies to the tail of the input pulse and leads to the addition of i) a pulse stretcher at the output of the discriminator and ii) an analog delay line in front of the Flash ADC.

It is readily seen that this circuit is a lot more complex than the other ones and that its only advantages are:

- i) Reduced power requirements (roughly two thirds that of the other circuits).
- ii) Shorter read-out times.

Several weaknesses must be mentioned:

- a) There must be one pulse height memory address counter per channel.
- b) The sampling rate cannot be changed without modifying the analog delay otherwise the number of base-line samples digitized before and after the pulse would change accordingly.

3. GATHER, THE GRAY ADDRESSED TIME AND PULSE HEIGHT RECORDER

3.1 General description

GATHER is a triggered circuit which does not need the analog delay line and where the pulse height memory address counter uses a gray code for its four least significant bits. The gray part of this address counter is free running at the fast clock rate thus scanning a 16-word blocklet (or "page") in the pulse height memory. In this respect the circuit behaves very much like the sample and store circuit described in Section 2.1 as, at any time, 16 "past" pulse height samples are memorized.

A block diagram of the circuit is given in Fig. 2 to help the reader understand the trigger mechanism. Let $GA(t)$ denote the decimal value of the gray address at time t ; whenever the time over threshold discriminator responds to an input pulse, $GA(t)$ is latched into a four-bit register LTRG the output of which is continuously compared to $[GA(t) + 4] \text{ modulo } 16$. It can be seen that 12 time bins later the output of the comparator will:

- i) Flag the pulse height memory;
- ii) Enable the blocklet counter, i.e. the most significant stages of the pulse height memory address counter, thus moving to the next blocklet; and
- iii) Reset the discriminator bistable which stayed set for 12 time bins (120 ns at 100 MHz).

It is then clear that four samples are always recorded before the leading edge of the pulse, i.e. the four past ones that have not been overwritten.

In order to record unambiguously the time at which the input pulse was digitized in its 16 location blocklet of the pulse height memory, it is necessary to utilize a separate 1-bit wide time memory TM. This memory is fed with the discriminator bistable output and it does not need to be deep as part of the time information is available from the comparator flag in the memory blocklet. It will be shown below that the time memory can be eight times shorter than that of the triggered circuit described in Section 2.3. Moreover, it does not need to be of a fast type as the discriminator bistable output is at least 120 ns wide.

Figure 3 is a combined schematic showing how one pulse might be digitized and it will clarify this general description of the GATHER time and pulse height recorder.

Detailed information about the various parts of the circuit are given in the following subsections. The circuit performance will be discussed in the conclusion.

3.2 The gray address logic

Figure 4 shows a conventional synchronous gray code counter as described by various authors. This code is given in Table 1 together with

- i) The decimal and hexadecimal equivalents; and
- ii) The "plus 4" value associated with each gray pattern of 4 bits.

Table 1

Decimal	GRAY					GRAY + 4				
	Hexad.1.	Binary				Binary				Hexad.1.
0	0	0	0	0	0	0	1	1	0	6
1	1	0	0	0	1	0	1	1	1	7
2	3	0	0	1	1	0	1	0	1	5
3	2	0	0	1	0	0	1	0	0	4
4	6	0	1	1	0	1	1	0	0	C
5	7	0	1	1	1	1	1	0	1	D
6	5	0	1	0	1	1	1	1	1	F
7	4	0	1	0	0	1	1	1	0	E
8	C	1	1	0	0	1	0	1	0	A
9	D	1	1	0	1	1	0	1	1	B
10	F	1	1	1	1	1	0	0	1	9
11	E	1	1	1	0	1	0	0	0	8
12	A	1	0	1	0	0	0	0	0	0
13	B	1	0	1	1	0	0	0	1	1
14	9	1	0	0	1	0	0	1	1	3
15	8	1	0	0	0	0	0	1	0	2
		a ₃	a ₂	a ₁	a ₀	b ₃	b ₂	b ₁	b ₀	

a₃ a₂ a₁ a₀ b₃ b₂ b₁ b₀

The logic equations between each bit of the two codes (GRAY) and (GRAY + 4), are:

$$b_0 = a_0$$

$$b_1 = \bar{a}_1$$

$$b_2 = \bar{a}_3$$

$$b_3 = a_2$$

Let ℓ_0, ℓ_1, ℓ_2 , and ℓ_3 denote the bit values latched into the LTRG register of Fig. 2, the addition and the comparison are then directly given by the boolean expression:

$$\bar{c} = (\ell_0 \oplus a_0) + (\ell_1 \oplus \bar{a}_1) + (\ell_2 \oplus \bar{a}_3) + (\ell_3 \oplus a_2)$$

where $\oplus$ and $+$ are respectively the exclusive and the inclusive OR operators.

This logic function can easily be implemented provided the gray code and its complement are synchronous, which, in most designs, is not a problem.

An ECL 10K design of the GATHER circuit is shown in Fig. 5. It can be seen that there is only one logic level between the gray address lines and the $\bar{c}$ line. Moreover, there is no glitch on this line when latching or opening the LTRG register. This results from the fact that one, and only one, bit is changed between two consecutive gray values.

Two technological advantages must already be emphasized; they are:

- i) The extreme simplicity of the adder and comparator circuit which requires only two conventional integrated circuits;
- ii) The small amount of on-board noise generated by the gray address lines, especially when balanced lines are used for the four bits of the gray code.

3.3 The time digitizer logic

As described in Section 3.1 the comparator output $\bar{c}$ is used to flag the last pulse height in a blocklet of 16 locations. It is therefore sufficient to record the discriminator bistable output LT every eighth time bin into a 1-bit wide time memory TM (see Fig. 5).

The width of the LT signal depends on the time over threshold of the input pulse and can be expressed in number of time bins as:

$$\text{Width (LT)} = 12 + k * 16$$

where k is a positive integer.

The memory address counter of the time memory is the most significant part of a 10 (or more) bit synchronous counter of which the four least significant bits are used to generate the gray code. Thus, TM memory locations are unambiguously related to gray code values. Assuming a two time-bin wide write pulse (20 ns at 100 MHz) covering the third and the fourth states (modulo 8) of the gray code, then the correspondence between the gray code and the time memory address is that given in Table 2.

Table 2

GA (decimal)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
GRAY (hexad.1)	0	1	3	2	6	7	5	4	C	D	F	E	A	B	9	8
Memory address P	$2n$								$2n + 1$							
Write pulse	W W								W W							
Change of address	X								X							

If P denotes the address of the first set bit in a backward scan of the time memory; the sampling time t of the flagged pulse height can be found as follows:

- i) If P is even, then the decimal value GA of the gray address can be directly added to $P * 8$ and

$$t = P * 8 + GA . \quad (1)$$

- ii) If P is odd, then the pulse may extend over the gray addresses of location $(2n + 2)$ and

$$t = (P - 1) * 8 + GA \quad \text{if} \quad GA > 7 \quad (2)$$

or

$$t = (P + 1) * 8 + GA \quad \text{if} \quad GA < 8. \quad (3)$$

These three mathematical formulae can be implemented in a straightforward circuit as shown below.

Let

- P_0 denote the least significant bit of P ;
- GA_3 denote the most significant bit of GA ; and
- GA_8 the modulo 8 value of GA ,

then

$$t = (P + P_0 \oplus GA_3) * 8 + GA_8$$

where $+$ is the arithmetic ADD operator, $\oplus$ the exclusive OR operator and $*$ the arithmetic multiply operator.

Hence, it is clear that time and pulse height data can be uniquely matched and that small time memories can be used to cover long sensitive times.

For a 100 MHz sampling rate

- 128 word $\times$ 1 bit TM memory will cover 10.24 μ s; and
- a 1024 word $\times$ 1 bit TM memory, 81.96 μ s!

3.4 Read-out procedure

It was shown in the previous subsection that the discriminator bistable output width (LT - Fig. 5) covers $(12 + k * 16)$ time bins. Thus one might think that a blocklet always corresponds to a pair of locations in the time memory. This is unfortunately not true for the rare situation

where the time distance between consecutive pulses is 13, 14, or 15 time bins. It is therefore necessary to recognize this situation in order to prevent any mismatch between the set bits in the time memory and the blocklets.

During read-out, the two memories (time and pulse height) are backward scanned and a blocklet can be transferred as soon as a set bit is found at address P in the time memory TM . The problem is then to know whether the next (previous!) TM location can be skipped or not.

Let t_ℓ denote the timing of the last sample in the current blocklet, then if $t_\ell - 16$ covers the previous location of the TM memory, this location can be skipped as:

- i) If it corresponds to a stand-alone pulse, it does not matter;
- ii) If it corresponds to a 12 time bin pulse preceded 13, 14, or 15 time bins earlier by another one, the latter will necessarily cover the location $(P - 2)$ of the TM memory and it will not be omitted nor mistimed.

On the contrary if $t_\ell - 16$, as a result of k consecutive situations (ii), does not cover the location $(P - 1)$ of the TM memory, this location must not be skipped as it may be set and therefore correspond to the previous blocklet.

Figure 6 is the flowchart of the read-out procedure. Initialization statements and exit tests are not shown as they depend on the sensitive time of the channel.

It can be seen that very few signals are needed to operate the circuit in the read-out mode; they are:

- The memory write/read;
- The memory chip select when several channels share the same read-out logic;
- The counters up/down; and
- Two read-out clocks.

3.5 The proposed ECL 10K design

Figure 5 shows an ECL 10K version of the GATHER circuit.

The discriminator is an AMD 685 followed by a gate and a conventional set-reset bistable. The disable D signal is controlled by the stop logic (not shown) in order to make sure that the bistable is reset before read-out starts.

The time memory TM is an MCM 10147 (or equivalent) thus allowing for a 10.24 μ s memory time. The other integrated circuits are:

- A 10136 up/down 4-bit binary counter.
- A 10153 quadruple latch.
- A 10113 quadruple exclusive OR, and
- A 10102 quadruple NOR.

The 256 word $\times$ 8-bit memory is built with two MB 7071/H and the total power dissipation is 5 W including the 6-bit Flash ADC.

The equivalent sample and store circuit would dissipate 10 W and use the same number of components.

Finally, base-line data can be found in the last blocklet of the pulse height memory which is continuously overwritten until the read-out starts.

4. CONCLUSION

It was already pointed out in the second section of this report that the flagged sample and store circuit is the most powerful one as it preserves all the data produced by the detector during its sensitive time. The GATHER circuit cannot beat it on these grounds. However, the latter should be preferred whenever:

- i) There is a large number of channels.
- ii) The sampling rate is high, i.e. ≥ 50 MHz.
- iii) The sensitive time exceeds $10 \mu\text{s}$.
- iv) The number of pulses is smaller than 15.

The 16 location blocklet design described in this report can be modified, e.g. 8 location, to make more efficient use of the time memory.

Because of its reduced power requirements (50%) and its fast read-out time (5 times faster) the GATHER circuit opens up the possibility of high sampling rates to detectors that have long memory times.

Acknowledgements

The author wishes to acknowledge the participation of the members of the OPAL central detector electronics working group in useful meetings. He would also like to thank Messrs. T. Armstrong, W. Beusch, and R. Hammarström for their constructive reading of the manuscript.

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Figure captions

- Fig. 1 Schematics of three conventional Flash ADC data buffer circuits. The sample and store circuit a) has a $1024 \text{ word} \times 8 \text{ bit}$ memory M1; a free bit is used in the flagged version b) to flag the pulse height samples that exceed the discriminator DSC threshold and thus speed up read-out and data processing. The triggered circuit c) has a smaller memory M2 ($256 \text{ word} \times 8 \text{ bit}$) which is addressed by a sample counter SMPL CNTR; the time position of the stored samples is memorized in a time memory M3 ($1024 \text{ words} \times 1 \text{ bit}$), once the discriminator output (DSC) has been stretched (STR) and de-randomized (DRM); the analog delay DLY compensates for the propagation delay of the DSC, STR, DRM, and M3 circuits.
- Fig. 2 Schematic of the Gray addressed time and pulse height recorder. The gray part of the address generator is freely running at the fast clock rate and scans a 16-word blocklet in the pulse height memory. Whenever the input signal exceeds the discriminator DSC threshold, the LT bistable latches the gray address into the LTRG register; 12 time-bins later the comparator output $\bar{C}$ goes low, enables the blocklet counter CNTR and clears the LT bistable. This circuit utilizes a smaller time memory than conventional triggered circuits and it does not need an analog delay line.
- Fig. 3 Combined schematic showing how a pulse might be digitized, flagged and timed in the two memories of the GATHER circuit (refer to Fig. 2 for mnemonics).

- Fig. 4 Schematic diagram of a Gray counter. The use of a synchronous binary counter suppresses glitches on the gray lines.
- Fig. 5 Diagram of an ECL 10K design of the GATHER circuit. Address lines may be common to several circuits. (Mnemonics are self-explanatory and/or may be found in Figs. 1 to 3.)
- Fig. 6 Flow chart of the inner read-out loop of the GATHER circuit.

Fig. 1

Fig. 2

B6

Fig. 3

Fig. 4

Fig. 5

Fig. 6