C/VHDL Codesign for LHCb
VELO zero-suppression algorithms

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Introduction – TELL1

LHCb DAQ Interface Board (EPFL)  x300

36 values * 64 links * 1.1MHz * 10bit = 2.95GB/s

64 links @ 40MHz or 24 fibers @ 1.2Gbps

DSP on 5 Altera Stratix EP1S25 ..evolving algorithms ..at high data rates

50.44 cluster * 1.1MHz * 2B = 106MB/s

2 (4) GBE copper links

(L1 raw bandwidth w/o protocol overhead)
Motivation – Code Consistency

FPGA Design (VHDL)

DSP

parallel progress - how to guarantee consistency?

System Simulation Framework (C++)

DSP on FPGA

C/VHDL Codeign
Manfred Muecke
Requirements

to guarantee consistency, one of the two models has to be generated automatically.

? → VHDL
- syntesizeable VHDL
- latency as design parameter
- efficient resource usage

? → C
- fast execution
- simple integration/interface
Chosen solution

Confluence – a synchronous hardware generation language and compiler

Confluence Compiler + Code Generator
Confluence

Open source project (www.confluent.org)

.. functional language for synchronous systems
.. written in O’Caml
.. runs under Unix/Linux/Cygwin/..

.synthesizable VHDL

.bit- and cycle-accurate C-model
Common code base

FPGA Design (VHDL) -> DSP.cf -> System Simulation Framework (C++)

DSP (VHDL) -> DSP on FPGA (C)
Example - Linear Common Mode Suppression

- Calculates mean, slope and deviation over 32 samples
- 40MHz data stream (x16/FPGA)
# Measurements

<table>
<thead>
<tr>
<th>LCMS</th>
<th>Handcoded VHDL</th>
<th>Confluence</th>
<th>C</th>
<th>VHDL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resources (LE, memory bits)</td>
<td>235 LEs, 7680 bits, 2 9bDSP</td>
<td>-</td>
<td>329 LEs, 1088 bits, 6 9bDSP</td>
<td></td>
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<tr>
<td>VHDL simulation time (ModelSim)</td>
<td>~120s</td>
<td>-</td>
<td>~80s</td>
<td></td>
</tr>
<tr>
<td>C runtime (gcc)</td>
<td>-</td>
<td>&lt;1s</td>
<td>-</td>
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Outlook

- Implementing further algorithms
- Integrating C model in VELO simulation
- Automated checking of model consistency
- Language features for DSP

- Other solutions/languages?
Links

LHCb - http://lhcb-public.web.cern.ch
TELL1 - http://lphe.epfl.ch/~ghaefeli

Confluence - http://www.confluent.org
O’Caml - http://www.ocaml.org

email - Manfred.Muecke_at_cern.ch
Thanks for your attention!

Questions?
Algorithm → VHDL

- IP-based source (Simulink)
  (Xilinx, TI, Synplicity DSP Synthesis, ...)
  - vendor locked (MathWorks + TI/...)
  - limited/application-specific IP

- Algorithmic source (behavioural synthesis)
  - on the go (Celoxica, Mentor Catapult C, Forte’s Cynthesizer)
  - SLDL efforts: SystemC, SystemVerilog
  - no RTL control (latency)

=> as of now, we still have to code in VHDL/RTL (if we care about speed)!!
Confluence features

- Functional language (recursion)
- Dynamic typing (ports adapt)
- List type
- Vector type -> Hardware
- Purely synchronous
- Implicit Synchronization (clock, reset, enable)