C/VHDL Codesign for LHCb VELO zero-suppression algorithms

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Introduction – TELL1

LHCb DAQ Interface Board (EPFL) x300

36 values * 64 links
* 1.1MHz * 10bit
= 2.95GB/s

64 links @ 40MHz
or
24 fibers @ 1,2Gbps

(L1 raw bandwidth
w/o protocol overhead)

50.44 cluster
* 1.1MHz * 2B
= 106MB/s

2 (4) GBE
copper links

DSP on 5 Altera Stratix EP1S25
..evolving algorithms
..at high data rates

Motivation – Code Consistency

Requirements

- to guarantee consistency, one of the two models has to be generated automatically..

? → VHDL

- synthesizable VHDL
- latency as design parameter
- efficient resource usage

? → C

- fast execution
- simple integration/interface

Chosen solution

Confluence –
a synchronous
hardware generation
language and compiler

Confluence

Open source project (www.confluent.org)

..functional language for synchronous systems

..written in O'Caml

..runs under Unix/Linux/Cygwin/..

`.vhd` synthesizable VHDL

`.c` bit- and cycle-accurate C-model

Common code base

Example - Linear Common Mode Suppression

- calculates mean, slope and deviation over 32 samples
- 40MHz data stream (x16/FPGA)

Measurements

LCMS		Handcoded VHDL	Confluence	
			→ C	→ VHDL
Resources (LE, memory bits)		235 LEs, 7680 bits, 2 9bDSP	-	329 LEs, 1088 bits, 6 9bDSP
VHDL simulation time (ModelSim)	1 000 000 cycles P4 2,6GHz	~120s	-	~80s
C runtime (gcc)		-	<1s	-

Outlook

- Implementing further algorithms
 - Integrating C model in VELO simulation
 - automated checking of model consistency
 - language features for DSP
-
- Other solutions/languages?

Links

LHCb - <http://lhcb-public.web.cern.ch>

TELL1 - <http://lphe.epfl.ch/~ghaefeli>

Confluence - <http://www.confluent.org>

O'Caml - <http://www.ocaml.org>

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Thanks for your attention!

Questions?

Algorithm → VHDL

- IP-based source (Simulink)
(Xilinx, TI, Synplicity DSP Synthesis, ...)
 - vendor locked (MathWorks + TI/...)
 - limited/application-specific IP
- Algorithmic source (behavioural synthesis)
 - on the go (Celoxica, Mentor Catapult C, Forte's Synthesizer)
 - SLDL efforts: SystemC, SystemVerilog
 - > no RTL control (latency)

=> as of now, we still have to code in VHDL/RTL (if we care about speed)!!

Confluence features

- Functional language (recursion)
- Dynamic typing (ports adapt)
- List type
- Vector type -> Hardware
- Purely synchronous
- Implicit Synchronization
(clock, reset, enable)