The upgrade of the ATLAS Inner Detector

D. Ferrère, University of Geneva

On behalf of the ATLAS collaboration

12th Pisa Meeting on Advanced Detectors
La Biodola, Isola d'Elba (Italy)
May 20 - 26, 2012
LHC Plans and Upgrade Phases

The future observations at LHC should drive physics investigations at HL-LHC

The Machine and the Detectors are working towards the Upgrade Phases to improve the performances as well as the life time.
Features:
- 4th Pixel layer (instead of b-layer replacement)
- Closer interaction point (5.05 → 3.27mm)
- Smaller pixels (50 x 250 μm²)
- Better sensors, better R/O chip
- More robust tracking
- Better performance

Reduce beam pipe diameter (47 mm) in Beryllium under production
IBL Layout and Features

IBL features:
- 14 staves overlapping in Phi and mounted around the beam pipe on support rings
- Small clearances between beam pipe - IBL - IST : 2.5 to 2.7mm
- Stave to stave gap is only 0.8mm → Integration for the last stave delicate
- Instrumented stave made of 12 planar and 8 3D sensor modules along 664mm
Sensor Technologies

Planar sensor – n-in-n
Charges are collected at the strip surface

3D sensor
Charges are collected at the bulk implanted electrodes

<table>
<thead>
<tr>
<th>Structure</th>
<th>Planar</th>
<th>3D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness (nominal) [μm]</td>
<td>200</td>
<td>230</td>
</tr>
<tr>
<td>Depletion voltage [V]</td>
<td>~35</td>
<td>10 - 25</td>
</tr>
<tr>
<td>Working voltage after LHC fluence (5x10^{15} 1MeV n_{eq}/cm^{2}) [V]</td>
<td>~1000</td>
<td>~160</td>
</tr>
<tr>
<td>Module width [μm]</td>
<td>41325</td>
<td>20450</td>
</tr>
<tr>
<td>Active size WxL [mm^{2}]</td>
<td>16.8 x 40.9</td>
<td>16.8 x 20.0</td>
</tr>
</tbody>
</table>

Production status:
- Planar sensors from CiS: **424 good double chip (DC) tiles** (89.1 % yield) - IBL needs 168 tiles (75% planar).
- 3D sensors from CNM & FBK: **306 good tiles** as today (62% yield) – IBL needs 112 tiles (25 %).

1st time 3D sensors will be used on a Si-tracker
Efficiency

A number of pixels does not work after proton irradiation (TID ~ 3x IBL lifetime)

Same behavior for both sensor types => FE-I4 “feature” (Pixels masked during analysis) will be addressed with FEI4b

Charge collection
FEI4 main features:
- IBM (130 nm)
- 70 Million transistors
- 26880 pixels (50 x 250 μm²)
- Lower noise than FE-I3 (~150e- with sensor)
- Lower threshold operation
- Higher rate compatibility
- Radiation hard to >250Mrad
- In use for pixel R&D and towards Upgrade phase 2

Through the FEI4 progresses:
- First version FEI4a for validation and IBL prototypes (32 FE-I4A wafers received in 2010/11)
- FEI4b features: minor fixes + r/o functionalities + uniform pixel matrix + Power functionality
- First FEI4b delivery in Dec. 2011
- FEI4b now in production (30 wafers) and wafer probing is almost completed (yield ~60%)

FEI4b noise before and after irradiation: 114e → 124e (both tuned)
Module Production Status

- Production is in progress in two assembly sites
- Started first with FEI4a module production for stave 0
- FEI4b modules has just started – PRR is programmed for beginning of June

Thin module process steps (100 and 150μm thick FE):

1. FE-I4 wafers thinned
2. glued on glass support wafer
3. bump deposition
4. dicing wafer & substrate
5. flip-chip & reflow
6. substrate wafer removal by power laser.

Modules with FEI4a

Am241 source scan

Layout of the SMD components are clearly visible

Planar module

Typical Noise scan

3D module
Stave and Flex Features

<table>
<thead>
<tr>
<th>Stave features:</th>
<th>Flex features:</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Made of light material (K9 carbon foam + CFRP skins for stiffness)</td>
<td>- Mix of 4 Cu-layers and 2 Al-layers for the LV lines. Total thickness ~450μm</td>
</tr>
<tr>
<td>• Ti pipe of 1.5mm ID and 0.1mm wall thickness</td>
<td>- The 2 Al-layers needs to be processed with CVD for Chrome and Copper (vias)</td>
</tr>
<tr>
<td>• Face plate (module side) is coated with Parylen for safer electrical break to detector HV</td>
<td>- The wings supply through 1 layer the connectivity for every FE. Wing thickness 70μm</td>
</tr>
<tr>
<td>• Tight planarity and envelope tolerance: +/- 0.1mm</td>
<td>- Wings are folded and glued for very precise envelope required for the integration</td>
</tr>
<tr>
<td>• Stave fixations on 3 points: 2 end-blocks + central support</td>
<td></td>
</tr>
</tbody>
</table>

**Stave & flex pre-production started and OK**

- ID 1.5mm Ti boiling pipe
- K13C/RS3 Omega Stiffener
- K9 Foam block
- K13C/RS3 parylen coated face plate
- Flex Bus
- Peek end blocks

**1st AlCu flex ever made for tracker in fabrication for IBL**
Module Loading and QA

The module loading and QA consists of 16 working steps

Key features of the loading procedure:
- Modules are mounted with a thermal grease interface + epoxy glue drops
- Thermal grease was qualified for its good thermal performance and for its radiation hardness
- Rework and module replacement is possible but not straight forward

⇒ Module and flex QA prior to loading is essential

- All staves will be thermal cycled with loaded modules for QA – Electrical tests and metrology survey will be made before and after this operation
- Electrical insulation between HV groups will be done ⇒ Thin polyimide layer in module gaps

The stave will remain on a **handling frame** for all assembly and QA operations including the pipe extension and the integration around the beam pipe. One per stave with high precision machining.
Stave Integration

Staves Assembly around the New Beam pipe with the MPC (Multi-Purpose Container)

IBL_MPC (8.9m long)

1. Stave pipe extension to 7m - Brazing technique
2. MPC as a multi purpose object for: BP container, stave loading, IBL Test bench and, IBL container.
3. Testing has been performed on an IBL_MPC 1.6m long prototype (done in January)
4. IBL_MPC proto to be used for IBL Integration checks, sealing issue, interfaces with LPSC “tables”

IBL_MPC prototype @ UNIGE (1.6m long, cut out successfully)
Integration & Installation

Two viable options are investigated:
- IBL to Pixel integration in the surface building associated to nSQP installation
- IBL to ATLAS integration in the pit

IBL to Pixel integration in SR1

ITT already in SR1
Integration scenario clearly defined

Pixel Integration & Testing Tool

IBL to ATLAS integration in the pit

“ID” Mock up – Bldg180

Dummy IST

Insertion Table

Long Guiding Tube (LGT)
**CO2 Cooling**

*Test bench allowed to evaluate IBL system* (branch + stave):
- Coolant at -39°C → Stave -24.4°C (60% of the DeltaT due to the stave TFoM)

**Joint CERN-PHDT & Nikhef responsibilities**

- Plant construction @ Nikhef (by April 13)
- Integration of electronics @ CERN (May-June 13)
- Commissioning of cooling plant (July-Sep. 13)
- Installation in Cavern: Oct. 13

**Diagram:**

- Junction box @ Muon Sector 5 (Accessible)
- Vacuum insulated concentric tube (~13m)
- Vacuum insulation
- Vacuum lines
- Dummy load

**14 IBL staves (7 flow pairs)**
- (7x A→C flow / 7x C→A flow)

**Cooling Unit A**

**Cooling Unit B**

**Identification:**
- USA-15
Pixel nSQP – new Service Quarter Panels

**nSQP features:** (pending decision by mid 2012)
- No optical transceiver inside the ID region (VCSEL problems on ID triggered the project)
- On-detector optoboards replaced by new accessible optoboards located at ID End-Plate
- Reproduces the Pixel services with design improvements
- Add long-term reliability to the operation of the detector

**Installation and Integration (2013-2014) in phase with IBL at the surface building**

**Pixel running experience 2010 + 2011**
- Data taking efficiency in 2011: 99.8%
- 95.9% of Pixel modules are active
  - 2.1% before LHC turn
  - 2.0% lost in 2010 + 2011
- Problems constantly increase after cooling cycles and ~equally distributed

**nSQP is expected to improve Pixel efficiency & reliability**

[Image: Pixel during integration in SR1]
DBM – Diamond Beam Monitor

The goals of DBM:
✓ Luminosity
  • Monitor luminosity delivered to ATLAS for individual BCIDs
  • Aim for % level accuracy in lumiblock (1-2 minutes)
✓ Beam Spot
  • Unbiased (trigger) beam spot monitoring
  • Aim for ~1cm accuracy per event
✓ Background monitoring
  • Topology of BG different than IP interactions
✓ Track Trigger test-bed
  • Possible test-bed for ideas (pattern reco., tracking, …)

DBM installation is linked to IBL and nSQP integration and installation

3 successive modules pointing towards the IP

Noise map of a DBM module

Module on test board
ID Upgrade Phase 2 - Topics

**Topics under investigation for the tracker upgrade:**

- **New ID layout:** Only silicon pixel and strip detectors ↔ Simulations
- **Trigger:** Si-track trigger for L1 decision is considered using RoI
- **New detector technology:** n-in-p planar for strips and pixel (slim and active edges), 3D-sensors & Diamond (innermost layers), Gossip – Current R&Ds efforts
- **New ASICs technologies:** Deep submicron 250 nm → 130nm
  - Pixel FEI4b in production + R&D in 65nm
  - Strip ABCN130 to be submitted at the end of 2012
- **Cooling with more headroom:** CO2 plant for coolant down to -35°C or lower
- **New powering scheme:** Serial powering or DC-DC for parallel powering
- **Faster readout:** FE asics (160/320 Mbps) and optical link (5Gb/s)
  - SCT 1.3 kch/link → Upgrade up to 123 kch/link
- **SCT Module integration** will be grouped on a stave or a super-module structure
- **DCS** is proposed to be partially integrated into the readout architecture
- **Engineering:**
  - Assemble and commission the complete ID in a surface building
  - Service reuse of cables between counting room and detector
- **Installation:** Limited access time inside the cavern → Need clear and well prepared integration plans
- Classical layout – Barrel & Disk
- 2 innermost pixel layers should be replaceable (IST R=11 cm)
- Full pixel package should be replaceable
- Pixel services should be axial

**I-beam stave concept for Innermost 2 layers**

**Possible options for outer layers**

Goal is to reduce or suppress disc → material budget saving

**Conical layout**

**Alpine stave concept**

**Real prototype for feasibility**
**Strip Tracker – Stave & Petal**

**Features:**
- Single sided modules mounted on each side of core structure (Carbon foam + CFRP planes)
- Cooling pipe embedding into the core structure
- Stave service bus is laminated with the core structure and modules are glued on top
- Hybrids are directly glued on top of the Si-strips and are serviced at each side of the sensor
- Stave design is compact

**Thermo-mechanical stave**

**Petal layout**

**Progress so far:**
- Successful module production in several institutes with ABCN250
- Stavelets with 4 module evaluated with success on system tests – Noise performance with Serial and DC-DC powering configurations
- Thermo-mechanical measurement of real stave has been studied
- Hybrid and sensor designs in progress for matching the new FE in 130nm technology with 256 ro channels
Strip Tracker - Super-Module

Features:
- Double sided modules allowing for space point reconstruction (back-to-back sensors mounted to few µm)
- Module mounting with Z-overlapping for full hermeticity
- Module symmetry and bridged hybrids allowed for very low thermo-mechanical deformation (< 2µm out of plane)
- 12 modules are precisely mounted with grease joint on a local support with cooling pipe and plates on the sides.
- Modularity allows for modules and items replacement during production or even late after integration

Module noise inside test box and on local support very similar and uniform

Super-module prototype for 8 modules
5 modules are mounted with DC-DC

Light local support CRFP structure for 12 modules + CC cooling plates
### Summary

**Phase 0 long shutdown will allow:**

- The ATLAS ID to insert in 2013/14 a new innermost Pixel layer namely IBL
- **IBL is possible thanks a new reduced beam pipe** diameter now in production (delivery in Fall)
- **IBL layout is a mix of planar and 3D sensor technology** integrated on the stave
- **The FEI4 readout chips is one of the key items** which is working fine and the latest version is in production – Also used for future Upgrade development
- The IBL parts are in production – **Schedule is on a fast track**

### Phase 2 long shutdown – R&D:

- Pixel and Strip communities are both working on the layout, the module and the integration concepts
- **Pixel** is focusing on **sensor R&Ds** and working on **integration of multi-FE modules**
- **Strips** R&Ds have **integrated multiple modules into system tests** with DC-DC and serial powering
- **Strip ABCN front-end readout in 130nm technology is under design** and will be submitted by the end of 2012