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A CMOS 0.13 μm Silicon Pixel Detector Readout ASIC for the PANDA experiment¹

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ABSTRACT: The ToPiX ASIC is a custom development for the hybrid pixel sensors of the PANDA experiment Micro Vertex Detector. The ASIC will provide both the time and amplitude informations (via the Time over Threshold technique) of the incoming particle. ToPiX will consist of a matrix of 116×110 cells with a pixel size of $100 \times 100 \mu\text{m}^2$, the column readout logic and two 311 Mbit/s serializers. A reduced scale prototype in CMOS 0.13 μm has been designed and tested. The prototype includes eight columns with the full cell analogue and digital circuitry and the end of column readout.

KEYWORDS: Radiation-hard electronics; Front-end electronics for detector readout; Digital electronic circuits

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Contents

1	Introduction	1
1.1	The micro-vertex detector	1
1.2	The silicon pixel detector	1
2	The ToPiX ASIC	2
2.1	Pixel cell	3
2.2	Column readout	4
3	ToPiX prototype	5
4	Test results	5
5	Conclusions	7

1 Introduction

The PANDA experiment [1] at the future FAIR facility under construction in Darmstadt, Germany, aims at the study of the antiproton-proton and antiproton-nucleus annihilation reactions. By taking advantage of the physics potential provided by the high-intensity phase-space cooled antiprotons provided by the HESR, the PANDA experiment will perform a wide program of particle and nuclear physics.

PANDA is characterized by the absence of an hardware trigger signal. Therefore all data coming from the detector has to be tagged with a time stamp and sent out to the data acquisition system. This poses a great challenge on the data transmission system, especially for the innermost detectors where the track density and the material budget requirements are more stringent.

1.1 The micro-vertex detector

The micro-vertex detector (MVD) is the innermost part of the PANDA apparatus. It consists of silicon detectors, arranged in a 4 barrel layers around the interaction point and in 6 disks in the forward direction. Silicon Pixel Detectors (SPDs) are used for the first two barrel layers, the first 4 disks and the inner part of the the last two disks. The rest of the MVD is made of Silicon Strip Detectors (SSDs). Figure 1 shows the MVD layout.

1.2 The silicon pixel detector

The SPDs for the PANDA experiment make use of the well-known hybrid technology. The silicon detector, made on a p-in-n epitaxial substrate, is bump-bonded to the readout electronics. Silicon detector based on epitaxial layer substrate has been chosen for its better radiation tolerance, as reported in [2].

Figure 1. PANDA Micro Vertex Detector.

Table 1. ToPiX specifications.

N. of rows	116
N. of columns	110
Pixel cell size	$100 \times 100 \mu\text{m}^2$
Clock frequency	155.52 MHz
dE/dx measurement	ToT, 12 bits dynamic range
Noise floor	$< 32 \text{ aC} (200 e^-)$
Time resolution	6.45 ns
Power consumption	$< 750 \text{ mW/cm}^2$
Particle rate	up to $6 \cdot 10^6 \text{ hits/s}$
Total ionizing dose	$< 100 \text{ kGy}$

2 The ToPiX ASIC

The unique requirements for the electronic readout of the SPDs of the PANDA experiment, mainly related to the absence of a trigger signal, lead to the development of a custom readout ASIC [3]. The ASIC, named ToPiX, is a matrix of 116 rows and 110 columns of $100 \mu\text{m} \times 100 \mu\text{m}$ pixel cells. ToPiX provides the position, the arrival time and the measurement of the injected charge of the crossing particle. Table 1 summarizes the ASIC specifications.

The time and energy measurements are performed as follows. A 12-bit time stamp signal is transmitted to all pixels in the matrix in order to have a common time reference. The current time stamp value is stored into the pixels only when a signal is detected by the preamplifier-comparator chain. In order to obtain the signal amplitude information, the time stamp at the trailing edge of the comparator is also stored. A simple Time over Theshold (ToT) mechanism is therefore

Figure 2. Schematic of the pixel cell.

implemented by adding a register and storing the time stamp value at both edges of the comparator signal. This measurement technique has been already successfully implemented in other ASICs for silicon pixel readout [4]. Another advantage of this technique is its intrinsic capability to operate also when the input preamplifier is saturated, thus making it very attractive for the large dynamic range (up to 50 fC) foreseen in the PANDA environment.

The ASIC is designed in a commercial CMOS 0.13 μm technology in order to take benefit of the high integration level of modern technologies and of the intrinsic resistance to radiation in terms of total ionizing dose.

ToPiX communications uses CML differential drivers in order to reduce the switching noise of the output drivers and to be able to drive signals few tens of centimeter away at high speed. Owing to the 1.2 V power supply, the well known LVDS standard has not been adopted and replaced by SLVS [5]. Albeit LVDS driver can be designed in this technology using 2.5 V compatible transistors, a second power supply would have been required. Moreover, these thick oxide transistors show a much higher threshold voltage shift under irradiation than the standard ones.

2.1 Pixel cell

The pixel cell, shown in figure 2 is based on a charge amplifier with a constant current feedback circuit in order to linearly discharge the feedback capacitor. The pixel threshold voltage is programmable at the pixel level via a 4 bits DAC.

The value of the time stamp bus corresponding to the rising and the falling edges of the comparator output is stored in two 12-bits registers. When both registers have been loaded the pixel control logic goes into a busy state. The internal busy signal is put in logical OR with the busy of the previous pixel cell and sent to the following one. A single busy signal is thus sent to the end of column logic which starts the readout sequence. If more than one pixel is busy, the pixel with the highest priority (i.e. the one with busy=0 at its input) sends its data to the end of column logic

Figure 3. Schematic of the end of column circuitry.

via the address and data bus. Leading and trailing edge time stamps are read-out from the data bus in two successive readout cycles. Meanwhile the pixel address is always present on the address bus. When the readout operation is completed (i.e. the read_cmd signal goes down) the pixel exits from the busy state and the following busy cell can start the transmission. A veto circuit masks the comparator output when the pixel is in the busy state. An 8-bit configuration register is used to retain informations about the threshold DAC setting, the pixel masking and the test signal enable.

2.2 Column readout

A simplified schematic of the column readout is shown in figure 3. The pixel cells are organized in double columns with common time stamp, address and data buses. A column control readout unit (CRCU) receives the busy signal from the two columns and controls the pixel readout signals and the end of column sense amplifiers. The data read-out from the pixel column are stored into a FIFO. The output of the FIFOs corresponding to the 55 double columns are read-out by a chip control unit (CCU) which sends the FIFO data to the output serializers for data transmission.

Both the FIFO registers and the CRCU and CCU state machines are protected against SEU via Hamming encoding. A SEU in the state bits is detected and corrected in the successive clock cycle. Therefore the protection scheme is ineffective only when two or more errors occur in the same clock cycle. In the FIFO a less robust scheme has been implemented for the data in order to save chip area: the information is encoded during the write operation and decoded during the read operation. No correction is performed when the data is stored into the FIFO.

The serializer is basically a shift register switching on both sides of the clock signal. It is therefore possible to achieve a data rate twice the clock frequency without using a PLL for clock multiplication.

Figure 4. Prototype layout.

3 ToPiX prototype

A reduced scale prototype with all the main building blocks (apart from the double rate serializer) has been designed in a CMOS $0.13\ \mu\text{m}$ technology, produced and tested. The prototype includes two 256-cells double columns and two 64-cells double columns with the full analogue and digital circuitry, the end of column logic with the end of column buffer and the control logic and the chip control logic with the serial slow control interface. The die size is $4.5 \times 4\ \text{mm}^2$. Figure 4 shows the chip layout.

4 Test results

The electrical tests of the chip have been performed using the integrated test circuitry, which allows to inject a programmable charge to the preamplifier input of one or more pixels. The circuit operates as follow: a calibration level is set via an external DAC; a digital pulse is then fed into the circuit from a test input which generates a voltage step with amplitude equal to the calibration level to an on-pixel 36 fF capacitor connected to the input of the preamplifier. The pulse is enabled by a test enable bit in the pixel configuration register, thus making possible to select any combination of pixels for the test pulse injection. The pixel configuration register also allows the connection of the pixel comparator output to an external line for test purposes. In this case only one pixel at time can be enabled to avoid conflicts.

Figure 5. Measured analogue gain and noise.

In the current test set-up, all control lines with the exception of the test pulse and the comparator test output are controlled via an FPGA-based board which in turn is connected to a PC via an ethernet cable. The test system is therefore very compact and will also be used for the test beams and the irradiation tests.

Figure 5 shows the chip analogue gain and noise of the 640 pixel cells of a typical chip. The measured gain and noise are 66 mV/fC and $104 e^-$, respectively. The measured gain and noise values are in good agreement with the simulations. It should be mentioned that the measurements have been made without the detector and therefore an increase of the noise value in the final system is expected.

Figure 6 shows the Time over Threshold transfer function over the full input range. The circuit maintains a good linearity even for high input charges where the input preamplifier is saturated. The measurement has been obtained with a 5 nA discharge current on the preamplifier feedback circuit. The measured 232 ns/fC ToT gain is in good agreement with the simulated value of 202 ns/fC.

Figure 7 shows the Time over Threshold transfer function for lower charges, up to 6 fC. A good linearity can be achieved down to 0.6 fC, while for smaller charges a time compression is observed.

The baseline measurements showed an average value of 0.73 V with a σ of 5 mV. After the calibration procedure with the integrated DACs the σ is reduced to 0.65 mV.

Figure 6. Time over Threshold versus input charge — full range.

Figure 7. Time over Threshold versus input charge — up to 6 fC.

5 Conclusions

A CMOS 0.13 μm pixel prototype for the readout of the silicon pixel detector of the PANDA experiment has been presented. The ASIC provides spatial, time and energy information of the incoming particle. Energy measurement is obtained via the Time over Threshold technique. Test results prove the functionality of the chip and are in good agreement with the simulations. Tests with the detector and irradiation tests for both TID and SEU will be required before the production of a full scale ASIC.

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