The ATLAS IBL BOC Prototype Evaluation

**N. Schroer¹, M. Wensing⁶, G. Bruni², J. Joseph³, N. Krieger⁴, A. Kugel¹, P. Morettini⁵, M. Neumann⁶,
A. Polini², M. Rizzi², R. Travaglini², S. Zannoli², A. Zoccoli², M. Bruschi², I. Dantone²,
D. Falchieri², J. Dopke⁷, T. Flick⁶, A. Gabrielli², J. Grosse-Knetter⁴, T. Heim⁶**

¹ZITI-University of Heidelberg, ²University & INFN Bologna, ³LNBL Berkeley, ⁴University of Goettingen,
⁵INFN Genova, ⁶University of Wuppertal, ⁷CERN

Introduction

The ATLAS detector at the LHC at CERN will be upgraded in 2013 with an additional B-layer inserted into its existing Pixel Detector. For this IBL (insertable B-layer) new off-detector read-out electronics were designed and the prototype of the new back of crate (BOC) card will be presented here.

The purpose of the BOC is to interface between the front end electronics (FEE), the read-out driver (ROD) and the read-out system (ROS). Control and clock signals sent to the FEE need to be bi-phase mark (BPM) encoded and timed correctly to synchronize the detector readout. Data from the front-end is set into the right phase relation to be correlated to the corresponding event.

While the current BOC is implemented with custom made components to handle the synchronization, encoding and to establish the optical interfaces, the new IBL BOC is based on commercial off-the-shelf components and state of the art FPGAs which yields a highly flexible board.

Hardware

The main parts of the IBL BOC are the two Spartan6 LX150T FPGAs (BMF - BOC Main FPGA), each handling double the data throughput of a current BOC, hence four times in total. All the functionality formerly performed by custom made components is now integrated into these FPGAs. The necessary firmware is stored in non-volatile flash memories and is programmed by the third FPGA a Spartan6 LX75T. This so called Board Control FPGA (BCF) is also managing the communication with the ROD, handling the distribution of the read-out clock and has a Gigabit Ethernet interface. All three FPGAs have a 512Mb DDRII memory chip attached. To replace the custom made 12-channel optical plugins, SNAP12 modules have been chosen. They can handle all the data rates of the current (40/80 Mbps) and the IBL BOC (160 Mbps) and more (up to 3.5Gbps) if that is needed for future upgrades. The space consuming HOLA (High speed Optical Link for ATLAS) mezzanine card establishing the SLINK connection to the ROS was replaced by integrating the protocol logic into the FPGAs and by providing double the optical connections this option also supports the future Fast TracKer (FTK). Monitoring temperatures and humidity can be done with an ELMB (Embedded Local Monitoring Board) mezzanine card. Additional mezzanine connectors are available for both BMFs providing upgrade flexibility for the future. For testing and debugging a serial USB UART interface and multiple LEDs and pin header are available.

Picture of an IBL BOC from the second revision

Firmware

In the TX path 40Mbit/s input data is bi-phase-mark (BPM) encoded with an 80MHz clock. The output transitions at every, or every second rising edge of this clock if the input is high or low respectively. This implementation yields an output duty cycle close to 50% which reduces the need for correction. For the subsequent mark-to-space ratio (MSR) and delay adjustment chains of multiplexers provide a fine delay granularity of ~300ps. Additionally, registers can be used for coarse delay steps of e.g. 25ns depending on the applied clock frequency.

Clock data recovery (CDR) and synchronization of the RX data is done by a 4x oversampling and edge detection circuit utilizing the ISERDES blocks of the Spartan6 FPGA. The 8b10b decoding and parallelization is implemented in a standard straight forward way before the data is buffered in FIFOs and multiplexed via the VME connector to the ROD.

Configuration and control of the BOC is performed by a Microblaze core running on the BCF connecting to the Setup Bus via VME. Furthermore Ethernet and serial (USB connector) connections to the BCF are available.

Tests

The second revision of the IBL BOC prototype is available for testing, which is done in VME crates as well as on the table and includes connectivity tests with a redesigned ROD and readout tests with a DORIC (Digital Opto-Receiver Integrated Circuit) board and an FE-I4 single chip card.

The following has been tested and proper function verified:

Firmware blocks:

- TX path: BPM encoding and MSR correction (tested with DORIC)
- RX path: synchronization, 8b10b decoding, parallelization and the MUX
 - optical readout chain BOC → DORIC → FE-I4 → BOC tested with a digital scan
- integrated S-Link (simulation)

Hardware:

- programming of all FPGAs via JTAG / FLASH
- SNAP12, SFP and QSFP optical modules
- clock distribution on the BOC and to the ROD
- DDRII memory
- data transmission via VME backplane to/from ROD
- Ethernet works up to 100 Mb/s

Status & Summary

The second revision of the IBL BOC prototype has all the known issues from the first revision fixed and all tests could be performed successfully again. Functionality of the crucial hardware components have been verified and the development of necessary firmware blocks is well advanced and tests show promising results. Software for the MicroBlaze core is currently being developed and extensive system tests including all parts of the readout chain are ongoing.

For further information

Please contact nicolai.schroer@ziti.uni-heidelberg.de
or visit www.ziti.uni-heidelberg.de
More information on the ATLAS project can be obtained at www.atlas.ch
or more general at www.cern.ch