FTK: A Fast Track Trigger for ATLAS

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ABSTRACT: We describe the design and expected performance of a track trigger system for the ATLAS detector at the Large Hadron Collider. The Fast Track Trigger is a highly parallel hardware system designed to operate at the Level 1 trigger output rate. It is going to provide global tracks reconstructed in the inner detector with near offline resolution at the beginning of the Level 2 trigger processing. The system is based on associative memories for pattern recognition and fast FPGAs for track reconstruction.

KEYWORDS: Trigger detectors, Trigger concepts and systems, Trigger algorithms.

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1. FTK

The Fast Tracker (FTK) [1] is a trigger upgrade for the ATLAS detector at the Large Hadron Collider (LHC). As the LHC luminosity approaches its design luminosity of $10^{34}\text{cm}^2/\text{s}$ the combinatorial problem arising from charged particle tracking becomes increasingly difficult. The FTK is a highly-parallel hardware system intended to provide high-quality reconstruction of all tracks with transverse momentum above 1 GeV. Its speed and physics performance have been estimated at simulated luminosities up to $3 \times 10^{34}\text{cm}^2/\text{s}$, corresponding to 75 interactions per bunch crossing. An overview of the ATLAS detector and trigger system is given in the following section, followed by details of pattern recognition and track fitting.

1.1 The ATLAS Detector and Trigger

ATLAS is one of the two general-purpose detectors at the LHC [2]. It is designed to detect particles produced in proton-proton collisions at a center of mass energy of $\sqrt{s} = 14$ TeV. Particles are detected by the inner tracking detectors, electromagnetic and hadronic calorimeters, and a muon system. The inner tracker is inside a 2 T solenoidal magnetic field. From 2010 – 2011 ATLAS was recording 5.3 fb^{-1} of data with an energy of $\sqrt{s} = 7$ TeV. Peak luminosities of about $3.5 \times 10^{33}\text{cm}^2/\text{s}$ have been achieved. In 2012 the LHC energy is increased to $\sqrt{s} = 8$ TeV with peak luminosities exceeding $6 \times 10^{33}\text{cm}^2/\text{s}$. The inner detector consists of (in increasing distance from beam line) the Pixel detector, the Semiconductor Tracker (SCT) and the Transition Radiation Tracker (TRT). Pixel and SCT are used in the FTK system. The Pixel detector system contains 80 M channels of $50 \times 400\text{ }\mu\text{m}^2$ silicon pixels. These are arranged in three barrels at radii of 5, 9 and 12 cm with three disks on each side, between radii of 9 and 15 cm. Typically each track traverses three Pixel layers. The SCT system consists of 4 double layer of silicon strip detectors. Each double layer has

an axial- and a stereo layer with $80\ \mu\text{m}$ pitch. The entire SCT has 6M channels and is mounted on cylinders at radii of 30.0, 37.3, 44.7, and 52.0 cm. The end-cap modules are very similar in construction but use tapered strips aligned radially. The FTK uses all 3 Pixel and 4 SCT double layers mapped into 11 logical layers. Use of the insertable b-layer is anticipated, too. The rapidity coverage extends up to $|\eta| < 2.5$. Details regarding the inner detector is given in Ref. [2].

A three level trigger system [3] is used to select interesting events. The first level is hardware-based, operating at a maximum output rate of 100 kHz. It provides regions of interest, portions of the detector in azimuth and pseudorapidity, which caused the event to trigger. Level 2 and the Event Filter are realized as computing farms and are collectively known as the High Level Trigger (HLT). The HLT consists of several thousand CPUs. Level 2 operates within regions of interest with an output rate of 2 kHz, while the Event Filter has access to all information in the event, with an output rate of 200 Hz.

2. Physics with the FTK

There is a variety of physics applications for the FTK. One of the most prominent is the source of electroweak symmetry breaking which remains yet unknown. The easiest explanation, the Higgs mechanism [4, 5, 6], predicts the Higgs boson whose branching ratios to other particles are dependent on their masses. Therefore the production of heavy particles like b -quarks and τ leptons are of particular interest. These couplings can be modified by new physics and their measurement is a crucial test for the Standard Model. In Standard Model measurements the FTK helps to maintain high efficiencies while controlling background processes at high pile-up.

Figure 1, left, shows the isolated muon efficiency using the EM calorimeter isolation with two different cell energy thresholds. Criteria are set to achieve a $b\bar{b}$ rejection factor of 10. As the second plot of the same Fig. demonstrates, applying tracking isolation improves the efficiency and by only including tracks from the muon vertex, the efficiency is largely independent of the pile-up.

These examples demonstrate that tracking can play an important role in identification of interesting events while maintaining high efficiency. With increasing luminosity the use of tracking increases even more. The FTK will operate at the Level 1 trigger output rate, reconstructing all tracks at near-offline quality for use in the HLT. In addition this frees up CPU time in the HLT, which can be used for other purposes.

2.1 Simulated Performance

The FTK system has been simulated in software to determine its expected performance. FTK tracks are compared with tracks reconstructed using the ATLAS offline tracking algorithm. The resolution of track parameters is shown in Fig. 2 for tracks with $|\eta| < 1$, demonstrating that the FTK resolution is comparable to that of the offline tracking.

The FTK configuration uses pattern banks and constants suitable for up to 75 pile-up interactions. Figure 3 shows the efficiency of the FTK and offline algorithm to reconstruct muons of $p_T > 1\ \text{GeV}$. The efficiency drops for FTK tracks around pseudorapidity $\eta = 1$ are located at the transition region between barrel detector and forward disks. These have been addressed by relaxing the number of hits required in these particular regions.

Figure 1. Left: Isolated muon efficiency using the EM calorimeter isolation with two different cell energy thresholds as a function of the number of pile-up interactions, for a fixed $b\bar{b}$ rejection factor of 10. Right: Isolated muon efficiency using track isolation with and without a cut on the distance between the track and the muon at the beamline as a function of the number of pile-up interactions, for a fixed $b\bar{b}$ rejection factor of 10. Figures from Ref. [1].

Figure 2. Comparison of the helix parameters for Offline track reconstruction (black) and FTK (red). The track's transverse momentum is required to exceed 1 GeV and its pseudorapidity is limited to the central region ($|\eta| < 1$). A single muon sample is used. Figure from Ref. [1].

Figure 3. Comparison between single muon tracking efficiencies for FTK and offline algorithms vs. p_T (left) and η (right). Figures from Ref. [1].

The potential for heavy flavor identification (b -tagging) with the FTK tracks at high luminosities is evaluated using an algorithm based on the transverse impact parameter d_0 of tracks in jets. Template histograms of the impact parameter divided by its uncertainty are created for light jets and b jets. These are combined to form a likelihood. Figure 4 shows the expected performance for FTK and offline tracks. The simulated event samples are $WH \rightarrow b\bar{b}$.

Figure 4. Light-quark jet rejection vs b -quark jet efficiency for offline and FTK tracks at pile-up as expected for a luminosity of $\approx 3 \times 10^{34}$. Figure from Ref. [1].

3. Technical Design

3.1 Overview

The FTK is based on the experience of the Silicon Vertex Trigger at the CDF detector at Fermilab [7, 8]. The system is based on FPGAs and a highly-parallel Associative Memory (AM) chip [9]. The system is divided into eight core crates, each covering a 45° range in azimuth plus 10° overlap. Each core crate is further divided into four regions of η and two regions in ϕ . This yields 8 $\eta - \phi$ towers per crate and 64 trigger towers altogether. A $\eta - \phi$ tower is served by two processing units containing the AM chips for pattern recognition, Track Fitters (TF), Data Organizers (DO) to coordinate between pattern recognition and track fitting, and a Hit Warrior (HW) to remove duplicate tracks from the output. The processing units receive their inputs from Data Formatter (DF) boards

and pass their output to second stage boards which perform final full resolution track fitting and quality tests. Each of these components are described below. A sketch is given in Fig. 5.

Figure 5. Sketch of the FTK system [1].

Dual output front end links from the silicon detectors direct a duplicate set of the output to the Data Formatter boards which perform hit clustering and formatting of the data to be mapped to the 11 logical layers of the FTK architecture. Then it routes the clusters to the relevant processing units. In each processing unit the Data Organizer reduces the cluster resolution by a factor ≈ 10 into superstrips used for pattern recognition while storing the full resolution clusters for track fitting. The superstrips then are passed to the AM chips. Those operate in parallel to compare the incoming superstrips to approximately 100 million precomputed patterns per core crate. Matched patterns are sent back to the DO, which retrieves the full resolution hits and sends them to the Track Fitter. The TF does linear calculations of the helix parameters and χ^2 components using prestored constants and the location of the hit in each layer. Every combination of hits within a given pattern is fitted; those passing a fit-quality criteria are kept. The last stage of each processing unit is the Hit Warrior which removes duplicate tracks based on the number of shared hits between various tracks and the χ^2 of the fit.

3.2 Pattern Recognition and Track Fitting

Tracking is performed in two stages to keep the combinatorics at a manageable level. The first stage uses 8 out of 11 silicon layers for pattern recognition and track fitting while the second stage refits the tracks found in the first stage using all 11 layers. The first 8 layer stage uses 3 Pixel, 4 axial SCT and 1 stereo SCT layer. At least seven of eight layers are required to have a hit. The pattern matching takes place in CAM-based custom built AM chips, each containing 50k-100k patterns each. Hits entering the system are simultaneously compared to all stored patterns. The AM chips are grouped in sets of 32 chips on a local associative memory board (LAMB). Each AM board contains four LAMBs. Once all matched patterns, called roads, in an event are found the information is sent back to the DO. The DOs are located on an auxiliary (AUX) card attached to the AM board. Each AUX card has four instances of the Data Organizer, Track Fitter and Hit Warrior. Upon receiving the roads from a LAMB, the Data Organizer looks up the full resolution

hits within a road and sends them to the Track Fitter. The TF unit is expected to fit one track per nanosecond. This high rate is achieved by the large numbers of DSPs in the FPGA used to perform a simple linear fit for each set of N hit coordinates x_j :

$$p_i = \sum_j^N c_{ij} x_j + q_i \quad (3.1)$$

The p_i are the five helix parameters and the $N - 5$ χ^2 components, all of which are determined from the constants c_{ij} and q_j . If a fit is above a given χ^2 threshold and the candidate track has hits in all the detector layers, a majority recovery is performed. During this recovery the track is refitted several times, ignoring one of the hits each time to check whether a subset of hits will yield a good χ^2 . This allows a track to be recovered if one of the hits in the combination comes from noise or from a different track. The second stage of fitting uses the good tracks from the first stage to look for expected hits in the remaining 3 layers, using an inversion of Eq. 3.1. If at least 10 out of 11 hits are found, the track is refit with all of the hits and subjected to a final fit quality test.

3.3 Variable Resolution Patterns

One of the challenges in the design of the FTK is the large number of matched roads expected at $3 \times 10^{34} \text{cm}^2/\text{s}$. Although the system is already segmented into independently operating $\eta - \phi$ towers, the number of matched roads out of the AM could still be a challenge for the Data Organizer at very high instant luminosities and better pattern matching resolution could be necessary. Variable-resolution patterns have been developed to obtain better resolutions with equal AM bank sizes or the same resolution with much smaller banks [10]. Finer-resolution patterns lead to a lower fake rate at the cost of more required AM space, while coarse resolution maintains higher efficiency at the cost of increased combinatorics in the Track Fitter. The solution described here maintains a balance between these considerations. The logic of the AM chip design has been upgraded to include local subdivisions of each superstrip in a pattern.

The “don’t care” feature of modern CAMs is implemented so that the width of each pattern can be varied layer by layer. This allows the available hardware pattern space to be optimized to maximize efficiency while minimizing the number of random hits that have to be fit.

Simulation studying events with different pile-up conditions have been performed. A standard AM bank produces roughly the same number of roads of a variable resolution pattern bank that is 3-5 times smaller when using a single DC bit in the AM logic [10]. At the level of 70 pile-up, a fairly uniform 900-1300 clusters are expected per layer and tower.

4. Conclusion

The Fast Track Trigger for ATLAS will be able to increase efficiency and control background processes for particularly interesting events containing b quarks, τ leptons and isolated, high p_T electrons and muons. This is achieved by using global, high speed tracking at the beginning of the Level 2 trigger. The challenges given by increased combinatorics in track reconstruction with increasing luminosity and simultaneously greater need for computational power are solved by using precomputed AM based patterns and fast FPGAs in a highly parallel system.

A vertical slice test using collision data in summer 2012 is in preparation [11]. The dual output silicon detector front end cards needed are already installed in ATLAS. The full set of dual output cards for the final system is already produced. A data formatter prototype board is currently under design and will be ready by summer 2012. A prototype input mezzanine [12] is ready for the vertical slice test. The AM chip prototype (AMchip04) is expected by early summer 2012 and the design of the AM board (AMBFTK) is finished. An existing board (AMBslim5) [13] will be used for the vertical slice test. For the data organizer board a pre-prototype is available and will be used in high-speed testing. The second stage board which performs the full 11 layer fit is currently undergoing conceptual design and firmware development. We expect the system to be operational in the data taking period following the 2013-2014 shutdown.

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References

- [1] A. Andreani et al. The fasttracker real time processor and its impact on muon isolation, tau and b-jet online selections at atlas. *IEEE Trans. Nucl. Sci.*, 59:348–357, 2012.
- [2] The ATLAS Collaboration. The ATLAS experiment at the CERN large hadron collider. *JINST*, 3:S08003, 2008.
- [3] The ATLAS Collaboration. Expected performance of the atlas experiment - detector, trigger and physics. arXiv:0901.0512v4.
- [4] R. Brout F. Englert. Broken symmetry and the mass of gauge vector mesons. *Phys. Rev. Lett.*, 13:321, 1964.
- [5] P. Higgs. Broken symmetries and the masses of gauge bosons. *Phys. Rev. Lett.*, 13:508, 1964.
- [6] T. W. Kibble G. S. Guralnik, C. R. Hagen. Global conservation laws and massless particles. *Phys. Rev. Lett.*, 13:585, 1964.
- [7] J. Adelman et al. The silicon vertex trigger upgrade at CDF. *Nucl. Instr. and Meth. A*, 527:361, 2007.
- [8] A. Annovi et al. A vlsi processor for fast track finding based on content addressable memories. *IEEE Trans. Nucl. Sci.*, 53:2428, 2006.
- [9] L. Ristori M. Dell’Orso. A highly parallel algorithm for track finding. *Nucl. Instr. and Meth. A*, 278:436, 1989.
- [10] A. Annovi et al. A new variable-resolution associative memory for high energy physics. *Advancements in Nuclear Instrumentation Measurement Methods and their Applications (ANIMMA), 2011 2nd International Conference on Digital Object Identifier ANIMMA*, 2011. 10.1109/ANIMMA.2011.6172856.

- [11] A. Annovi et al. The edro board connected to the associative memory baby fasttracker processor for the atlas experiment. *2nd International Conference on Technology and Instrumentation in Particle Physics, Chicago, IL, USA, 9 - 14 Jun 2011*, 2011.
- [12] A. Annovi et al. A fast general-purpose clustering algorithm based on fpgas for high-throughput data processing. *Nucl.Instrum.Meth. A*, 617:254–257, 2010.
- [13] A. Annovi et al. Associative memory design for the fast tracker processor (ftk) at atlas. *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2011 IEEE*, page 141, 10 2011.