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THE FASTBUS CABLE SEGMENT

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Abstract

The Fastbus Cable Segment is a high speed parallel multidrop bus, which is operated with differential current drivers and differential line receivers. This paper describes the development leading to that scheme, the implementation and application results.

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Introduction

A Fastbus system [1] consists of multiple bus Segments. These Segments can be implemented as Backplane or Cable Segments. A fundamental property of Fastbus is the identical protocol on both, the Backplane and the Cable Segment.

In certain cases the Fastbus protocol permits or even requires the same signal being asserted simultaneously by several devices. Using this OR function, problems may arise, if the line is not driven properly. These problems are masked on short transmission lines, but do occur on long transmission lines. Primarily a line driving solution had to be found, keeping in mind the following requirements for the Cable Segment :

- independent and simultaneous assertion of the same signal by several devices must be possible,
- the drivers and receivers have to be operational within a reasonable common mode voltage range,
- the devices should not load the line in the powered down condition or if the power supply of a device fails,
- the maximum length, for which the Cable Segment still remains operational, should not be less than 30 m,
- one should be able to connect up to 32 devices to the Cable Segment.

Development

Twisted pairs, which can be mass terminated, have been chosen as transmission lines for the bus. The basic forms of transmitting digital data over these lines are the single ended or differential techniques using either voltage or current drivers.

Tests, which have been performed to evaluate their suitability for the Cable Segment, show the following [2] :

- Single ended voltage drivers, differential line receivers :

This scheme operates well, if only one driver is activated at any one time. The common mode range can be improved by referenced power supplies for the devices, which compensate for the ground potential differences between the devices [3].

When several devices are driving a line simultaneously (wired OR function) due to the low output impedance of the drivers multiple reflections occur before the drivers stabilize in a current sharing mode. If then a driver gates off its signal, thus takes away its contribution to the current sharing, glitches can be observed on the line. These "wired OR glitches" have a duration corresponding to another stabilization time, their amplitude depends on the ratio of the current sharing and may be such, that temporarily wrong levels can be observed on the line (Photo 1).

Driver A

Driver B

Line at A

Line at B

Photo 1 - Distance between Driver A and Driver B : 25m.

When Driver A is turned off, a "wired OR" glitch can be observed. The width of the glitch at A corresponds to the logic delay of Driver B plus twice the signal propagation delay between A and B.

(Horizontal scale = 200 ns/div)

(Vertical scale = 5 V /div, Driver A, B
= 0.5 V /div, Line A, B)

- Current driving (single ended, differential) :

The use of current drivers leads to current stacking if more than one device is driving the same signal, which may limit the application of this technique.

The 10194 (100194) [4,5] type is capable of transmitting and receiving full duplex signals on a bus line. The incorporated receiver part of this device operates single ended, which results in a low common mode voltage range.

The SH100250 is a differential full duplex transmitter/receiver device intended for point to point connections [6]. Splitting up the Cable Segment into a series of point to point connections and repeating the signals at each device is a way to perform the OR function, but the "power down" requirement can not be met [7].

With the 10192 driver [4] a differential scheme can be implemented. In this case in addition to the termination of the transmission line at both ends, active circuitry is required to compensate for the varying number of devices being attached to the line and to correctly bias the line for the receivers [8]. The 16 mA source current of this driver is not adjustable, if 10 drivers are turned on simultaneously their operational limit is reached.

Implementation

The first implementation of the Cable Segment was based on the 10192 tests. Two current driver types,

- a low current driver made of discrete components for the lines on which signals may be asserted simultaneously by several devices
 - the 10192 driver for all other lines
- and active circuitry at both terminations were used [9].

With the first four Segment Interconnect prototypes a 100 m multidrop has been established and successfully tested [10].

For widespread use the terminator was too complex and the power consumption too high. The discrete components low current driver design has been modified to reduce the power consumption, to increase the common mode range and to allow the use of a simple line termination. A thick film hybrid circuit, the "Quad Fastbus Cable Segment Driver", has been developed.

Figure 1 shows the implementation of the Cable Segment with one driver, one receiver and the two terminators.

The modified driver contains a current source, a matched current sink and a current switch controlled by the "Data Out" signal. The circuit is designed such, that in the quiescent state the source current I_s flows directly into the sink without effecting the current in the transmission line (source and sink are both connected to the "1" line of the pair). In its "ON" state the driver still sources the current I_s into the "1" line of the pair, but sinks this current now from the "0" line, which results in a differential voltage across the signal pair.

The value of the source current of the driver is set to 4 mA, which is sufficiently high to ensure that the voltage resulting from a single activated driver can be correctly sensed by the line receivers. On the other hand this current is sufficiently low to ensure that the differential voltage resulting from the current stacking of several active drivers does not exceed the operational limits of the devices.

The transmission line is terminated at both ends.

At one terminator the signal pair is connected to a bias voltage V_{term} , which allows the drivers and receivers to be operated around the center of their common mode voltage range.

The current source, which has been connected to one terminator, is biasing the lines such, that in the quiescent state the "0" line is more positive than the "1" line. This source current is set to a value, which is sufficiently high to ensure that the condition for the quiescent state can be met. The current also has to be sufficiently low to ensure that the signal resulting from a single activated driver can be correctly sensed.

Conclusions

The implemented scheme has been tested and meets the requirements, a differential multidrop bus can be established.

- Driver :

The difference between the source and sink current is less than 1 % (manufacturing specification). Source and sink current variations over the temperature range from + 20°C to + 75°C are less than 1.5 %. The matching of the currents remains within the 1 % tolerance over this temperature range. The common mode voltage range is ± 3.5 V. The typical propagation delay is 1.5 ns. In a powered down condition the drivers do not load the line. All measurements have been done with + 5 V and - 5.2 V, which are standard Fastbus supply voltages. The circuit has now become commercially available [11].

Receiver :

The receivers have not been incorporated into the hybrid circuit design, as the common mode voltage range of presently available standard ECL line receivers is smaller than the one of the drivers. The input current of the receivers should be below 50 μ A and approximately (tolerance 5 %) the same for both inputs.

Length :

The maximum length of the Cable Segment depends on various factors such as the quality of the cable, the number of devices attached to it, etc. We calculated it for a 110 Ohm, AWG 28 twisted pairs cable with 32 devices connected to it and obtained 40 m. In the calculations the wire resistance, the signal attenuation, the source-sink current mismatch, the bias current, the receiver input currents and worst case clustering have been taken into consideration [12].

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FIG.1: FASTBUS CABLE SEGMENT IMPLEMENTATION