Quality Assurance and Functionality Tests on Electrical Components during the ATLAS IBL Production

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The ATLAS Insertable B-Layer (IBL)
In 2013 a new beam pipe (39mm outer diameter) hosting a new layer of pixel sensors will be installed in the current ATLAS Pixel detector. For this IBL, two prototypes and 24 production staves will be produced. 14 out of the 24 staves will be mounted on the new beam pipe and form the IBL detector. Each stave will host 32 FE-I4B readout chips arranged in 12 double chips and 8 single chip modules. The active pixel region will be approximately 60cm long. Before mounting to staves the functionality of all single components has to be verified.

Module Reception Tests
The modules’ functionality will be tested after shipment from the production sites (Geneva and Bross) in the reception test main at Geneva University. By using the configuration files from the two production sites the direct comparison assesses the modules’ quality after transportation and before leading to the staves. In addition, particle properties will be investigated with the help of source scan measurements in the testing setup at CERN.

Stave Flex Tests
Stave flexes (two per stave) connect the modules to the PPO region (pew). During the various production steps all electrical connections have to be tested to assure that all modules can be powered and the communication can be established correctly. These preparation steps are:
- Reception from the production sites
- Banding of the dog leg (shaping of PPO region)
- Cleaning of the flexes
For each test the stave flexes are connected to the mechanical structure shown in Fig. 4. A Chris System TestCh 1 cable and harness tester is used to check the electrical connections.

IBL Production QA Stand
The ATLAS Insertable B-Layer (IBL)

Stave0 Reception Test - Electrical Tests
On 29th June 2012 the first real prototype stave for the IBL arrived in the CERN SR1 clean room. It is equipped with the foreseen sensor flavours bump bonded to FE-I4A chips. After connecting to the QA stand (see Fig. 3) some basic tests were performed to assure the stave’s quality after transportation and handling.

As soon as the mapping is verified the output data can be configured by the DAQ software and then send back an idle pattern. This 8b/10b pattern is function seen with the help of a differential probe on the debugging pins of the HSSI (High Speed IO) adapter cards (Fig. 5). From the amplitude and pattern in Figure 6(a) one can see that the LVDS signals of one chip are much lower than on the other chips (compare Fig. 9(b)). These eye patterns were measured while running a threshold scan. Thus, there is data on the signal but the idle pattern is still dominant between the frames. The LVDS levels can be adjusted by setting reference and offset registers in the FE-I4 chip configuration. Hence, this chip could be recovered and is now fully functional.

Module Characterisation on Stave Level
Fig. 12 shows a comparison of threshold and derived noise behaviour of the sensors. At Geneva University, the FE-I4B modules were powered by lab power supplies with very small cables. Whereas, at CERN the regulator boards are connected to the modules via longer cables.

Oscillogram and derived noise of Stave0 A side
Once the chips are tuned properly the particle detection properties can be investigated using two Am-241 sources which can be moved at a certain operating distance over the stave. Therefore, the 10cm long inner containers are mounted onto a linear motor which eventually can be controlled by the DAQ software. This enables automatic source scans. A first result of a 20min source scan can be seen in Fig. 13. Always four chips are covered by one source container. However, the dimensions of the sources themselves are a bit smaller. Hence, there are more entries in the occupancy plots in the middle of each 4-chip group, regions with a low number of entries, which is roughly the same for each chips, correspond to the SRD parts which are loaded into the module flex (see Fig. 2).

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References