Characterization of the FE-I4B pixel readout chip production run for the ATLAS Insertable B-layer upgrade

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Motivation for FE-I4

„Insertable B-Layer“

- Recover from eventual failures in present Pixel system, esp. B-Layer
- Ensure excellent tracking, vertexing and b-tagging performance during LHC phase I
- Add robustness to tracking with high luminosity pileup

Upgrade of outer layers for HL-LHC

- New pixel detector planned
- 2 removable internal layers radii about 3.5 – 10 cm
- 2-3 fixed outer layers radii about 15 – 25 cm
- Lower costs
- FE-I4 fits requirements for outer layers in terms of
  → Hit occupancy
  → Radiation hardness

→ Small radius: ~3.5 cm
→ Higher hit occupancy per pixel
→ Increased radiation damage
→ Need for low material to reduce multiple scattering
FE-I4 reminder

- 19 x 20 mm² → ~6 times size of FE-I3
- Pixel size 50 x 250 µm → FE-I3: 50 x 400 µm
- 26,880 pixels
- Organized in 336 rows and 40 double columns
- Readout organized in four pixel regions, hits buffered at pixel level until LV1-trigger → cope with high occupancies
List of Changes FE-I4A \(\rightarrow\) FE-I4B

- **FE-I4A**: prototype:
  - different pixel flavours
  - three powering options prototype
    - DCDC
    - Serial Powering
    - Direct powering
    - No internal reference voltage

- **FE-I4B**: experiment chip:
  - Uniform pixel matrix.
  - Provided different options for \(V_{\text{ref}}\) generation
    (see dedicated slide)
  - DC-DC charge pump removed

- Other fixes in FE-I4B:
  - Limited test charge injection
    \(\rightarrow\) Pulser Output impedance
    100K \(\rightarrow\) 40K
    \(\rightarrow\) Low leakage switches for \(C_{\text{inj}}\) selection
  - Selected DACs: Adjusted Slope, centered.
  - Reference current setting internal register \(\rightarrow\) wire bond pads
    (SEU safe)
Saturation in test charge injection circuitry observed in FE-I4A.
Test Pulse Injection Response

- Saturation in test charge injection circuitry observed in FE-I4A.
- Improved situation in FE-I4B.
  - Decreased output impedance, low leakage transistors for transmission gate switches.

**Injection Pulse in all injection modes**

**FE-I4A**

- Injection mode:
  - no Cinj, all DCs
  - single Cinj, all DCs
  - both Cinj, all DCs
  - no Cinj, 1/4 DCs
  - single Cinj, 1/4 DCs
  - both Cinj, 1/4 DCs
  - no Cinj, 1/8 DCs
  - single Cinj, 1/8 DCs
  - both Cinj, 1/8 DCs
  - no Cinj, single DC
  - single Cinj, single DC
  - both Cinj, single DC

**FE-I4B**

- Injection mode:
  - no Cinj, all DCs
  - single Cinj, all DCs
  - both Cinj, all DCs
  - no Cinj, 1/4 DCs
  - single Cinj, 1/4 DCs
  - both Cinj, 1/4 DCs
  - no Cinj, 1/8 DCs
  - single Cinj, 1/8 DCs
  - both Cinj, 1/8 DCs
  - no Cinj, single DC
  - single Cinj, single DC
  - both Cinj, single DC
Uniform Pixel Matrix

- **FE-I4A**:  
  - Pixel **prototype** flavours.  
    → Non uniform pixel matrix.  
  - Externally powered top row ESD rails (not accessible with sensor mounted).
Uniform Pixel Matrix

- **FE-I4A:**
  - Pixel *prototype* flavours.
  - Non uniform pixel matrix.
  - Externally powered top row ESD rails (not accessible with sensor mounted).

- **FE-I4B:**
  - Single pixel flavor chosen
  - Uniform pixel matrix.
  - ESD rails internally powered.
• IBL Half Stave consists of 6 double chip planar silicon sensor modules + 4 single chip 3D silicon sensor modules.
IBL Powering Scheme

Half Stave

- IBL Half Stave consists of 6 double chip planar silicon sensor modules + 4 single chip 3D silicon sensor modules.
- 4 Front End chips build one IBL power group.
• IBL Half Stave consists of 6 double chip planar silicon sensor modules + 4 single chip 3D silicon sensor modules.
• 4 Front End chips build one IBL power group.

• Each Front-End chip holds two on-chip LDOs for analog and digital supply voltage.
• In chip regulators in “partial shunt mode“:
  – LDO with additional minimum $I_{\text{in}}$.
    → Regulator consumes $I_{\text{min}}$ if $I_{\text{load}} < I_{\text{min}}$.
    → No additional power consumption when modules configured.
    → Transients lower than in pure LDO mode.
• Different reference voltage options integrated in FE-I4B.
Regulator Reference Voltage Options

• Regulator needs $V_{\text{ref}} = \frac{1}{2} V_{\text{out}}$.

• Two Options:
  - Bandgap reference.
  - Tuneable $V_{\text{ref}}$ from $I_{\text{ref}}$.
**V_{ref} Option Features**

**Bandgap Reference**
- $V_{ref}$ increases with dosis.
- Possible danger for FE, if analog regulator voltage constantly increases above 1.6 V

**Tuneable $V_{ref}$**
- Good tuning range if $I_{ref}$ is correct.
- $I_{ref}$ powered from analog regulator → Power up issues @ low temperatures.

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**LDO Test VrefBG + VrefTune**

**VDDA Power Up Test @ -40°C**
**IBL Powering Scheme**

- Tie together $V_{\text{ref tune}}$ and $V_{\text{refBG}}$ → two benefits:
  - Additional startup current → safe power up $I_{\text{ref}}$ at low temperatures.
  - The resulting reference is between the two initial references
    
    \[
    V_{\text{ref}} = \frac{2}{\left(\frac{1}{V_{\text{ref tune}}} + \frac{1}{V_{\text{refBG}}}\right)}
    \]
    
    → still tuneable and safe operation after heavy irradiation.

- Chosen powering scheme:
  - Tuneable and bandgap $V_{\text{ref}}$ tied together for analog regulator.
  - Tuneable reference voltage for digital regulator
    → Safe analog $V_{\text{ref}}$ at IBL end of lifetime dose.
    → Reliable power up at very low temperatures (tested down to -60 °C).
    → Keep possibility to adjust regulator output for both regulators.
Wafer Level Tests

- Current Consumptions
  - Several IC configurations
Wafer Level Tests

- Current Consumptions
  - Several IC configurations
  - Full digital activity
- IC calibration
  - Reference Current setting
  - Charge Calibration
    - Calibration voltage characteristics
    - Injection Capacitance

Current Consumption → Abort Probing

Global IC Cuts
Wafer Level Tests

- Current Consumptions
  - Several IC configurations
  - Full digital activity
- IC calibration
  - Reference Current setting
  - Charge Calibration
    - Calibration voltage characteristics
    - Injection Capacitance
- Digital readout logic
  - Data processing
  - Four pixel digital region
    - Latency counters
    - Hit Buffers
- Analog performance
  - Threshold / Noise Distribution
  - Injection delay circuitry
- Digital Periphery Blocks
  - Scan Chain Tests for all blocks
  - IDDQ tests on some wafers at Aptasic

\[ \text{[ZIVKOVIC]} \]
• Mean capacitance of 10 wafers: 6.0 fF. Simulated capacitance: 5.7 fF. (large uncertainty expected)
• All measurement results (6000 ICs) between 5.5 fF and 6.8 fF
Threshold / Noise Distribution

- Threshold not tuned on wafer
  → Large spread in mean threshold.

- Mean noise in good agreement with expectation.
Main „Yield killer“
24 FE-I4B wafers used for this plot

• ~ 8%: too high current: run gets aborted to protect probe needles.
• ~ 23%: Total Pixels Failing: IC fails if > 0.2% of all pixels show errors in any test.
30 out of 90 IBL wafers probed.

Preliminary Yield FE-I4B: \((60.7 \pm 2.3)\%\).
Summary

• IBL Frond-End electronics production run (FE-I4B) submitted October 2011
• Changes wrt. full scale prototype FE-I4A effective
• Detailed IC characterization on single IC level far advanced
• Production run wafer probing ongoing
  – Extensive wafer probing in Bonn (15,000 values per wafer)
  – Probing at Aptasic, some repetition, few more tests (Iddq)
    → See [ZIVKOVIC]
  – 31 wafers probed (28 unpatched, 3 patched)
  – Preliminary yield in expected range: 60.7 % green ICs
• Module assembly started, first flip chipped modules arrived
ESD problem + patched FE-I4B

• **Analog** regulator simplified ESD protection scheme.
ESD problem + patched FE-I4B

- Digital regulator simplified ESD protection scheme.
- High potential ESD rail floating → danger for pads connected to gate of transistor ($V_{\text{ref2}}$).
• Digital regulator simplified ESD protection scheme.
• High potential ESD rail floating → danger for pads connected to gate of transistor (V_{ref2}).
• „External“ (wire bond order) or „metal layer“ fix (FE-I4B_{patched}) provides full ESD protection.
Threshold Map Tuned

Threshold mod 0 chip 0

Threshold mod 0 chip 0

Noise mod 0 chip 0

Noise mod 0 chip 0

Constant 5510
Mean 3135
Sigma 36.49

Constant 3354
Mean 114.6
Sigma 9.234

"Channel" = row+336*column+26880*chip

"Channel" = row+336*column+26880*chip
- Best $I_{ref}$-DAC setting centered in FE-I4B.
- Tuned $I_{ref}$ between 1.95 µA and 2.05 µA.