An Upgraded ATLAS Central Trigger for 2014 LHC Luminosities

Michiru Kaneda (CERN)

On behalf of the ATLAS Level-1 Central Trigger Group

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The LHC and the ATLAS Detector

- **Multi-Purpose detector placed at one of the beam crossing points of the LHC**
- **The detector consists of:**
 - Inner Detectors within 2 T Solenoid Magnet
 - Calorimeters: Tile Scintillator and Liquid Argon
 - Muon System with Toroid Magnet
- **Status during 2012:**
 - The LHC runs at the center-of-mass energy of 8 TeV
 - Peak instantaneous luminosity: $7.7 \times 10^{33} \text{cm}^{-2}\text{s}^{-1}$
 - Integrated luminosity: 16fb^{-1} (~Oct)
- **Plan for 2014 (Phase-0 upgrade):**
 - The LHC will run at the center-of-mass energy of 13~14 TeV
 - Peak instantaneous luminosity: $\sim 1 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$

Implementation of the CTP

- **Components of the CTP**
 - **CTPIN** receives triggers inputs from sub-detectors, synchronizes and aligns them with respect to Bunch Crossing (BC), and routes them to the Pattern In Time (PIT) bus
 - **CTPCORE** receives PIT, generates L1A and sends event information to LVL2 and DAQ
 - **CTPOUT** fans out L1A and timing to Local Trigger Processors (LTP) in sub-detectors, receives, masks and monitors the BUSY signals from LTP
 - **CTPMON** receives PIT, and monitors total and bunch-wise rates
 - **CTPMI** is the interface for the timing signals
 - **CTPCAL** is for calibration requests from the detectors

The Central Trigger Processor

- **The ATLAS detector's trigger system consists of three distinct levels**
 - Level-1 (LVL1), Level-2 (LVL2) and Event Filter (EF)
- **L1 trigger is hardware trigger**
 - Inputs from sub-detectors are collected by the Central Trigger Processor (CTP)
- **The CTP Functionality**
 - Collect and combine trigger inputs
 - Make final decision of LVL1 (Level 1 Accept, L1A)
 - Receive the LHC timing
 - Mask for 8 Bunch Groups
 - Prescale triggers
 - Generate Dead time: Simple and Complex (Leaky Bucket)
 - Send L1A to Front-ends of sub-detectors for readout
 - Identify and send Region-of-Interest information to LVL2
 - Send readout data to Data Acquisition system (DAQ)
 - Monitor trigger, dead-time and busy signals
- **Requirements for LVL1**
 - The rate is reduced to a maximum of 75kHz
 - The maximum latency of LVL1 is $2.5 \mu\text{s}$
- **The CTP has worked very smoothly for the data during initial LHC run**
- **Primary motivation for upgrade:**
 - Increase the number of concurrent trigger inputs
 - Increase the number of concurrent trigger items

The CTP Upgrade Plan for 2014

Resource Upgrade

	Used	Available	Upgrade
CTPIN input cables (partially used)	9	12	
CTPIN input signals	212	372	
CTPIN integrating monitoring counters	138	768	1856
PIT bus lines	160	160	320
CTPCORE trigger items	241	256	512
CTPCORE bunch group masks	8	8	16
CTPCORE maximum number of AND terms	6	256	512
CTPCORE maximum number of bits OR in terms	6	12	15
CTPCORE per-bunch trigger item counters	12	12	256
CTPOUT cables to TTC partitions	20	20	25
CTPMON per-bunch monitoring counters	88	160	

- **New modules: CTPCORE++ and CTPOUT++ are being developed**
 - while same PIT bus backplane will be used with double rate
- **Double the number of trigger inputs: 160->320**
 - Multiplexing two inputs signals to one signal will be done on CTPIN
 - require extra ~2BC latency
- **Double trigger items: 256->512**
- **Double bunch groups: 8->16**
 - Mask will be applied after items are formed (it is a part of the trigger item)

- **Multiple trigger partitions (1->4)**
 - Use common trigger menu
 - each partition has own trigger mask and dead-time
 - Primary L1A Partition (L1Ap) provides LVL2 and DAQ readout
 - Other partitions are used for commissioning, calibration, etc.
- **64 electrical LVDS inputs for L1Topo trigger signals (CTPCORE++)**
- **Additional 12 optical inputs using ribbon-fiber receiver (CTPCORE++)**
- **Multiplexing of trigger signals (CTPOUT++)**

CTPCORE++ Trigger Path