**An Upgraded ATLAS Central Trigger for 2014 LHC Luminosities**

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*On behalf of the ATLAS Level-1 Central Trigger Group*

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**The LHC and the ATLAS Detector**

- Multi-Purpose detector placed at one of the beam crossing points of the LHC
- The detector consists of:
  - Inner Detectors within 2 T Solenoid Magnet
  - Calorimeters: Tile Scintillator and Liquid Argon
  - Muon System with Toroid Magnet
- Status during 2012:
  - The LHC runs at the center-of-mass energy of 8 TeV
  - Peak instantaneous luminosity: $7.7 \times 10^{33} \text{cm}^{-2} \text{s}^{-1}$
  - Integrated luminosity: 16 fb$^{-1}$
- Plan for 2014 (Phase-2 upgrade):
  - The LHC will run at the center-of-mass energy of 13–14 TeV
  - Peak instantaneous luminosity: $1 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$

**The Central Trigger Processor**

- **Components of the CTP**
  - CTPIN receives triggers inputs from sub-detectors, synchronizes and aligns them with respect to Bunch Crossing (BC), and routes them to the Pattern In Time (PIT) bus
  - CTPCORE receives PIT, generates L1A and sends event information to LVL2 DAQ
  - CTPOUT fans out L1A and timing to Local Trigger Processors (LTP) in sub-detectors, receives, masks and monitors the BUSY signals from LTP
  - CTPMON receives PIT, and monitors total and bunch-wise rates
  - CTPML is the interface for the timing signals
  - CTPCAL is for calibration requests from the detectors

**Implementation of the CTP**

**The CTP Upgrade Plan for 2014**

**Resource Upgrade**

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<thead>
<tr>
<th>Resource</th>
<th>Used</th>
<th>Available</th>
<th>Upgrade</th>
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<tr>
<td>CTPIN input cables (partially used)</td>
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<td>CTPCORE trigger items</td>
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<td>CTPCORE bunch group masks</td>
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<tr>
<td>CTPCORE maximum number of AND terms</td>
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<td>512</td>
</tr>
<tr>
<td>CTPCORE maximum number of bits OR in terms</td>
<td>6</td>
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<td>15</td>
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<tr>
<td>CTPR per-bunch trigger item counters</td>
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<td>CTPOUT cables to TTC partitions</td>
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<td>CTPMON per-bunch monitoring counters</td>
<td>98</td>
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- **New modules: CTPCORE++ and CTPOUT++ are being developed**
  - while same PIT bus backplane will be used with double rate
- **Double the number of trigger inputs: 160->320**
  - Multiplexing two inputs signals to one signal will be done on CTPIN
  - require extra ~32B latency
- **Double trigger items: 256->1256**
- **Double bunch groups: 8->16**
  - Mask will be applied after items are formed (it is a part of the trigger item)

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**CTPCORE++ Module**

- **CTPCORE++ Module**
  - in other FPGA
  - CTPCAL
  - PIT bus
  - Trigger & Timing signals
  - LVL2 inputs
  - CTPOUT signals (PIT, CAM, LVL2)
  - L1Ap

**CTPCORE++ Trigger Path**

- PIT (Pattern In Time)
- CTPR (Trigger item before Precal)
- L1Ap (L1A for physics partition)
- L1A (L1A for secondary partition)