ATLAS Level-1 Calorimeter Trigger Upgrade for Phase I

Weiming Qian

On behalf of ATLAS Level-1 Calorimeter Trigger group

Outline

- Current ATLAS Level-1 Calorimeter (L1Calo) Trigger
- Phase I upgrade (2018)
- eFEX architecture
- High Speed Demonstrator (HSD)
- PCB simulation
- HSD initial test results
- Summary

Current L1 Calo

- Sliding window algorithm
 - Counts over different thresholds
- 4 subsystems with 16 9U VME crates
- Low latency synchronous pipeline design
 - Over 7000 analogue channels from calorimeter
- Very successful operation since LHC start

L1 Calo phase I upgrade

- Motivation
 - For phase 1 (2018), LHC luminosity $\sim 2.5 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$
 - Total L1 trigger rate has to remain at $\leq 100\text{kHz}$
 - Trigger thresholds have to remain about the same to maintain physics sensitivity to electroweak processes
- Constraints
 - Phase I upgrade has to stay within current level-1 latency envelope $\sim 2.5\mu\text{s}$
 - Forward compatible with phase 2 upgrade (2022)
- Strategy
 - Using higher granularity trigger towers (digitised on detector), both laterally and in depth
 - Higher granularity should also improve energy resolution in presence of high pile-up
 - Initial physics simulation very promising, more simulation needed

EM trigger tower sums

➤ LAr calorimeter

New Rcore algorithm
Operates on middle layer

$$Rcore: \frac{\sum 2 \times 3}{\sum 2 \times 7} > a$$

$$\Delta\eta \times \Delta\phi = .025 \times .1$$

Option 1 (1141):
7 sums/tower

Option 2 (1441):
10 sums/tower

Back layer:
1 sum 0.1×0.1

Middle layer:
4 sums (0.025×0.1)

Strip layer:
1 sum (0.1×0.1) or
4 sums (0.025×0.1)

Presampler: 0.1×0.1

Baseline design

L1 Calo at Phase I

eFEX partitioning & link count

EM Calorimeter

eFEX modules

Core			Core + Env.		Fibre count (Merge in eta)		Fibre count (Merge in phi)		Total Fibre count	12-way fibre Ribbon count		
eta	phi	Proc	eta	phi	em	Had	em	Had		em	Had	Tot
3	64	192	6	64	192	64	156	48	204	13	4	17
5	32	160	8	35	140	35	112	40	147	10	3	13
10	16	160	13	19	114	38	104	39	143	9	4	13
12	16	192	15	19	114	38	120	45	152	10	4	14
16	10	160	19	13	104	39	114	38	143	9	4	13
25	8	200	28	11	132	44	140	56	176	11	4	15
50	4	200	50	7	140	49	150	50	189	12	5	17

Assumptions:

1. LAr trigger tower sum option 2: 1441
2. Links @6.4 Gbps
1 fibre carries 2.5 EM towers or 8 Had towers

Need to balance the fibre number vs. fibre mapping/data sharing complexity

eFEX module

➤ Characteristics

- 150~200 optical links for data input from LAr DPS
 - >50% shared between modules
 - >25% shared between FPGAs on the same module
- 6.4Gbps or higher line rate for each link
- MiniPOD/MicroPOD
 - 12-channel embedded optical transmitters/receivers
- 4 or more FPGAs for algorithm processing
- ATCA based
- MTP-CPI coplanar optical backplane connector
 - All optical input links via ATCA zone 3 area
- Built-in “ROD” and “RoI” merger functionalities
 - Additional dedicated FPGAs

Challenges

- Multi-Gbps data sharing with tight latency constraint
 - Serial link serialization/deserialization ~ 4 clock ticks
 - Minimize the number of stages of serial link in trigger path
 - Optical transceiver host board achievable trace length $\sim 20\text{cm}$
 - Electrical fan-out, if works, is limited within single module
 - MiniPOD/MicroPOD optical power budget $8\sim 10\text{dB}$
 - Optical splitting is limited to 1-to-2, very marginal
 - Data sharing between eFEX crates/modules
 - Serial link duplication at DPS, or/and
 - Passive optical splitting
 - Strong constraint on eFEX partition if used alone
 - Data sharing between FPGAs on the same eFEX module
 - Electrical fan-out, if works, or
 - Use GTX/GTH far-end PMA loopback
 - $\sim 14\text{ns}$ latency penalty

Challenges

➤ Density

- Zone 3 ~ 95mm
- MTP-CPI backplane connector width 22mm
- Maximum MTP-CPI connectors in zone 3
 - 4
- Maximum fibres in each MTP connector
 - 48, recommended by Avago
- Maximum fibre links via zone 3
 - 16 12-way fibre ribbons (192 fibres)
- For the simplest data-sharing
 - eFEX processing $3(\eta) \times 64(\Phi)$ towers
 - Needs 17 12-way fibre ribbons
 - eFEX processing $50(\eta) \times 4(\Phi)$ towers
 - Needs 17 12-way fibre ribbons

ATCA zone 3 cannot support the simplest data-sharing schemes.

Challenges

➤ High-speed PCB design

- Impedance control
 - PCB trace, via
- High frequency attenuation
 - Skin effect, dielectric loss
- Crosstalk
 - Near-end crosstalk (NEXT)
 - Far-end crosstalk (FEXT)
- Clock jitter
 - Synchronous vs. asynchronous link
- PCB differential skew
 - PCB material weave pattern
- Power distribution system
 - Nominal voltage +/- 2.5% for Xilinx Virtex-7 GTH

High Speed Demonstrator (HSD)

- Main Purpose
 - Multi-Gbps PCB design
 - PCB simulation
 - Correlation of PCB simulation and hardware
- Xilinx Virtex-6 FPGA
 - 24 GTX, 0.5~6.6Gbps
 - 24 GTH, 9.9~11.1Gbps
- Features
 - Two clock domains
 - Crystal vs. TTC clocks
 - Various trace lengths
 - Up to 50cm
 - Blind via technology
 - High-speed fan-out buffer
 - Local data-sharing
 - 12-way optical transceivers
 - Various link topologies via SMA

High Speed Demonstrator (HSD)

➤ Strategy

- Pre-layout simulation
 - Derive PCB layout rules
- Post-layout simulation
 - Verify PCB layout quality
- Time Domain Reflectometry /Transmission (TDR/TDT) test
 - Verify PCB manufacture quality
- Eye/BER (Bit Error Rate) test
 - Correlate PCB channel simulation to hardware

PCB simulation examples

- PCB material selection
 - 15cm PCB trace losses with different PCB materials
 - We choose PCB material with loss tangent of 0.01 for HSD

PCB simulation examples

➤ Crosstalk

- D/H: the most important parameter to control crosstalk
- Stripline crosstalk falls off much quicker than microstrip crosstalk

D/H	3	5	10
Microstrip NEXT	6.5%	2%	0.5%
Microstrip FEXT	10%	5.6%	1.7%
Stripline NEXT	1%	0.06%	0.0%
Stripline FEXT	0.1%	0.0%	0.0%

Actual crosstalk values will vary with different differential trace configurations.

PCB simulation examples

➤ PCB via design

Bad differential via example
Extracted from Virtex-7 Development board design
HyperLynx: Zdiff ~ 40Ω

- Increasing via anti-pad
- Shrinking via diameter
- Stripping off non-function pads
- Increasing via separation

Good differential via example
HperLynx: Zdiff ~ 70Ω

15cm + 4 bad vias @6Gbps

15cm + 4 good vias @6Gbps

PCB simulation examples

- Exploring achievable PCB channel length
 - Choose 3 different ranges for HSD pcb channel length for easy comparison between hardware and simulation

15cm w/o vias @6Gbps

30cm + 2 vias @6Gbps

50cm + 2 vias @6Gbps

Blue hexagon: SFP+ optical transmitter input tolerance eye mask

HSD Hardware

- Power DC-DC converters
 - ~10 power rails needed by FPGA
- IPMC
 - ATCA Low level hardware management
- Power + IPMC takes ~1/4 of ATCA board area
- Need to put IPMC on a daughter card to save PCB space

HSD initial tests

- TDR - Verifying PCB impedance
 - Impedance $\sim 110\Omega$, just on the edge of PCB impedance specification ($100\Omega \pm 10\%$)
 - Huge SMA reflection, due to excessive capacitance @ SMA launch, about 1 pf.
 - Need 3D fullwave EM solver to properly design SMA launch.

HSD initial tests

- TDT – Verifying PCB channel loss
 - Insertion loss SDD21 over 50cm differential trace
 - Tr of TDR scope is 35ps, measurement is accurate up to 10GHz

HSD initial tests

➤ TDT

- Compared to simulation, 7dB difference @5GHz, huge!

HSD initial tests

➤ TDT

- Simulation with extra SMA launch capacitance
- Very close to measurement up to 7GHz

HSD tests

➤ PCB Differential skew

- Goal: differential skew < 0.1 UI, for 10Gbps, that is 10ps
- 22 degree rotation of module relative to PCB panel helps
- Measured ~1ps skew over 50cm, excellent

Summary

- We have good understanding of the problems of the ATLAS Level-1 Calorimeter Trigger Upgrade for phase I.
- Precise system/module specifications will depend on further discussions between Level-1 trigger group and LAr group.
- A high-speed (6Gbps/10Gbps) demonstrator has been built to test new technology and to educate us in multi-Gbps PCB design.
- HSD initial tests showed some good results and uncovered some issues.
- High-speed PCB simulation has been integrated into PCB design flow and it has showed promising results in the diagnosis of HSD initial test issues.
- More detailed tests on HSD will be followed and the results will feed into phase I upgrade design.

BACKUP SLIDES

Data sharing between eFEX crates/modules

Type	Material	Trace Width (mm)	Loss Tangent	Copper Thickness (oz) see 1	Copper Thickness (μm)	Trace Length (mm)
Microstrip	FR4-6/8	0.3	0.022	1	35	200
	Nelco 4000-13	0.3	0.016	1	35	300
Stripline	FR4-6/8	0.125	0.022	0.5	17.5	150
	Nelco 4000-13	0.125	0.016	0.5	17.5	200

SFP+ 8/10Gbps optical transceiver host board achievable trace length, SFF8431 specification

Link duplication @ DPS

- Electrical fan-out, or
- FPGA GTX/GTH duplication

Optical splitting

Optical power budget for passive optical splitting

Based on Multi-Mode fibre optics (Parallel optics only available in Multi-mode currently)

- Insertion loss per MTP/LC connector: ~0.25dB
- Insertion loss of 2x splitter: ~ 4.0 dB
- Total insertion loss in the fibre channel: $0.25 \times 6 + 4.0 = 5.5$ dB
- Link penalties: 1dB
- Optical power margin: 2dB
- The optical power budget of optical transceivers should be > 8.5 dB

MiniPOD/MicroPOD optical transceiver power budget is 8dB(worst) to 10dB(average) based on tests @Fermilab, very marginal!

Electrical fan-out

The diagram illustrates the Far-end PMA loopback architecture, showing the flow of data and clock signals between the TX and RX sides of the PMA and PCS blocks.

TX Side (Top):

- TX PMA:** Receives data from the Channel Clocking Architecture. It includes TX OOB and PCIe Pre/Post Emp, TX Clock Dividers, and a PISO.
- TX PCS:** Receives data from the TX PMA. It includes PCIe Beacon, SATA OOB, Polarity, Phase Adjust FIFO, and a TX Gearbox.

RX Side (Bottom):

- RX PCS:** Receives data from the RX PMA. It includes RX PIPE Control, RX Status Control, RX Elastic Buffer, RX Gearbox, and an RX PMA interface.
- RX Serial Clock:** Receives data from the Channel Clocking Architecture. It includes RX EQ, DFE, RX OOB, RX Clock Dividers, and a S/P/O.

Far-end PMA loopback: A yellow box labeled "Far-end PMA loopback" is connected to the TX PCS and RX PCS blocks, indicating the loopback path.

Connections:

- Red arrows indicate the flow of data and clock signals.
- The TX PCS and RX PCS blocks are connected via a loopback path.
- The TX PCS and RX PCS blocks are connected via a loopback path.