The sROD Demonstrator for the ATLAS Tile Calorimeter Upgrade

Fernando Carrió Argos

Universidad de Valencia - CSIC, IFIC

On behalf of the ATLAS Tile Calorimeter
System

- Introduction
 - Present Tile Calorimeter
 - Tile Calorimeter Phase II Upgrade
 - Front-end Phase II Upgrade
- sROD demonstrator
 - Requirements
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- Status and Planning
- Summary

Present Tile Calorimeter

- Segmented calorimeter of steel plates and plastic scintillator tiles which covers the most central region of the ATLAS experiment at LHC (CERN)
 - 4 partitions: EBA, LBA, LBC, EBC
 - Each partition has 64 modules
 - One module hosts up to 48 photomultiplier tubes (PMTs)
 - Total number of readout channel is 9856
- Light produced by a charged particle passing through a plastic scintillating tile is transmitted to PMTs
 - Front-end electronics (on-detector)
 - Digitizes signals coming from PMTs
 - Placed in super-drawers (2 drawers)
 - Outermost section of the modules
 - Back-end electronics (off-detector)
 - Receives digital data coming from front-end
 - Main component is the Read Out Driver (ROD)
 - Reconstruction processing } L1 trigger
 - Data transmission

TileCal detector

ATLAS trigger system

TileCal Phase II Upgrade

- LHC increases luminosity in a factor of 10 by 2022: sLHC
- The TileCal Phase II Upgrade is focused on replacement of most of the readout electronics.
- The new readout architecture will provide:
 - Full digital Level-1 trigger
 - Higher reliability and robustness
 - Redundant data links to the off-detector electronics
 - On-detector electronics will send all data to off-detector electronics every beam crossing (40MHz)
 - Redundant power supplies
 - Higher radiation tolerance
- The Demonstrator Program for Phase 0 aims to test the new readout architecture:
 - Will be installed into detector at end of 2013 shutdown
 - Read out up to four adjacent drawers
 - Hybrid drawers compatible with the present system:
 - Complete new on-detector and off –detector electronics
 - Will provide both analog and digital trigger signals

TileCal Phase II Upgrade

- Present architecture system:

- Future architecture system:

	Present	Upgrade
Total BW	~ 165 Gbps	~20 Tbps
Nb fibers	256	8192
Fiber BW	640 Mbps	5 Gbps

Front-end Phase II Upgrade

- Front-End Boards (FEBs)
 - Modified 3-in-1 card (chosen for the Demonstrator project)
 - Enrico Fermi (University of Chicago)
 - QIE chip
 - Argonne National Laboratory and FermiLab
 - FATALIC ASIC
 - Clermont Ferrand (LPC)
- MainBoard (Stockholm University + Enrico Fermi UC)
 - Digitizes signals coming from 4 modified 3-in-1 cards
 - Readout of up to 12 PMTs
 - Sends digitized data to the DaughterBoard
 - Performs AD conversion of data and digital control of the FEBs
 - Maintains compatibility with other FEB alternatives
- DaughterBoard version 2(Stockholm University)
 - Data processing unit
 - Two Xilinx Kintex-7 FPGAs
 - High speed communication between on and off-detector electronics (sROD)
 - One QSFP+ connectors for the down link
 - One SNAP12 connector for data transmission to sROD

DB v1 plugged in a MainBoard with 2 modified 3-in-1 cards

FATALIC 2

QIE block diagram

DaughterBoard version 2

- Requirements for the sROD demonstrator

- Reception of data from new front-end electronics (48 PMTs)
 - 8 fibers x 5Gbps
- Data processing
 - Pipeline and derandomizer memories
 - Reconstruction algorithms
 - Data transmission
- Management and transmission to front-end electronics
 - Control and configuration of digitizer electronics
 - Control and communication with the high voltage power supplies
- L0/L1Calo trigger functionalities
 - Implementation of a preprocessor trigger
 - Data transmission to trigger system

New front-end architecture

sROD demo - Diagram

sROD demo - Mechanical

- AMC standard compliant
 - Double mid-size AMC (180.6mm x 148.5mm)
 - Can be plugged in a ATCA carrier or in a uTCA platform

Double mid-size AMC

sROD demo#1 →

sROD demo#2 →

ATCA carrier

ATCA test bench

- Processing Units:

- 1 Xilinx Virtex 7 FPGA
 - XC7VX485T-2FFG1558
 - 48 MGT@10Gbps
- 1 Xilinx Kintex 7 FPGA
 - XC7K480T-2FFG901
 - 24 MGT@10Gbps

- Memories (per FPGA):

- 1 GB Parallel flash memory
 - FPGA bitstreams
 - Linux images
- 512MB DDR3 SDRAM
 - Pipeline and derandomizer memories
 - Linux operating system + MicroBlaze

- Power supply unit

- Combination of linear regulators and switched regulators

- FMC board for expansion functionalities
 - Connected to both FPGAs
 - Auxiliary clock unit management
 - Test clock distribution schemas
 - Clock synthesizer/Jitter cleaner
 - Processing Unit
 - DSP / Processor
- Communications
 - USB interface
 - Ethernet port
 - UART port
 - Communication with ATCA CPU / other AMCs in the same carrier
- MMC mezzanine (DESY + CERN)
 - ATCA carrier power management
 - AMC Temperature monitoring

FPGA Mezzanine Card (FMC)

MMC

● Parallel Optics

- 4 x Avago RX MiniPODs (12 x 10Gbps)
 - Receive data from new front-end electronics
 - 8 x 5Gbps
- 2 x Avago TX MiniPOD
 - Communication with the trigger system
 - Control and configuration of the front-end electronics
- 1 x SFP connector
 - Transmit data to present architecture
- 1 x Modified Luxtera QSFP+ module
 - Data reception from front-end electronics with “QSFP+ version”
 - 4 x 10 Gbps

Luxtera optical modulator

MiniPODs

sROD demo - Prelayout

sROD demo - ATCA

- ATCA test bench at IFIC laboratories (Valencia)
 - Complete system from Radisys
 - Fully operative
- SYS6006 Platform
 - 6 slots chasis
 - Dual star topology
 - One Switch – communication between ATCA blades
 - Shelf management module
- ATCA-1200 Carrier
 - 4 single/2 double AMC
 - Power distribution
 - High-speed communication with RTM
 - High-speed communication other ATCA modules
 - High-speed communication between AMCs
- A1200 RTM
 - 4 SFP optical modules per AMC (Total of 16 SFPs)
 - Connection to ATCA-1200 by zone 3 connector
- ATCA 4500
 - Compute Processing module with RTM

ATCA
test bench

VME crate

sROD demo - Status & Planning

- Schematics almost done!
 - Cadence FPGA System Planner 16.5 + Xilinx PlanAhead 14.2
 - Pin placement optimization
 - Cadence Design Entry CIS 16.5
 - Schematic design
- Layout design
 - Cadence PCB Editor 16.5
 - 16 layers (estimated)
- Signal/Power integrity studies
 - AnsoftLinks 6.0
 - Ansoft Siwave 5.0
- First prototype by January/February 2013

Cadence FPGA System Planner

- Off-electronics redesign is needed for the TileCal Phase II Upgrade
 - Installation of one sROD demo into the detector by 2014 (Demonstrator project)
- sROD demonstrator board
 - Double mid-size AMC board
 - Plugged in a Radisys ATCA-1200 carrier
 - Capable of receiving and processing data from one new drawer (48 PMTs)
 - Management and transmission to front-end electronics
 - L0/L1 Calo trigger preprocessor functionalities
 - Status:
 - Schematics almost done
 - Main components already order
 - Avago MiniPODs modules
 - Virtex 7 and Kintex 7 FPGAs
 - First prototype by January/February 2012

Back-up slides

Future architecture

Previous work

- RX and TX SNAP12 connectors – GBT protocol
 - 75 Gbps RX
 - 75Gbps TX
- Altera Stratix II GX

Optical Link Card