CERN-EP/83-191
12 December 1983

A MICROPROCESSOR-CONTROLLED READOUT SYSTEM
FOR IMAGING DRIFT CHAMBERS

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ABSTRACT

A multihit compact readout system for drift chambers is described. This system records the drift time, the charge division, and the energy loss for up to 16 hits per wire, giving a three-dimensional representation of multitrack events. A total of 1000 channels are used to read the imaging drift chambers in the forward arms in the UA1 apparatus at the CERN proton-antiproton Collider.

(Submitted to Nuclear Instruments and Methods
in Physics Research)

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1. INTRODUCTION

During the last years high-energy physicists have designed and built large and sophisticated multiwire detectors to extract information on the trajectory and the velocity of charged particles that is as complete as possible. These detectors, usually called pictorial or imaging drift chambers, are coupled to readout systems which provide a digitized three-dimensional representation of the final states that originated in high-energy particle collisions.

Here we present a compact readout system [1] designed in connection with the imaging drift chambers which equip the forward arms in the UA1 apparatus [2] at the CERN proton-antiproton Collider. In these chambers the space points along the particle trajectory are reconstructed by measuring the drift time and the charge division along the wire. The readout system records the drift time, the charge division, and the total charge collected on the wires for up to 16 hits per wire.

The basic unit is a five-station-wide CAMAC module, called a multihit flash digitizer (MHFD), which consists of a mother board (MB) supporting and carrying the bus lines for: i) 24 data memory (DM) cards; ii) two readout cards (RO1 and RO2); and iii) one clock (CK) card. The MHFD module encodes the information from 24 wires, stores it into memories, and transfers it to the dataway under standard CAMAC commands. Four such modules are housed in one CAMAC crate. As part of the system, a two-station-wide CAMAC module contains a control processor, linked to each of the four MHFD modules, which surveys the operational stability of all DM cards. One crate, served by a controller which satisfies the standard CAMAC specifications, is an autonomous readout system for 96 wires.

2. THE MULTIHIT FLASH DIGITIZER MODULE

The mechanics of the MHFD module are shown in fig. 1. The front panel supports four round connectors at which the pulses from the preamplifiers mounted on the chambers arrive via multiple, singly shielded, twisted-pair cables. These connectors are linked to the mother board with small 50 Ω coaxial cables. The MB is a multiple (five)-layer printed circuit carrying the power and bus lines for all the

other cards, which are supported with multipin connectors; it is powered via three dataway CAMAC connectors in parallel. The power consumption is about 300 W per module.

3. THE DATA-MEMORY CARD

The drift time, the charge division, and the total charge collected on one wire are digitized and stored into memories by the DM card (fig. 2) for up to 16 samples. For the charge division and total charge digitization, 6-bit, 50 MHz, ECL flash analog-to-digital converters (FADCs) (*) are used.

The block diagram of a DM card is shown in fig. 3. The left (L) and right (R) bipolar pulses from the preamplifiers arrive at two input differential amplifiers with gain $\times 2$, whose outputs are summed together and sent to the discriminator and, independently, also to two integration stages. The function of the integration stages is to measure the charges of the left and right pulses and to convert them into pulse amplitudes which are digitized by the FADCs. The time integration of the current from the left and right sides of the wire is realized by integrating the pulses with a large time constant, splitting each integrated pulse into two parts, delaying and attenuating one part, and then adding them together again

in a differential amplifier. The integration time, determined by a large-bandwidth delay line, is about 60 ns, and the over-all voltage gain of the integration stage is about 5. An instantaneous current of unit charge is thus converted into a pulse of 60 ns width and unit amplitude. In general the amplitude $Q(t)$ is proportional to the charge collected during 60 ns before the time t . The attenuation compensates for the fact that the integration time constant is not infinity and avoids the presence of overshoot at the output of the integration stage. The left and right integrated pulses, Q_L and Q_R , are then sent to the charge division FADC and summed together to obtain the total charge Q , which is encoded by a second FADC. In between the integration stage and the FADCs a baseline restorer ensures the short time stability of the d.c. levels at the inputs of the FADCs in case of heavy duty

*) Siemens type SDA 6020, Siemens, Munich, Fed. Rep. Germany.

cycles. The FADC inputs are protected against pulses exceeding the specified maximum difference of 3 V between the FADC reference levels. In the application foreseen for this readout system, this value corresponds to about ten times the minimum ionization.

Figure 4 shows how the integrated pulses, Q_L and Q_R , are connected to the FADCs in order to extract the charge division and the total charge information. Given the response function of a 6-bit FADC, defined as

$$N = 63(V_{IN} - V_{RB})/(V_{RT} - V_{RB}) , \quad (1)$$

where V_{RT} and V_{RB} are the "top" and "bottom" FADC reference voltages, the encoded charge division is simply related to the z coordinate along the wire by

$$z = \text{wire length} \times Q_L/(Q_L + Q_R) . \quad (2)$$

With the FADC reference voltages as in fig. 4,

$$V_{RT} = V_{RT}^0 + Q_R; \quad V_{IN} = V_{IN}^0; \quad V_{RB} = V_{RB}^0 - Q_L ,$$

the charge division response is

$$N_{\text{ch div}} = 63 \frac{(V_{IN}^0 - V_{RB}^0) + Q_L}{(V_{RT}^0 - V_{RB}^0) + Q_L + Q_R} .$$

The subtraction of the d.c. offsets is automatically done by the control processor which, by comparing the levels read on the three FADC inputs, ensures that

$$V_{RT}^0 = V_{IN}^0 = V_{RB}^0, \text{ i.e. } N_{\text{ch div}}/63 = z/(\text{wire length}) .$$

Relation (2) is rigorously valid only if one can neglect both the preamplifier input impedance with respect to the wire resistance, and the dynamical impedance seen from the charge division FADC reference inputs with respect to the FADC internal resistor chain (see fig. 4). To compensate for these effects, a small fraction of the left-charge pulse Q_L is subtracted from the right-charge pulse Q_R and vice versa. Since the charge pulses have different polarities, this compensation is simply realized with a suitable resistance in parallel.

In order to expand the dynamic range of the total charge measurement dE/dx , and to include the tails of the Landau distribution, the second FADC is operated in a non-linear mode by feeding a fraction of the input pulse $-Q$ into one of the reference inputs [3,4]. In this way the dynamic range is stretched over several times the minimum ionization at the expense of a loss of resolution at large pulse heights. From the circuit layout sketched in fig. 4, the response function is

$$N \frac{dE}{dx} = 63 \frac{V_1 - (Q - V_0^{NI})}{V_1 + \alpha(Q - V_0^{NI})} \quad (4)$$

where $V_1 = -6 V$, V_0^{NI} corresponds to the minimum digitized charge, and $\alpha = R_2/R_1$ is about 18. The d.c. offset V_0^{NI} is monitored by the control processor. The dE/dx FADC response function and the relative resolution $\delta V/V$ are plotted in fig. 5 as a function of the input pulse height V for an input pulse width of 80 ns. The response function is well fitted by a simple exponential.

The conversion of the FADCs is strobed by the discriminator via the strobe circuit (see fig. 3). The output of the discriminator, when in coincidence with the external gate, is fed back into a NOR via a delay line, and originates a pulse train of period $2 \times DL$, where DL is the delay-line length. The pulse-train width is determined by the time over threshold of the discriminator input pulse. Thus the strobe pulse allows $n + 1$ samples of charge division and total charge for pulse over threshold width larger than $2 \times n \times DL$. The delay line has 10 ns pick-off points so that the strobe circuit period can be chosen in steps of 20 ns according to specific applications. Of course it is not worth making it shorter than the integration time. A period of 60 ns corresponds to a "continuous sampling" read-out.

The same circuit strobes a 10-bit latch which receives the clock lines, thus associating the corresponding time information with each charge division and total charge sample. The strobe pulse increases a counter and shifts the encoded information into 16-step random access memories (RAMs). The circuit is locked off as soon as the 16th hit is recorded by the counter. In this case an overflow flag is set in one of the RAM locations.

All information, drift time, charge division, and dE/dx sampled during the time over threshold of the discriminator is encoded in real time. The DM cards are gated on for a period of about 3.6 μs , corresponding to the maximum drift time of the chambers, and at the end of the gate the information is digitized in the RAMs and is ready to be read out.

The DM card requires a careful and continuous control of the d.c. levels which define the response of the FADCs and the discriminator threshold. The control is realized through few points on the DM card, whose levels can be either read out or set by the control processor via an analog multiplexer (see Section 6).

4. THE CLOCK CARD

The CK card generates a 10-bit Gray-encoded clock with a least significant bit (LSB) of 4 ns. The clock, generated with a coaxial delay line, is triggered by the external gate START, and then encoded by a counter and a series of exclusive ORs into Gray code bits which are distributed to the DM cards via bus lines printed on the mother board. The Gray code allows a 4 ns LBS resolution, with the fastest frequency on the MB transmission lines being 62.5 MHz. The main components of the CK card are ECL 100,000 integrated circuits, voltage and temperature compensated, ensuring a frequency stability of better than 10^{-3} .

Although this readout system has been designed in connection with a bunched colliding beam machine, options are foreseen for use in fixed-target and in d.c. operated, colliding-beam experiments as well. At the CERN $p\bar{p}$ Collider the external gate, START, is synchronized with the SPS bunch-crossing signal, and its width is longer than the maximum drift time and shorter than the bunch-crossing period of 3.9 μs . The gated clock is cleared off in case of no trigger from the experiment. For applications in fixed-target experiments, the external gate will run in continuous mode and the delayed trigger, STOP, will be recorded on any of the DM cards. In this case only 15 hits are available for the chamber pulses.

5. THE READOUT CARDS

As mentioned before, the readout part is organized with two cards: R01 and R02.

The R01 card receives commands from both the DM cards and the R02 card and organizes, with priority encoders, the order of the data transmission from the DM cards' RAMs to the R02 card. At any Read command it scans through all the DM cards; empty cards (no hit recorded by the counter) are skipped. If hits are recorded, the counter is decreased and the data are transferred to the R02 card in decreasing drift-time order. When the counter is set to zero, R01 will pass to the next DM card.

The R02 card contains the logic for the CAMAC functions; it formats the data extracted from the DM cards and sends them out to the CAMAC dataway. The data for each hit are encoded in two 16-bit words containing two word identifiers, the overflow flag, the module (2 bits) and the wire identifier (5 bits), the charge division (6 bits), the total charge (6 bits), and the drift-time information (10 bits).

The readout time is 2 μ s per recorded hit.

6. THE CONTROL PROCESSOR

The task of the control processor is to monitor the operational stability of the DM cards continuously and to correct for variations of the FADCs' reference levels. The control is done by acting on eight points on each DM card (see Table 1). The control processor module is subdivided into two cards: i) the readout autonomous controller (RAC), and ii) the general-purpose microprocessor controller (GPMC).

A block diagram of the RAC is shown in fig. 6. The internal clock cycles continuously over the Read and Write addresses of the 96 DM cards' analog multiplexers. For each point the level is either read out via an 8-bit ADC and loaded into the 1 Kbyte memory or updated in the Sample and Hold with the value stored in the memory via an 8-bit DAC, the operation being addressed by the SELECT lines.

The cycle can be interrupted by the GPMC, which then has access to the data stored in the RAC memory. The GPMC is programmed to minimize the charge division FADC pedestals, and to equalize the dE/dx FADC pedestals and the discriminator thresholds for all DM cards. The sensitivity can be varied over a wide range and has been set to about 1 mV per count.

The RAC can operate in two different modes following the instructions from the GPMC: i) in short-cycle mode it will only Write and will thus keep the levels constant; ii) in long-cycle mode it will Read and Write, and thus the GPMC program will correct for fluctuations of the d.c. offsets. The time required by the RAC to cycle over all points on the 96 DM cards is 2.9 ms for the short cycle and 5.8 ms for the long cycle.

The GPMC has been described in detail elsewhere [5]. It comprises: a 6800 microprocessor^{*)}; 8 to 16 Kbytes of erasable programmable Read Only memory (EPROM); 2 Kbytes of random access memory (RAM); a CAMAC Input/Output port; an RS232 serial interface; an advanced data-link controller (ADLC) [6]; and a port for controlling the RAC. A resident monitor, located in 8 Kbytes of EPROM, can process alphanumeric commands addressed either from the RS232 terminal port or from the CAMAC dataway. The commands allow reading, loading, and histogramming of the contents of the RAC memory. Special commands devoted to the automatic tuning of the DM card parameters are located in 4 Kbytes of EPROM. The resident monitor operates as a background program waiting for instructions from the RS232 or from the CAMAC port. A foreground program, driven by the ADLC port, is active on interrupt, allowing the control of several GPMCs via a single ADLC master station located in the SUPERCARIAR processor [7]. The 2 Kbytes of RAM contain a table of the RAC, ADC, and DAC values, and the required setting for the discriminator threshold and the dE/dx pedestal for all DM cards.

Although there is no direct communication between the GPMCs and the MHFDs data-stream flowing in the CAMAC branch, the SUPERCARIAR processor can survey the data

*) Motorola, M6800 Application Manual, 1975.

of both GPMCs, via the ADLC port, and the MHPDs via a router connected to the CAMAC branch [8]. In this way a single program, resident in SUPERCAVIAR, can diagnose faults in the parameter setting of the DM cards.

7. AN APPLICATION

To fully exploit its multihit capability, this readout system has been tested with a large-cell drift chamber which reconstructs the transverse profile of high-energy electromagnetic showers. The chamber [9] consists of two 15 cm long drift cells in which the electric field drives the ionization electrons towards two central rows of five anode wires alternated with five cathode wires. The wires are 50 cm long, so that the sensitive area of the detector is $30 \times 50 \text{ cm}^2$. The distance between the anode wires is 10 mm.

The chamber was exposed to a high-energy electron beam and was placed after about 6 radiation lengths of lead. With a gas mixture of 40% argon + 60% ethane, and an electric field of 1.3 kV/cm, the drift velocity was 0.053 mm/ns. The anode wire voltage setting was such that the multiplication factor was about 2×10^3 in order to ensure a proportional mode operation over a large energy range.

For this test the minimum time distance between two consecutive hits, determined by the strobe circuit delay line, was set to 160 ns, so that the shower profile was measured by sampling the ionization density every 8.5 mm. Figure 7 shows the profiles of a 30 GeV shower measured on the five consecutive wire planes with the beam illuminating the upper drift cell. The vertical coordinate is obtained by drift time, and the horizontal coordinate by charge division along the wires: each sample is represented in the figure by a rectangle centred on the measured coordinates and with an area proportional to the dE/dx FADC response uncorrected for the non-linearity. The centre of gravity of the ionization density is obtained on each wire plane with a resolution of about 3 mm and 8 mm in the drift time and charge division projection, respectively, for a 30 GeV electromagnetic shower varying roughly as $1/\sqrt{E}$.

Acknowledgements

We would like to thank C. Ghesquière and G. Salvini for their continuous and enthusiastic support, S. Lazic for the drawings of the printed circuits, D. Berthet and A. Gandi and the staff of the Printed-Circuit Workshop at CERN for their patient assistance, and G. Lunadei for the test of the cards. The realization of this project was possible thanks to the skilful co-operation of the Electronics Workshop of the INFN, Sezione di Roma, and to the help and advice of many of our colleagues of the UA1 Collaboration.

Point		Action					
Charge division FADC V_0^{RT} (right pedestal)	"	"	"	"	"	"	Read
	"	"	"	"	"	"	Write
	"	"	"	"	"	"	Read
	"	"	"	"	"	"	Read
	"	"	"	"	"	"	Read
Total charge FADC V_0^{IN} (pedestal)	"	"	"	"	"	"	Read
	"	"	"	"	"	"	Write
	"	"	"	"	"	"	Read
	"	"	"	"	"	"	Read
	"	"	"	"	"	"	Write
Discriminator threshold setting		"	"	"	"	"	Write

Table 1

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Figure captions

Fig. 1 : The multihit flash digitizer module.

Fig. 2 : The data memory card.

Fig. 3 : Block diagram of the data memory card.

Fig. 4 : Schema of the control of the FADCs' reference levels.

Fig. 5 : Response function (left scale) and relative resolution (right scale) of the dE/dx FADC as a function of the pulse height at the input of the data memory card.

Fig. 6 : Block diagram of the readout autonomous controller.

Fig. 7 : Transverse profile of a 30 GeV electromagnetic shower, after 6 radiation lengths of lead, measured on five consecutive wires in a drift chamber. The chamber dimensions are 30 cm vertical and 50 cm horizontal. Each ionization sample is represented by a rectangle centred on the measured drift time (vertical) and charge division (horizontal) coordinates with an area proportional to the dE/dx FADC response (uncorrected for the non-linearity).

Fig. 1

Fig. 2

Fig. 3

Fig. 6

Fig. 7