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WIT2012 — WORKSHOP ON INTELLIGENT TRACKERS,
3–5 MAY 2012,
INFN PISA, ITALY

A hybrid module architecture for a prompt momentum discriminating tracker at HL-LHC

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ABSTRACT: The capability of performing quick recognition of particles with high transverse momentum (more than a few GeV/c) in the inner tracker is deemed essential to keep the CMS trigger rate at an acceptable level at a higher luminosity LHC ($L > 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$). We present an architecture for a novel tracking module based on a combination of a pixelated sensor with a short strip sensor that would offer such capability. The critical aspects of the design such as the projected power consumption, the resulting material budget, and the data flow model are discussed and estimates are given. It is also shown that a manufacturable module of this type is well within the capabilities of currently available microelectronic and packaging-assembly technologies.

KEYWORDS: Trigger concepts and systems (hardware and software); Electronic detector readout concepts (solid-state); Particle tracking detectors (Solid-state detectors); Data reduction methods

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1 The CMS tracker at the high-luminosity LHC

After the upgrade of the accelerator complex foreseen for the beginning of the next decade, the LHC is expected to produce an instantaneous luminosity of $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, that will be sustained for a large fraction of each fill through luminosity levelling (“High-Luminosity LHC”, or “HL-LHC”). The quoted luminosity corresponds to more than 100 pileup events per bunch crossing if the operating frequency is 40 MHz.¹ For such scenario, CMS will eventually collect up to 3000 fb^{-1} , after several years of operation, and its tracking system will have to be improved in terms of radiation resistance, readout granularity and ability to contribute information to the Level-1 trigger. The whole tracker will have to be replaced at the beginning of the next decade: this upgrade will involve the outer strip tracker, as well as a further upgrade of the inner pixel detector.²

The implementation of the trigger functionality has been studied thus far in the context of the outer tracker upgrade; this paper illustrates the concept for a detector module providing information for the Level-1 processing, with local rejection of signals from low-momentum particles.

1.1 Requirements for the outer tracker upgrade

The upgraded tracker will have to provide improved tracking performance in a more challenging environment, while producing at the same time fast information for the Level-1 trigger. The basic requirements can be summarized as follows:

¹The number of pileup events would be larger than 200 if the same luminosity was achieved with 20 MHz operation, which represents a much more demanding condition for the detectors.

²A first upgrade of the pixel detector is planned for the middle of this decade (“phase-1 upgrade”). The new detector will provide on average one more spatial point measurement per track compared to the present system, with a substantial reduction of material in the tracking volume, as well as enhanced robustness at high rate.

- (i) Robust tracking in operation with up to $200 \div 250$ collisions per bunch crossing in the worst-case scenario of 20 MHz operation (to be compared to the original LHC design figure of 20 collisions per crossing); this can be achieved by maintaining the occupancy at the level of a few percent, which requires increased granularity.
- (ii) Ability to provide satisfactory performance up to an integrated luminosity of about 3000 fb^{-1} , to be compared with the original figure of 500 fb^{-1} ; this requires the selection of more radiation hard silicon sensor material, especially for the innermost regions, as well as more stringent criteria in the qualification of electronics and mechanical assemblies.
- (iii) Reduced material in the tracking volume; the material is the most severe limitation on the performance of the present tracker [1], and it is dominated by electronics and services (notably in the region between barrel and end-cap).
- (iv) Ability to contribute information to the Level-1 trigger decision, in order to hold the overall rate below 100 kHz, without compromising the physics performance of CMS. The trigger requirement is discussed in more detail below.

1.2 Tracking information at Level-1

The event filtering at Level-1 becomes substantially more challenging at HL-LHC, not only because the rate of events passing a given selection scales with the instantaneous luminosity, but also because the performance of selection algorithms degrades with increasing pile-up.

For example, the single muon Level-1 rate has an irreducible tail due to poorly measured tracks that are compatible with straight trajectories, and are therefore not removed even by increasing the p_T threshold: such an effect is aggravated at high luminosity by accidental coincidences. In the High-Level Trigger, where the information from the tracker is also added, the reconstruction is substantially improved and the rate of muon candidates follows closely the generator rate (see also [2]). Some improvements are expected with the “Phase-1” trigger upgrade, which will yield an acceptable rate for luminosities up to about $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, but the rate will saturate again the available quota for higher luminosities. Hence, a possible option to investigate is to anticipate the use of tracking information in the Level-1 selection, along the lines of what is done today in the High-Level Trigger (HLT).

A similar problem is present in the single electron trigger, where high pile-up reduces the rejection power of isolation cuts on the calorimeter clusters.

Substantial discrimination power in the HLT reconstruction is provided by isolation criteria on single muon and electron candidates, which require also discrimination of the different collision vertices along the beam axis, to avoid rejecting good candidates on the basis of particles coming from another collision. In order to implement isolation cuts in the Level-1 selection, the Tracker will have to provide information on all tracks above 2 GeV, with a precision in the position of the collision vertex along the beam axis, z_0 , of at least 1 mm.

2 Implementation of the tracking trigger

The concept chosen for the implementation of the trigger functionality is based on detector modules that are able to provide selected information for the Level-1 trigger at each bunch crossing (at

Figure 1. Correlation of signals in closely-spaced sensors allows to reject low- p_T particles (a). The same transverse momentum corresponds to larger distance between the two signals at large radii, for same sensor spacing (b). In end-cap configuration, a larger spacing between the sensors is needed to achieve the same discriminating power as in the barrel at the same radius (c). The acceptance window (d) can therefore be tuned at the same time as the sensors spacing to achieve the desired p_T filtering in the different regions of the detector.

a frequency of 40 MHz), and at the same time store the full information that is sent out upon a positive trigger decision, at the usual frequency of 100 kHz.

The selection of the signals for the Level-1 stream is based on local rejection of signals from low- p_T particles, along the lines of what was originally proposed in [3].

2.1 Modules with p_T discrimination

The requirement for the module design is to reject locally signals from low- p_T particles, which are not interesting for the Level-1 reconstruction: rejecting particles with p_T below 1–2 GeV reduces the bandwidth requirements by one order of magnitude or more.

The basic concept consists of correlating signals in two closely-spaced sensors: the distance between the hits in the x – y plane is correlated with the particle p_T , allowing the p_T discrimination to be made. A pair of hits that fulfils the selection cut is called a “stub”, and its coordinates are sent out for the Level-1 processing (see sketches of figure 1). For a given p_T , the distance between the hits forming the stub is larger at larger radii; moreover, if the module is placed in end-cap configuration, the same discriminating power is obtained with a larger spacing between the two sensors, compared to a barrel module placed at the same radius. The effective p_T cut provided by the modules in the different locations can be optimized by tuning both sensor spacing and acceptance window. One of the options under study to realize modules with p_T discrimination capability (“ p_T modules”) is discussed below

3 The “PS” (Pixel-Strip) module

The module concept discussed in this paper is based on the assembly of one strip and one pixel sensor. The correlation of the coordinates measured by the two sensors in the x – y plane enables the p_T discrimination, while the segmentation of the pixelated sensor along the z direction (R direction in end-cap configuration), provides a precision coordinate that contributes to the required z_0 resolution for the reconstructed track (see above section 1.2).

Figure 2. Model of a “PS module”. Top: overall view of the assembly (a), and sketch showing the interconnectivity (b); strips are oriented along the z axis. Bottom: exploded view with all the main components.

The module has an area of approximately $5 \times 10 \text{ cm}^2$. A strip sensor and a pixelated sensor are mounted on a mechanical assembly providing support and cooling (see figure 2). The strip sensor is segmented into 2×1024 strips, making them approximately 2.5 cm in length. The individual pixels on the pixel sensor are approximately $1.5 \times 0.1 \text{ mm}^2$ in size.

Table 1. Estimates of power consumption, mass and radiation length for the PS module, including the auxiliary electronics for power and readout. The radiation lengths values are normalized to the sensor surface, and therefore correspond to the average radiation length of hermetic layers built out of these modules (external support structures and services are not accounted for in this table).

				Material		
				Mass (g)	X/X ₀	
Power				Sensors	4.29	0.43%
Front-end	Pixel ASICs	2.62 W	3.5 W	Hybrids	2.18	0.13%
	Strip ASICs	0.51 W		T management	3.67	0.19%
	Correlation	0.38 W		ASICs	2.60	0.26%
Readout	LP-GBT	0.5 W	0.8 W	Frame	7.59	0.39%
	GBTIA	0.1 W		HV	0.17	0.01%
	GBLD	0.2 W		Cooling contacts	2.44	0.22%
Power	DC-DC converter	0.8 W	0.8 W	Power	2.07	0.12%
Total				Connector	0.29	0.02%
				Screws	0.48	0.08%
				Opto	3.00	0.15%
				Total	28.8	2.0%

The strips are read out at the edges: wirebonds provide the connectivity to a high-density substrate carrying the ASICs, that are bump-bonded onto it. The pixelated sensor has its readout ASICs bump-bonded on it; wirebonds connect the chip periphery to the substrate carrying the strip ASICs, hence realizing the top-to-bottom connectivity; two wires are required for each pixel row, resulting in a wirebonding pitch of $50\ \mu\text{m}$. The correlation logic is implemented in the pixel chip periphery.

The shorter module dimension along the z coordinate is driven by the need to cover the entire length with two pixel chips, while the short strips make the module suitable for operating in regions with high particle densities. The chosen dimensions allow to obtain two sensors from a 6" silicon wafer, while the $100\ \mu\text{m}$ pitch in the pixel sensor ensures compatibility with large-volume industrial bump-bonding. For the occupancy expected at HL-LHC, this type of module is suitable for use in the radial region $R > 20\ \text{cm}$.

The auxiliary electronics is also implemented at the module level, on two “service hybrids” located on the short sides of the sensor. One service hybrid carries the DC-DC converter providing power to the module, the other carries the readout electronics and the optical converter. A preliminary estimate of the module power consumption, along with mass and radiation length, is shown in table 1. The estimates for the auxiliary electronics are extrapolations based on the ongoing developments. For the readout link, it is assumed that a further development of the GigaBit Transceiver (GBT) [2], in 65 nm CMOS technology will provide substantially reduced power consumption for the same bandwidth (Low Power GBT). For the DC-DC converter, the efficiency assumed is similar to that of existing devices [3], with a higher output current.

A brief description of the PS module electronics architecture is given below.

3.1 Electronics architecture

Both the pixel and the strip ASICs implement binary readout. After the front-end and the comparator stage, the data from the strip ASIC are sent to the corresponding pixel ASIC, which implements the subsequent processing and handling. The data from both ASICs are split in two paths, the “trigger” and the “readout”.

Readout data are stored in buffers, retrieved upon arrival of an external trigger signal, and sent to the readout link. The depth of the pipeline corresponds to a latency of $6.4 \mu\text{s}$, matching the latency of the ECAL front-end.

Trigger data are first processed to reconstruct clusters. For the pixel chip, a column of pixels is OR-ed, and the coordinate of the pixel hit is stored independently; each chip receives information from the first three channels of the neighbouring chip, in order to be able to find clusters across chips; clusters wider than a certain (programmable) threshold are rejected, and the centroid of accepted clusters is calculated.

In a second stage, the clusters found in the pixel and the strip chips are correlated to find “stubs” compatible with high- p_T particles. After time re-alignment, the cluster centroids are compared, and the combination is accepted if the two coordinates fall within a window, that has programmable width and offset.³ In this stage, each pixel chip receives information from 6 channels of the two neighbouring strip chips, in order to be able to find stubs from particles crossing the module at the edge of two chips. The coordinates of a maximum of 6 accepted stubs are encoded and sent to the readout link.

The data from the 16 pixel chips need then to be collected and passed on to the data link. Two options are considered for this part: a ring architecture where each chip sends a token and its data to the neighbour, and the last chip of the ring passes the data to the link, and a star architecture where each chip is independently connected to a concentrator chip, that formats the event and passes it to the link. The star architecture is conceptually simpler and intrinsically robust; the ring architecture requires fewer lines on the substrates and naturally implements optimal use of the bandwidth, but requires care to mitigate the effects of a failing node. A maximum of 7 stubs can be sent out in a given bunch crossing, with a sustainable average rate of 3 stubs per event.

3.2 Performance in simulation

This type of modules has been implemented in a possible upgraded tracker geometry, as shown in figure 3: PS modules cover the radial range between 20 cm and 50 cm, while the inner part implements the “phase-1” pixel detector, and the outer part is populated with “strip p_T modules”, that have similar functionalities as PS modules, but with no z segmentation. Such layout has been studied with the full CMS Monte Carlo simulation, to validate the data reduction performance, stub finding efficiency and expected precision in the L1 tracking.

For the highest expected luminosity, the densest environment is found in the first barrel layer located at approximately 23 cm, which has a rate of hit channels of nearly 20 MHz/cm^2 . After cluster reconstruction and stub finding and filtering, the rate of accepted stubs is below 1.5 MHz/cm^2 ,

³As explained earlier, the width needs to be programmable to tune the p_T threshold for a given module location in the Tracker. The offset accounts for the difference in ϕ between corresponding channels in the two sensors, and at the same time can correct for misalignments in the module assembly.

Figure 3. Possible tracker geometry, featuring PS modules in the radial region between 20 cm and 50 cm, in barrel and end-cap configuration.

corresponding to approximately 1.5 stubs per module and per bunch crossing, which compares well with the expected capabilities of the system (in the other layers the particle density is much lower, and the margin in the available bandwidth correspondingly larger). More details can be found in [6].

With the coordinates provided by the modules at Level-1, tracks could be reconstructed with a p_T resolution of $2 \div 3\%$ for $p_T = 100 \text{ GeV}/c$, and a z_0 resolution better than 1 mm in a large fraction of the acceptance.

3.3 Implementation plans and possible further developments

The technology choice for the implementation of the front-end ASICs is the 65 nm CMOS process: it is a strong technology node likely to remain available for many years, with high yield and availability of accurate simulation tools. The high density of digital logic will also help to minimize the size of the pixel chip periphery. The first analogue blocks are expected to be submitted during 2012, while the modelling of the digital logic will continue.

One limitation of the concept is the lack of connectivity between the two module halves, that are read out independently from the two sides: that generates a region of stub finding inefficiency in the centre, for particles that cross the module close to the middle line. Vias through the pixel ASICs could allow to “bridge” the two rows of chips in the middle, by adding a narrow substrate bump-bonded on top of the chips, across the middle line. A dedicated R&D is ongoing, and it is giving promising results.

Another possible improvement could be to reduce the pitch of the strip sensor down to $50 \mu\text{m}$, which would provide a 25% improvement in the p_T resolution of the stub, with a moderate impact on the overall module power consumption and on the complication of the assembly. The benefits of this option are being evaluated.

4 Conclusions and outlook

A promising concept of a pixel-strip module with local p_T discrimination has been presented.

The choice of interconnection technologies and design options is driven by the optimization of the performance for the specific needs of the tracker: the connection at the edges avoids the use of thick interposers, hence minimizing the mass, and at the same time offers the possibility to tune the

sensors spacing to optimize the p_T discrimination; the use of commercial technologies gives the perspective of high yield at an affordable cost; the module design is compatible with large-volume production (i.e. it allows for automatized assembly), and with assembly in a big detector (i.e. the module can be tested and operated as a self-contained block, and it is easy to mount and dismount from the supporting structure).

The electronics chain has been simulated in detail, and it provides the required performance to operate in the high-luminosity LHC environment. A few options are under study to further improve the design of the module.

Acknowledgments

I would like to thank the organizers for an interesting and lively workshop.

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