Status and future of the ATLAS Pixel Detector at the LHC

Alexandre Rozanov

On behalf of ATLAS Collaboration

“CPPM-IN2P3-CNRS-Univ. Aix-Marseille, Marseille, France

Abstract

The ATLAS Pixel Detector is the innermost detector of the ATLAS experiment at the Large Hadron Collider at CERN. The detector provides hermetic coverage with three cylindrical layers and three layers of forward and backward pixel detectors. It consists of approximately 80 millions pixels that are individually read out via chips bump-bonded to 1744 n-in-n silicon substrates. Intensive calibration, tuning, timing optimization and monitoring resulted in the successful five years operation with good detector performance. The record breaking instantaneous luminosities of $7.7 \cdot 10^{33} \text{cm}^{-2}\cdot\text{s}^{-1}$ recently surpassed at the LHC generate a rapidly increasing particle fluence in the ATLAS Pixel Detector. As the radiation dose accumulates, the first effects of radiation damage are now observable in the silicon sensors as an increase in the silicon leakage current and the change of the voltage required to fully deplete the sensor. The fourth pixel layer at the radius of 3.3 cm will be added during the long shutdown 2013-2014 together with the replacement of pixel services. Letter of Intent was submitted for the completely new Pixel Detector after 2023, capable to take data with extremely high leveled luminosities of $5 \cdot 10^{34} \text{cm}^{-2}\cdot\text{s}^{-1}$ at High Luminosity LHC.

Keywords: Large Hadron Collider (LHC), Pixel Detector, ATLAS, High Luminosity (HL)

1. Introduction

The ATLAS Pixel Detector [1] provides tracking information near the collision point and allows to find primary and secondary vertices in the ATLAS experiment [2]. The Pixel Detector gives three space points over the complete acceptance of the inner detector in the pseudo-rapidity range $-2.5 < \eta < 2.5$. The innermost barrel pixel layer (b-layer or layer-0) is located as close as possible (R = 5 cm) to the interaction point. Three cylindrical layers (R = 5, 9, 12 cm) and two end-caps, with three disks each (R = 9-15 cm), of pixel detectors provide hermetic coverage (Fig. 1). The active part of the Pixel Detector is made out of identical modules. A module is an active device with 2x6 cm with the sensor containing 47232 pixels. Typical pixel size is 50 x 400 µm. Planar 250 µm thick n-on-n Si sensors are used with 150 V bias. Sixteen front end chips [3] are bump bonded to the Si sensor. Front end chip (2880 pixels each) perform minimum ionizing particle detection and zero suppression on L1 trigger level. Each pixel has low noise amplifier with adjustable constant current feedback, low threshold discriminator with 5/7 bits adjust, charge measurement with Time over Threshold (ToT), bunch crossing time stamp at 40 MHz, analog and digital test pulse injection. End of column logic contains 64 deep hit storage during L1 latency in each double-column, zero suppression on L1 trigger and data transfer via flex hybrid circuit to Module Controller Chip (MCC) [4] for local event building. The data are readout from the MCC at 40-160 Mb/s speed, depending on layer. Pixel sensors and electronics are radiation tolerant up to the ionizing damage of 50 MRad ($\sim 10^{15} \text{n}_{eq}\text{cm}^{-2}$), which should be sufficient for data taking up to $\sim 300 \text{fb}^{-1}$ integrated luminosity. The pixel modules are cooled to -5/-13°C by evaporative C3F8 cooling. Low temperature cooling evacuate the heat produced in the electronics and sensors, slow down the radiation damage of the sensors and prevent the thermal run off after high dose irradiation when the depletion voltage should be raised up to 600 V.

Figure 1: Active region of the ATLAS Pixel Detector [1].

2. Operation, calibration, performance

Five years successful operation of the ATLAS Pixel Detector was possible due to rigorous tuning, monitoring and calibration procedures. Actual pixel thresholds were tuned to 3500 electrons with only 40 electrons dispersion (see Fig. 2) [5],[6].

Only 0.1 % of pixels were masked for such excellent threshold tuning. The corresponding pixel noise in a normal pixel is $\sim 170$ electrons (it is higher $\sim 300$ e in rare long/ganged pixels). This threshold tuning [6] results in a comfortable threshold/noise ratio $\sim 22$, presented on Fig. 3.
Figure 2: Pixel threshold distributions for normal, long and ganged pixels after tuning to 3500 e\textsuperscript{−} [6].

Figure 3: Pixel threshold to noise ratios distributions for normal, long and ganged pixels after tuning to 3500 e\textsuperscript{−} [6].

Lower threshold of 2000 e\textsuperscript{−} are also possible, but need more operational efforts. ToT charge was tuned to 20 (in units 25 ns Bunch Crossings (BC)) with 20 ke pulse injections. Such a ToT tuning makes possible reconstruction of the pixel cluster position with analog weighting algorithms and also single charged particle dE/dx measurements. The bands for pions, kaons, protons, antiprotons and deuterons are clearly visible on the plot with mean truncated charge versus momentum on Fig. 4 [8].

Figure 4: dE/dx calculated with mean truncated method on 3 pixel layers versus track momentum [8].

The pixel noise is so low that by disabling online only 0.1 % of noisy pixels with more than 10\textsuperscript{−}5 rate we reach less that 10\textsuperscript{−}7 noise occupancy. After final offline masking the noise occupancy is less than 10\textsuperscript{−}9. This corresponds to less than 0.1 noise hit per event in 80 millions pixels. However the real pixel occupancy during proton collisions comes not from the electronic noise, but from the particle hits due to the pile up of multiple minimum bias events in each bunch crossing. This effect was increased by a factor of two due to the 50 ns BC in 2011/12 running. The record breaking instantaneous luminosities of 7.7 \cdot 10^{33} cm\textsuperscript{−2} s\textsuperscript{−1} recently surpassed at the Large Hadron Collider generate a rapidly increasing particle fluence. For example, on the Fig. 5 a Z → \mu\mu event [7] is displayed with 25 pile-up vertices reconstructed with Pixel Detector.

Figure 5: Z → \mu\mu event with 25 pile-up vertices [7].

This high occupancy results in higher probability of module de-synchronisation due to the Single Event Upset (SEU) and readout errors, especially at the beginning of each LHC fill. Special module auto-recovery procedures reduce the number of these errors [6], as shown on Fig. 6 as a function of luminosity block number.

Figure 6: Number of pixel errors with and without auto-recovery procedure as a function of time in luminosity block number units [6].

As the radiation dose accumulates, the first effects of radiation damage are now observable in the silicon sensors. A regular monitoring program has been conducted and reveals an increase in the silicon leakage current, which is found to be correlated with the rising radiation dose recorded by independent sensors within the inner detector volume. The average leakage current per pixel layer, normalized to 0\degree C [6] is shown on Fig. 7, where one can clearly see the biggest effect in the layer-0. The predictions are describing well the measurements after scaling by 15 % in b-layer and 25 % in other layers. In the longer-term crystal defect formation in the silicon bulk is expected to alter the effective doping concentration, producing type-inversion and ultimately an increase of the voltage required to fully deplete the sensor. The decrease of the depletion voltage before the type inversion was clearly observed [6] by measuring pixel cross-talks (see Fig. 8). This method is so sensitive, that one can observe circular structures of very small doping variations in the silicon sensor wafer on Fig. 9 [6].

One of the most important characteristics of the pixel detector is the efficiency of active modules. The fraction of pixels affected by disconnected and merged bumps is close to 0.1 % only. Typically another 0.1 % of pixels are masked for noise.
suppression. Hit doubling mechanism of low charge pixel implemented in FE-I3 reduce in-time threshold and recuperate low charge pixels into correct BC correcting the time slewing effects. The efficiency of the active modules measured on the reconstructed tracks is approximately 99 % on most parts of the detector.

The spatial resolution of Pixel Detector is improved by ToT charge sharing mechanism as seen for transverse coordinate on Fig. 10 [6] and for longitudinal coordinate on Fig. 11 [6]. Transverse impact parameter resolution \(d_0\), which is crucial for vertex reconstruction and b-tagging, is close to the MC predictions (Fig. 12 [9]) and is well described by parameterization \(\sigma(d_0) = 10\mu m \oplus 140\mu m/\sqrt{p_T}\) GeV/c. Such a high precision vertex reconstruction allows detailed material mapping of the pixel detector by “hadronoscopy” with secondary hadron vertex distributions as shown on Fig. 13 [6].

After almost five years of operation from August 2008 up to January 2013, 95 % of ATLAS Pixel Detector is active. The non-active part consists of 88 disabled modules (5.0 %) and 47 disabled front-end chips (0.2 %). After some initial mortality, the average failure rate was 0.7 % per year. The massive off-detector VCSEL mortality was identified to be due to humidity damage and already repaired by dry air flow and changing the VCSEL type in the off-detector boards. Many of the failures inside Pixel Detector are correlated with cooling stops, so special effort was to reduce to the minimum the frequency and speed of thermal cycling. Most of the failures are probably related to the optoboards (cold soldering, broken wire-bonds, VCSELs failure, capacitors defects etc). The exact diagnostic of the failures will be known only after the full access to the detector, but...
there is a good chance to put back into operation 80 % of the disabled modules by replacing the actual services with new Service Quarter Panels (nSQP) during 2013-2014 LHC shutdown. The full pixel package should be removed from the ATLAS and transported into the surface clean room for the nSQP installation and repairs. New position of opto-boards at 6.6 m from the collision region will allow their maintenance every year. Installation of nSQP will also improve the data readout bandwidth of the pixel layer-1 by doubling the number of optical fibers, which might be important if LHC luminosity will be increased after the 2018 shutdown up to $2 \cdot 10^{34}$cm$^{-2}$s$^{-1}$. It will also give the possibility of reducing the material budget in the region $|\eta| = 2.2-2.6$ and will allow installation of new Diamond Beam Monitors (DBM). The physics impact of the nSQP installation was estimated as improvement in the rejection of the background light jets at the b-tagging of b-quarks. Assuming that ATLAS will run with the pile-up of 50 minimum bias events, expecting 2 % b-layer inefficiency, 80 % pixel modules repaired and reduction of the future module failure rate to 0.25 % per year, we expect the rejection of light jets will be improved by 20 % due to this nSQP installation.

4. Insertable B-Layer (IBL) - fourth barrel layer

The fourth pixel layer [10] at the radius of 3.3 cm will be added during the long shutdown 2013-2014 together with the replacement of pixel services. It will be installed very close to the new Be beam pipe of radius $R = 2.44$ cm. Fourth pixel hit combined with smaller longitudinal pixel pitch (250 $\mu$m) will improve the pattern recognition in the high pile-up environment. Shorter extrapolation lever arm and light material budget of IBL (1.9 % X0) will reduce multiple scattering errors for transverse impact parameter. Longitudinal impact parameter resolution will also be improved by small pixel pitch and shorter extrapolation. All these upgrades result in the improvement of the b-tagging by a factor of two even with 50 pile-up events. The active area of each of 14 IBL staves is 2cm x 64 $\mu$m x 223 cm. This provides coverage in $|\eta| < 2.5$. Planar n-in-n Si sensors [11] are used in 12 two-chip modules in the central part of the stave. 3D n-in-p Si sensors [12] are used in 8 one-chip modules at high pseudo-rapidities. The inactive area between two modules is 450 $\mu$m. FE-I4-B chip in 130 nm CMOS IBM technology is thinned to 150 $\mu$m and bump-bonded to the sensors. FE-I4 is the largest hybrid pixel chip in HEP with 26880 pixels (80 M transistors) of 50 $\mu$m x 250 $\mu$m pitch, which are arranged in 80 columns in $z$ and 336 rows in $\phi$. Four-pixel digital region contains local memory with recovery of low charge pixels in the correct BC in order to reduce time-walk effects. Zero suppression is done in the local pixel memory at L1 trigger, avoiding the transport of large amount of data to end-of-column region. The resulting dead-time at a pile-up of 80 events is only 0.6 %. The chip provide 4-bit charge ToT for each pixel hit. The chip can be readout at 200 kHz L1 trigger rate with output bandwidth of 160 Mb/s. Special design of the memories reduce SEU error cross-section to $< 10^{-15}$cm$^{-2}$. Both IBL sensor and electronics are designed for the radiation dose of 250 MRad ($\sim 5 \cdot 10^{15}$n$_{eq}$cm$^{-2}$), sufficient for Phase-I run up to 550 fb$^{-1}$. The IBL stave production should be finished in autumn 2013 for the installation in ATLAS beginning 2014. The transportation of the Pixel Detector to the surface (for nSQP installation and repairs) will greatly reduce the risk of IBL insertion into the existing Pixel Detector, as IBL support tube will be introduced into existing Pixel Detector (only 2 mm clearance) in the comfortable conditions of the clean room with close control.

5. Plans for High Luminosity LHC

ATLAS Collaboration recently submitted to CERN LHCC the Letter of Intent [14] for Phase-II upgrade, proposing in particular a completely new Pixel Detector after 2023, capable to take data with extremely high leveled luminosity of $5 \cdot 10^{34}$cm$^{-2}$s$^{-1}$ at HL LHC. The baseline pixel system has a classical layout with four pixel layers and 12 disks with total area of 8 m$^2$ and 638 M pixels. Alternative layouts with conical and shingled geometry are under studies. Light carbon structure mechanics (I-beam, flat, IBL-like options) are proposed to reduce material budget up to 1.2 % X0 per layer. The inner layer of the Pixel Detector should support the radiation dose up to 770 MRads during the run with total luminosity of 3000 fb$^{-1}$ in 2023-2033. This require further R&D on sensors in inner pixel layers: planar Si, 3D silicon and diamonds. R&D on front-end electronics for inner pixel layers is ongoing to meet radiation and high occupancy requirements. First pixel front end chip prototype in 65 nm CMOS technology targeting the pixel size of 25 $\mu$m x 150$\mu$m [15] gives very satisfactory results. Another option is to use 3D electronics with vertical integration using Through Silicon Vias (TSV) separating analog and digital tiers. Test 3D chips [16]-[17] compatible with 50 $\mu$m x 125 $\mu$m pixel size in 130 nm CMOS have shown excellent performance with two tiers communication. ATLAS is also looking into the novel HV CMOS approach [18] for monolithic pixels with extremely thin sensor layer and integrated analog electronics. It is very interesting for capacitive coupled pixels, 3D integration pixels and strip sensors. Intensive R&D program started on the multi-chip FE-I4 modules, flex/cables integrated into mechanical structures, pixel serial powering, Gigabit links etc. Part of the pixel system planned for Phase-II can be deployed earlier during Phase-I [19] 2018 LHC shutdown in order to benefit from the new pixel technology during the main LHC 300 fb$^{-1}$ run.
References

[12] Clara Nellist, paper presented at this Conference.