Prototype system for phase advance measurements
of LHC small beam oscillations

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Abstract

Magnet lattice parameters of the Large Hadron Collider (LHC) are measured by exciting beam transverse oscillations that allow measuring their phase advance using the beam position measurement (BPM) system. However, the BPM system requires millimetre oscillation amplitudes, with which nominal high intensity beams would cause large particle loss, dangerous for the LHC superconducting magnets. Therefore, such measurements cannot be done often, as they require special low intensity beams with important set-up time. After its first long shut-down the LHC will be equipped with new collimators with embedded BPMs, for which a new front-end electronics has been developed. Its main processing channels based on compensated diode detectors are designed for beam orbit measurement with sub-micrometre resolution. It is planned to extend this system by adding dedicated channels optimised for phase advance measurement, allowing continuous LHC optics measurement with much smaller beam excitation. This subsystem will be based on diode peak detectors, similarly to the LHC base-band tune (BBQ) measurement systems. The signal acquisition, digital processing and data transmission will therefore need to serve both Diode ORbit (DOR) and Diode OScillation (DOS) subsystems, resulting in one data stream adequate for Ethernet transmission. The DOR sub-system has already been prototyped for some time with very good results. This paper describes the first prototype of the DOS sub-system, in particular its digital signal processing implemented on a simple 32-bit microcontroller, meant to demonstrate the feasibility of real-time phase advance calculation on such a modest hardware. After introducing the subject, the system architecture and discussing the prototype processing algorithms, first lab measurement results are presented. The achieved phase advance measurement resolution in the order of 0.1° for 0.03 % amplitude modulation and 1 Hz system bandwidth gives perspective of LHC beta-beat measurements with the beam excitation at the 10 μm level.

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Prototype system for phase advance measurements of LHC small beam oscillations

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Abstract—Magnet lattice parameters of the Large Hadron Collider (LHC) are measured by exciting beam transverse oscillations that allow measuring their phase advance using the beam position measurement (BPM) system. However, the BPM system requires millimetre oscillation amplitudes, with which nominal high intensity beams would cause large particle loss, dangerous for the LHC superconducting magnets. Therefore, such measurements cannot be done often, as they require special low intensity beams with important set-up time. After its first long shut-down the LHC will be equipped with new collimators with embedded BPMs, for which a new front-end electronics has been developed. Its main processing channels based on compensated diode detectors are designed for beam orbit measurement with sub-micrometre resolution. It is planned to extend this system by adding dedicated channels optimised for phase advance measurement, allowing continuous LHC optics measurement with much smaller beam excitation. This sub-system will be based on diode peak detectors, similarly to the LHC base-band tune (BBQ) measurement systems. The signal acquisition, digital processing and data transmission will therefore need to serve both Diode ORbit (DOR) and Diode OSCillation (DOS) sub-systems, resulting in one data stream adequate for Ethernet transmission. The DOR sub-system has already been prototyped for some time with very good results. This paper describes the first prototype of the DOS sub-system, in particular its digital signal processing implemented on a simple 32-bit microcontroller, meant to demonstrate the feasibility of real-time phase advance calculation on such a modest hardware. After introducing the subject, the system architecture and discussing the prototype processing algorithms, first lab measurement results are presented. The achieved phase advance measurement resolution in the order of 0.1º for 0.03 % amplitude modulation and 1 Hz system bandwidth gives perspective of LHC beta-beat measurements with the beam excitation at the 10 µm level.

Keywords—phase measurement; quadrature demodulation, LHC; betatron oscillations; beta-beating;

I. INTRODUCTION

The LHC accelerator contains some 1200 dipole superconducting magnets bending its two beams to close their trajectories on the 27 km circumference and some 400 main quadrupole magnets, controlling the beam sizes [1]. Those main magnets are accompanied by some 7000 other superconducting and warm magnets, setting higher order beam dynamics and correcting the fields of the large magnets. Magnetic field in each of the magnets changes with its current, which is a function of the actual beam energy and the machine operation mode, and is provided by a power converter. Often magnets of the same family are powered in series, resulting in about 1700 independent power converter circuits, requiring some 86 MW of the peak input power [1].

In general, beam dynamics in a given point of the LHC circumference depends on magnetic fields of many magnets, whose current functions are calculated and set assuming desired beam dynamics and magnet models based on calculations and measurements. The accuracy of those models is often not sufficient to guarantee the required quality of the LHC optics and its scaling with beam energy and therefore particle beam is used as the ultimate probe of the magnetic field. One of the methods allowing fine beam dynamics corrections, so called beta-beat measurement, consist of exciting beam transverse betatron oscillations by means of a dedicated magnet, so called AC-dipole [2]. The oscillations are observed with the Beam Position Monitor (BPM) system, allowing measuring the position of each of the LHC beams in some 500 locations, independently in the horizontal and vertical planes, with the time resolution adequate to distinguish individual nanosecond beam bunches with 25 ns spacing [1]. The phase advance of the driven oscillations changes from one BPM to another according to the magnetic field lattice of the accelerator and the knowledge of the phase advance allows optimisation of the accelerator optics, and as a result, improving the LHC performance and safety.

The minimal beam oscillation amplitude used for beta-beat measurements is limited by the resolution of the LHC BPM system along with the required phase measurement quality and the maximal amplitude is defined by the acceptable particle losses. The LHC BPM system was optimised for trajectory measurements and is capable of measuring beam excursions in the order of a few tens of mm, which however makes it not optimal for measurement of small beam oscillations. Therefore beta-beat measurements require oscillation amplitudes in the order of 1 mm to obtain phase advance measurement resolution in the order of 0.1º. Unfortunately such oscillations are far too large to be applied to the nominal LHC physics beams, as they would generate too much particle loss, dangerous for the LHC superconducting magnets. This is why beta-beating is measured only with specially prepared safe beams of much smaller intensity, making the measurement quite time consuming. For this reason the beta-beat measurements cannot be performed as a regular operational procedure, which potentially might improve the LHC overall performance.
Measurements based on beam oscillations are also required to determine the LHC betatron tune frequency, that is the frequency of natural betatron oscillations. The tune frequency is critical for beam stability and its lifetime and as such must be measured and controlled using a real-time feed-back system, also with the nominal physics beams. For such beams maximal allowable beam oscillation amplitudes are in the order of 1 µm and therefore a new technique was developed for the LHC tune measurement [3]. In this technique, called direct diode detection (3D), an unprecedented resolution for betatron oscillation detection was achieved by rejecting the large beam position nanosecond pulses from a BPM before any active electronics and processing only small oscillation signals, being an amplitude modulation of the large pulses. The performance and simplicity of the Base-Band Q (BBQ) system exploiting the 3D technique initiated ideas of using it also for beta-beat measurements. The prove-of-principle hardware was set-up on the SPS accelerator in 2008 and beam measurements were performed, as described in [4]. The measurements demonstrated that the 3D technique is very efficient for beta-beat measurements, however, its operational implementation on the LHC was at that time not possible. After a few years the situation changed, as in 2015 the LHC will be upgraded with new collimators, equipped with embedded BPM button electrodes [5], for which a new front-end electronics has been developed [6]. Similarly to the BBQ system, it is based on diode detectors and requires high resolution ADCs operating in the kHz range, which opens a possibility to build electronics accommodating in one unit both, orbit measurement system and beta-beat dedicated circuits, sharing the BPMs, cables, data processing and transmission. In this way the Diode Oscillation (DOS) sub-system can be added to the Diode Orbit (DOR) system at small development and production cost, resulting in one Diode Orbit and Oscillation (DOROS) system.

II. ARCHITECTURE OF THE DOROS SYSTEM

The primary application of the DOROS system is processing of signals from the new collimator BPMs to allow precise control of the LHC collimator jaws to position them symmetrically with respect to the beam. The DOROS system will be optimised for this purpose and the DOS sub-system is designed to be compatible with the optimal choices made for the DOR part. In this section the DOR system is described only as an introduction to the signal processing of the oscillation signals. Further details on the DOR system can be found in [6].

The block diagram of two channels of the DOROS front-end is shown in Fig. 1, foreseen for signals from one pair of BPM electrodes. One DOROS front-end, built as 1U 19” unit, will accommodate 8 channels, intended for 4 electrode pairs. Nominal LHC beams induce on BPM electrodes nanosecond pulses with amplitudes in the order of 100 V, which are too large for active electronics. Therefore, the input constant impedance (non-reflective) 80 MHz low-pass filters (LPF blocks in Fig. 1) lower the pulse peak amplitude to fit into the system dynamic range for the maximal beam intensity and make the beam pulses longer. The filters are followed by RF transformers (Tr) providing a galvanic insulation between the system ground and the LHC ground with BPMs and long coaxial input cables, which are subject to interference from nearby large high power circuits. Then the signals pass calibration circuitry, allowing cross-calibration of the channels with beam or locally generated calibration signals. The programmable gain amplifiers (PGAs) allow amplification of signals of low intensity beams to the level of linear operation of the following compensated diode detectors (CDDs), which are the key part of the DOR sub-system. The DOR signal bandwidth is limited to some 10 Hz and then digitised with two channels of a 24-bit ADC. The two followers (F) decouple the beam pulses going to the DOR compensated diode detectors, producing DC orbit signals, and DOS diode peak detectors (DPDs), delivering signals related to small amplitude modulation of large beam pulses and suppressing DC beam position signals. The DOS detector signals are sent to a differential amplifier (DA), prior to pass by low-pass filters with the cut-off frequency of 0.5*frev, where rev is the LHC revolution frequency of 11.2 kHz. Then the oscillation signal is digitised with another channel of the ADC shared by both DOS and DOR sub-systems. The ADC samples acquired at frev rate are transmitted through an SPI link to the microcontroller (MC), performing all digital signal processing. The microcontroller is connected to the Ethernet Physical Layer (EPL) block, assuring Ethernet communication and allowing sending the processed samples as UDP frames.

A very important part, especially for the DOS sub-system, is the Synchronisation Circuits (SC) block. It allows relating the oscillation signals acquired by different DOROS front-end units, which are not guaranteed to be installed in the same location. The block allows synchronising external reference signals delivered by the LHC timing system to their local equivalents derived from beam pulses. These circuits will be discussed in detail in a following chapter.

III. PHASE CALCULATION ALGORITHM

As the beam transverse oscillations are excited on
frequency $f_{exc}$ in the ideal case the output signal on $k$-th DOS channel contains only one harmonic component of frequency $f_{exc}$ and amplitude $A_k$ with an arbitrary phase $\phi_k$. If the signal is sampled at $f_s$ rate and sampling period of $T_s = f_s^{-1}$, then its $n$-th sample is

$$s[n] = O_1 + A_k \sin(2\pi f_{exc} n + \phi_k)$$

where $O_1$ is the channel DC offset. The interesting information is present at $f_{exc}$ only, so it is possible to employ the digital quadrature demodulation principle, schematically shown in Fig. 2. It allows narrow-band detection of the component of interest, replacing band-pass filtering around $f_{exc}$ by low-pass filtering around DC, which is much more efficient to implement.

Since the excitation frequency $f_{exc}$ is known, it can be used to generate digital local oscillator (LO) quadrature components

$$LO_i[n] = A_{LO} \cos(2\pi f_{exc} n + \phi_{ref})$$
$$LO_q[n] = A_{LO} \sin(2\pi f_{exc} n + \phi_{ref})$$

where $A_{LO}$ is the amplitude of the components. It is assumed that the components have $\phi_{ref}$ phase common for all DOS front-ends. Such synchronisation will be achieved by means of the DOROS synchronisation circuits, LHC timing system and procedures described later.

By mixing $s[n]$ with $LO_i[n]$ and $LO_q[n]$ one produces in-phase and quadrature components, considered as real and imaginary parts of a complex signal. The complex mixing product signal contains components at DC with amplitude dependent upon the signal phase relationship and unwanted harmonics. The exact value of the operational frequency $f_{exc}$, of margin for the compromise between two BPMs is then calculated as the difference of the respective DOS channel phases.

In the LHC case the $f_{exc}$ frequency is always related to the machine revolution frequency $f_{rev}$ distributed by the LHC timing system (e.g. $f_{exc} = 0.3 f_{rev}$). Each unit of the DOROS system will receive $f_{rev}$ reference signal, which will allow generating the local oscillator quadrature signals. Also the

ADC sampling frequency $f_s$ will be equal to $f_{rev}$, assuring the sampling synchronisation in all DOROS front-ends, potentially dispersed in distant locations around the LHC circumference.

In reality the DOS signals will contain, in addition to the useful component at $f_{exc}$, also noise and interference, polluting the quadrature mixing products. They have to be removed by the low-pass filters before calculating (4), therefore, the quality of these filters influences directly the final result accuracy. As the phase information is carried at one frequency only, in case of constant spectral noise density, the signal-to-noise ratio (SNR) at the filter output is inversely proportional to its bandwidth. Therefore, the filter cut-off frequency should be as small as possible to minimise the noise on the components of the quadrature mixer output signal, which converts into the noise of the final calculated phase according to (4).

In the LHC case the phase advance information is typically required at 1 Hz rate, allowing using some $10^4$ DOS signal samples acquired at $f_{rev}$ rate for producing one phase reading. This opens a possibility of building very efficient low-pass filters with cut-off frequencies in the Hz range.

Beam DOS signals will contain many unwanted components related to beam dynamics and other systems acting on the beam. The most important ones are the natural betatron oscillations, spaced from $f_{exc}$ by some 300 Hz and 50 Hz mains harmonics. The exact value of the operational frequency $f_{exc}$ can be chosen such that it is located between two 50 Hz spectral lines, giving 25 Hz, that is 0.002 $f_{rev}$, of margin for developing the filter stop-band attenuation. Therefore, the quadrature mixer filters should be optimised for good attenuation at 25 Hz. The final choice of the filter must address the compromise between the filter attenuation and its bandwidth, as better stop-band behaviour implies larger filter bandwidth for the same filter response delay time, in this paper referred to as the filter length. The final trade-off between the filter equivalent-noise bandwidth (ENBW) and sidelobe level and decay will depend on the expected noise and interference on the beam signals. The best seems an implementation of a filter with an architecture allowing changing its frequency characteristic from a simple averaging filter, having very good noise and poor spectral properties, to a filter with a fast asymptotic sidelobe decay, which, however, implies worse ENBW. Then the filter characteristic can be easily configured by changing the filter coefficients according to the actual beam conditions.
The quadrature mixer low-pass filters should have frequency characteristic with zeros creating notches distributed at multiples of \( f_s/N \), where \( N \) is the filter length. The notches are foreseen for optimal filtering of the unwanted mixing product around \( f_{exc} \) and \( 2f_{exc} \). To profit from this feature, the excitation frequency should be one of the discrete frequencies

\[
f_{exc} = \frac{f_s}{N m}, \quad m \in \{1, 2, \ldots, \frac{N}{2} \}
\]  

(8)

The digital local oscillator can be realised as a look-up table (LUT) with values of the first quarter of the sine wave expressed in an integer fixed-point arithmetic. Taking into account condition (8), the number of LUT values for \( m \)-th optimal frequency is

\[
L_{\text{LUT}} = \frac{N}{4m}
\]  

(9)

To keep the maximal \( f_{exc} \) resolution of \( f_s/N \) one needs \( N/4 \) values in the LUT. For example, a filter with length of \( N = 10^4 \) allows optimal \( f_{exc} \) values every about 1 Hz requiring a reasonable 10 kB of memory for 32-bit LUT values.

IV. SYSTEM SYNCHRONISATION

Equation (1) assumes that the phase of the sampled DOS signal is independent of \( f_{exc} \) frequency. In general this is not true, as sampling of each DOS signal \( s_k[n] \) depends also on a delay \( \tau_k \) related to the propagation time difference of the beam signals and the external \( f_{rev} \) reference defining the ADC sampling clock

\[
s_k[n] = O_k + A_k \sin(2 \pi f_{exc} (T_k n + \tau_k) + \phi_k)
\]  

(10)

resulting in a phase component \( \phi_k \) depending on \( f_{exc} \)

\[
\phi_k = 2 \pi f_{exc} \tau_k
\]  

(11)

The above relation can be used to calculate delays \( \tau_k \) on each DOS channel by measuring the phase change \( \Delta \phi_k \) caused by an excitation frequency change \( \Delta f_{exc} \). Then the subsequent DOS phase measurements are compensated for \( \phi_k \) according to (11). As evaluation of \( \phi_k \) requires only a relative measurement, the phase resolution in the order of 0.01° is possible, especially that for such a special procedure longer measurement time and larger excitation amplitude can be afforded. For the frequency change of 0.25\( f_{exc} \), this would allow some 10 ns time resolution.

As seen in (4), each DOS channel provides phases with respect to phase \( \phi_{LO} \) of the quadrature mixer LO. Each DOROS front end will receive \( f_{rev} \) reference signal, however, its exact phase is unknown, depending on many parameters, as for example the length of the optical link distributing the LHC timing. However, the phase of the \( f_{rev} \) reference can be adjusted on the timing receiver module by comparing it to its locally generated equivalent, using the synchronisation circuits shown schematically in Fig. 3 for one BPM. One DOROS unit will have two such blocks, one for each of its BPs. As in general the BPs can be in different LHC locations and have different cable lengths, the blocks are fully independent, delivering clock signals to two ADCs, based on two external \( f_{rev} \) references. The DOROS synchronisation principle is similar to the one of the existing LHC system, in which a calibration procedure the bunch timing related to each BPM can be individually adjusted in 0.1 ns steps to align with the BPM beam signals.

The most important part of the DOS synchronisation scheme in Fig. 3 is the Local Timing Generator (LTG) block, generating local \( f_{rev} \) reference. In the simplest case it can be just a fast comparator triggered with beam pulses. If the LHC is filled with only one bunch, each LTG in the DOROS system will generate pulses synchronous to the beam.

As sketched in Fig. 3, the local and external \( f_{rev} \) references go to a phase detector (PD) followed by a low-pass filter (LPF), whose slowly changing output voltage is measured on one of the ADC channels. The phase detector is constructed in such a way, that when the rising edges of the local and external \( f_{rev} \) references are aligned, the ADC measures minimal voltage \( V_{ref} \). During the calibration procedure the phase of the external \( f_{rev} \) reference is adjusted to minimise \( V_{ref} \), indicating the phase match of the local and external references. Once the phase of the external \( f_{rev} \) reference is calibrated, each DOS channel uses this signal to synchronise sampling of its ADC and the quadrature mixer LOs. This synchronisation is done by a Phase-Locked Loop (PLL), including the internal ADC divider (/512) relating the ADC master clock (MCLK) provided to the ADC and the ADC sampling clock (CLK) appearing on an ADC output. The PLL has a phase detector giving the lock when the phase difference between the external \( f_{rev} \) reference (already synchronised to the beam as described above) and the ADC sampling clock is zero. As shown in the block diagram, the quadrature mixer LO is synchronised to the ADC sampling clock.

The DOROS system cannot operate with only reference \( f_{rev} \) generated locally by the LTGs, as their synchronous operation on all DOROS units cannot be guaranteed at all times. In particular, an important perturbation in LTG operation will be switching gains of the amplifiers, perturbing beam signal continuity. This is why the DOROS synchronisation has to be based on the external \( f_{rev} \) references from the LHC timing. The internal ones generated locally are required only occasionally for the calibration procedure and then special conditions can be assumed. In particular, one can assume that when there is no beam in the LHC, the synchronisation circuits in each DOROS
unit are reset and the system gain is set to an optimal value for the intensity of the expected pilot bunch, always injected as the first one. Then the injected pilot bunch triggers successively all DOROS units, enabling their time stamp counters. If the counters count periods of external \( f_{exc} \), they allow precise time stamping of UDP frames sent from all DOROS front-ends.

In the final system the LTG will be implemented in a more general way, so that it can also work with the nominal LHC beams with 2808 bunches. It will employ the fact that the LHC 25 ns bunch train does not occupy the whole 89 µs of its revolution period, but always has some 3 µs gap (so called abort gap). The LTG of each DOROS unit will trigger on the first bunch after the abort gap.

Please note that the acquisition of the DOR signals does not require any synchronisation and for convenience will be done in parallel to DOS signals, to profit from 8-channel ADCs.

V. PROTOTYPE SYSTEM

The DOS prototype was built as a sub-system accommodated with the DOR prototype in one 19” 1U unit. The DOS part had a simplified architecture, adequate for fast implementation, however, allowing an estimation of the performance of the final system. The DOS sub-system contained two channels, sharing the high frequency part and acquisition with four DOR channels. The acquisition was done with a \( \Sigma \Delta \) 24-bit ADC having 8 simultaneously sampled channels, 4 of which were used by the DOR sub-system and 2 by the DOS part. One remaining channel was used to measure the voltage from an analogue temperature sensor and the second was connected to the ADC reference for test purposes. The prototype microcontroller was clocked at 80 MHz and had 256 kB of RAM and 512 kB of flash memory. It was connected to the Ethernet through a specialised physical layer chip.

The ADC master clock was based on the 10 MHz reference of the signal generator (Agilent 33522A) used to simulate beam signals during lab measurements, assuring the synchronisation of the ADC sampling to the DOS input signals. The ADC MCLK of 5 MHz resulted in the sampling frequency \( f_s \) of about 9.8 kHz. The ADC was sampling continuously storing samples from its all channels in a serial format in the SPI buffer. Once the buffer was full with the new data, the ADC was generating an interrupt on the microcontroller, while maintaining the continuous sampling. This way the microcontroller processing was synchronised to the ADC sampling. The microcontroller was then reading the ADC data from the buffer over the SPI link clocked at 20 MHz. The 24-bit DOR and DOS samples were converted to numbers in fixed-point Q1.31 arithmetic prior to further processing.

The DOS quadrature mixer was simplified to operate only at one frequency \( f_{exc} = f_s / 4 \). Its low-pass filters were implemented as classical averaging filters with programmable length \( N \). Please note that such a filter has very good noise properties (ENBW = \( f_s / N \)) and has notches in the frequency characteristic every \( f_s / N \). All \( N \)-s being multiples of 4 guarantee notches at \( f_s / 4 \) and \( f_s / 2 \), optimal for filtering high frequency products of the quadrature mixing at \( f_s / 4 \). The averaging filter has very poor sidelobe decay, however, it was not a problem for lab measurements aiming mostly at estimating noise influence on the phase measurement quality. The DOR samples were averaged by the same factor \( N \) as DOS samples. All DOS and DOR results were truncated, formatted to Q1.31 numbers and stored in the output UDP buffer prior to sending in an UDP frame.

The DOROS prototype was controlled by a web interface, implemented on the microcontroller as an HTML server. The prototype allowed sending data to two IP destinations and continuous transmission of raw non-processed ADC samples. The UDP frames with the DOROS data could be synchronised to an external 25 Hz timing, used also by the standard BPM system.

VI. LAB MEASUREMENTS

The DOS sub-system prototype was tested only in the lab as beam tests were not possible, due to the lack of dedicated beam time. However, the parts common for both DOS and DOR sub-systems, in particular high frequency amplifiers, data acquisition and transmission were tested on the DOR prototype, operating during 2011 and 2012 runs on the SPS and LHC, with the most recent results described in [6].

The DOS prototype was measured in a lab with beam signals simulated by a signal generator, producing a sinewave of 12.345678 MHz chosen to avoid correlations with its amplitude modulation, simulating the beta-beat driven beam oscillations. The simulated excitation frequency was exactly \( f_s / 4 \), that is about 2.44 kHz, assured by using the generator 10 MHz reference to produce the ADC master clock.

For beam operation the oscillation signals appear on the BPM opposing electrodes out-of-phase. This is why the DOS diode detector signals are first processed by the differential amplifier. During lab measurements the generator was driving one of the beam inputs of each of the DOS channels, while the second inputs were grounded, forcing equal signals on both DOS channels. Then the expected phase difference between the two DOS channels was zero, allowing precise measurement of the systematic and statistical phase errors.

All the presented measurements were done for the worst case of the maximal system gains, which were 35 dB for the RF programmable gain amplifiers and 60 dB for the low frequency differential amplifier. Typical DOS signal spectra for \( N = 10^4 \) samples are shown in Fig. 4 for the amplitude modulation of the simulated beam signals of 0.01 %. The average of 100 independent spectra (in red) allows estimating the frequency domain SNR for some 46 dB. The time domain SNR is smaller by the FFT processing gain of \( \sqrt{N/2} \) and can be estimated for some 10 dB, quantifying the sensitivity of the diode detection method. Please note that the spectral noise floor is not flat, shaped by the RC filters of the DOS diode detectors and the 0.5 \( f_s \) low-pass filters.

The standard deviation of the phase measurements as a function of the amplitude modulation depth is shown in Fig. 5 for two prototype DOS channels (in blue) and their phase difference (in red). Each point corresponds to 100 measurements, each done on \( 10^4 \) DOS samples. It can be seen that the fit of the measurement standard deviation is approximately inversely proportional to the amplitude
modulation depth. The upper horizontal axis is scaled in the absolute beam oscillation amplitude, assuming conversion of the modulation depth into micrometres according to the theoretical position characteristic of a BPM with 60 mm electrode distance, approximating collimator BPMs with jaws fully open. Note that the phase difference measurement with a statistical error of about 0.1° can be expected with the oscillation amplitude in the order of 5 µm, which would be a large improvement with respect to the current performance.

The systematic error of the phase measurement was in the order of 0.1°, caused mostly by the asymmetry of the DOS low-pass filters (2nd order Sallen-Key), having at the operating frequency 38° phase shift. It is planned to address such systematic errors by measuring the phase shift of each DOR channel at the beta-beat excitation frequency with a signal generated by a local one-chip Direct Digital Synthesiser (DDS). All DDS-es of the system can be synchronised to the same phase by clocking them with a harmonic of the external \( f_{ref} \), reference and resetting with the injection trigger.

VII. CONCLUSIONS AND OUTLOOK FOR THE FINAL SYSTEM

Noise performance of the presented prototype of the DOROS sub-system measured in the lab gives a perspective of improving the sensitivity of the LHC beta-beat measurements by some two orders of magnitude. The sub-system will be built as a part of the DOROS system, foreseen to be installed in 2015 for processing the signals from the BPMs embedded into the new LHC collimators. One DOROS front-end unit will process signals from 8 electrodes and send the results as UDP frames. It can serve for two collimators, each having two jaws, with one button BPM on each extremity of each jaw.

Sub-micrometre beam orbit resolution and good stability of the DOR system demonstrated with beam measurements make it a potential solution to improve the quality of the LHC orbit measurement near the collision points, where the LHC experiments are installed. It is considered to install DOROS system in such critical locations in parallel to the existing operational BPM system, with the beam signals shared between the two systems. The possibility of measuring beta-beat in such locations with the DOS sub-system may be very beneficial for improving the LHC performance and safety. Therefore, the DOROS system will be built in the perspective of using it also on regular LHC BPMs, resulting in a quite large system size. For this reason the new DOROS should be optimised not only for performance, but also for reliability and the ease of its maintenance and automatic testing.

The final DOROS sub-system will be different from the prototype by having four channels, requiring substantial computational power. This demand will be increased even further by the fact that the beta-beat measurement on regular LHC BPMs is done in parallel on two frequencies, different for the horizontal and vertical accelerator planes, allowing the measurement of local betatron coupling [2]. This would require running quadrature mixing on two frequencies, doubling signal processing and the DOS final output data rate. This is why the microcontroller for the final system must have much larger processing and the DOS final output data rate. This is why the microcontroller for the final system must have much larger computing power than the one used in the prototype. Also solutions based on FPGAs are considered. The final choice will be made taking into account also other factors, like available software tools and synergies with other projects realised in the CERN Beam Instrumentation group.

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