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DESIGN AND CHARACTERISTICS OF A 32-CHANNEL, 100 MHz,
ZERO SUPPRESSING, FASTBUS PULSE SHAPE DIGITIZER

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Abstract

This paper describes a very fast, high density, time and pulse height digitizer using a novel zero suppressing technique which significantly reduces the amount of data produced by the detectors requiring a long memory time.

1. INTRODUCTION

Large volume drift chambers are widely used in high energy physics experiments for the determination of particle trajectories and energy loss. Sampling techniques recording the pulse shape in time slices as short as 10 ns [1,2] were recently developed to improve the multihit capability and the two track resolution. The design of a pulse shape digitizer for this type of application must however solve many conflicting constraints, some examples of which are:

- (1) cost, power dissipation and packing density,
- (2) easy processing of the large amount of data stored in each channel and,
- (3) long memory time in order to cope with the ever increasing variety of chamber geometries.

The 32-channel FASTBUS module described in this paper is based on a self-triggering time and pulse height digitizer, previously described in [3]. Its exceptional 82 μ s memory time, at 100 MHz sampling rate, is achieved without compromising on (1) and (2). Each channel allows the recording of a maximum of sixteen windows each of sixteen samples, within the memory time.

The Gray Addressed Time and pulse HEight Record er (GATHER - [3]) does not write baseline (or pedestal) samples into the fast memory buffer that follows the front end Flash Analog to Digital Converter (FADC [4-7]). Wire signals, together with four prepulse samples, are stored into one or more blocklets of sixteen words and the arrival time of the input pulse is unambiguously recorded by flagging:

- (1) the corresponding blocklet location and,
- (2) a time memory which is scanned eight times slower.

In this particular application, the GATHER logic is triggered by the analog sum of the pulses produced at the extremities of a current dividing wire. The FADC front end has a 6 bit accuracy and covers an 8 bit dynamic range with a hyperbolic response curve [8].

The characteristics of the 100 MHz FADC front end are discussed in the next section. The GATHER technique and its implementation in a FASTBUS environment are then described.

2. FLASH ANALOG TO DIGITAL CONVERTERS
AT 100 MHz SAMPLING RATES

Several 6-bit 100 MHz FADC integrated circuits (IC) have been extensively tested by the Physics Institute in Heidelberg, Germany [2]. They are the Siemens SDA 5010, SDA 5200 and the TRW TDC 1029. The dynamic range of these circuits has been extended by dynamically driving the divider chain as described in [8]. The detailed diagram of the front end driver for the TRW TDC 1029 is shown in fig. 1.

Fig. 1 Diagram of the front end amplifier/driver for the TRW TDC 1029 Flash ADC (hyperbolic response), (T_1 , T_2 transistors with $f_t \geq 500$ MHz at $I_c = 30$ mA and $V_{ce} = 1.7$ V).

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The binary coded value x at the output of the FADC is a hyperbolic function of the input voltage V :

$$x = 64 \cdot V / (V_0 + a \cdot V)$$

where V_0 is the voltage across the resistor ladder of the FADC (375 mV), and a , the fraction of the input voltage fed at the bottom end of this ladder (0.75). V_0 and a mainly depend on

- (1) the current source biasing the circuit and
- (2) the resistor value of the reference ladder.

However, 4% drifts do not affect the transfer characteristic and, once tuned with a parallel resistor between the V_{RT} and V_{RB} terminals, the circuit performances are stable.

Tests on the three ICs have shown the problems described in [6] e.g.: erroneous codes and weak differential linearity at high input frequencies. Moreover, packaging, power supply requirements, inputs and outputs are different. In making a choice, one has to balance performance, power dissipation and cost.

The performances at the maximum Nyquist frequency of 50 MHz are summarized by the graph in fig. 2 (hyperbolic drive). It can be seen that the TRW circuit is better at high frequencies for analog input signals with amplitudes below 40% of the full scale; whereas it is always better at 10 MHz. Another advantage of the TRW chip over the Siemens ones is that it does not need an extra level of buffering to reliably drive the down stream, 100 MHz memory. Unfortunately the TDC 1029 has a 24 pin package (16 for Siemens), a 50 Ω resistor divider (120 Ω for Siemens) and it dissipates 800 milliwatts more than its competitors.

As high Energy Physics detectors need a large number of these ICs (several thousands), the overall cost per channel will be the main criteria in making a choice.

The FASTBUS module described here has been designed to check the feasibility of a high packaging density (320 FADC channels per FASTBUS crate). It has therefore been implemented with the TDC 1029 circuit which requires more power and more board space than the Siemens ones, it will always be possible to replace it with the SDA 5200 if desired (see the modularity of the design).

Fig. 2 Performance curves for three 100 MHz Flash ADCs near the maximum Nyquist frequency, hyperbolic response, beat frequency test.

3. THE GRAY ADDRESSED TIME AND PULSE HEIGHT DIGITIZER GATHER

Fig. 3 is a schematic of the two most commonly used methods for baseline data suppression.

In the first one, the channels are driving a fast readout bus and data are digitally compared to pedestal values. Whenever data exceeds threshold, the readout processor scans the pulse height memory of the current channel and it collects useful data together with a few prepulse samples. An example of such a system can be found in [2].

In the second method, fig. 3, the comparison is analog and valid samples are written into the pulse height memory under control of a derandomizer and memory allocator circuit. A one-bit wide time memory is also necessary to calculate the arrival time of the pulses.

Fig. 3 Top: digital baseline cancellation is not practical at high frequencies and long memory times; Bottom: front end discrimination reduces the memory size.

The second method wins over the first one whenever one needs a high sampling rate together with a long memory time. Many image chambers for H.E.P. experiments have 5 to 20 μ s drift times and 100 MHz sampling rates are necessary for optimum double pulse resolution. Fast, sizable, memories would be necessary with the first circuit to store the pulse height samples whereas two 256 x 4 bit ICs are sufficient with front end baseline cancellation.

A schematic of the GATHER logic is shown in fig. 4. The pulse height memory is partitioned in 16 blocklets of 16 words and the current blocklet is continually scanned via a 4 bit GRAY coded address generator. Whenever an input pulse exceeds the

discriminator threshold, the GRAY value G is latched into a register LTRG which outputs are continually compared to (G + 4). It is readily seen that a match will be found 12 clock periods after the beginning of the pulse. At this particular time, the blocklet counter is incremented thus keeping four unaffected prepulse samples. The last used location in the blocklet is flagged by the LTRG, (G + 4) comparator output so that a time value can be unambiguously associated with each sample. The raw time information is obtained by flagging a time memory which is scanned eight times slower than the blocklets. A 1 K word time memory thus covers an 82 μ s memory time at 100 MHz.

Fig. 4 The Gray Addressed Time and pulse Height Recorder (GATHER) utilizes the mathematical properties of a 4 bit GRAY code to allocate one or more blocklets of 16 locations to discriminated input pulses.

The decoding of the time flags in the two memories is easy and the mathematical aspects are discussed in [3]. The blocklet addressing logic (LTRG, (G + 4)) is straightforward and requires four conventional ECL 10 K ICs the 10153, 10113, 10102 and 10136. Time offsets of eight or twelve samples, instead of four, can also be implemented thus allowing for refined discrimination of the pulses.

From a pure technological point of view, the circuit can be easily laid out on a printed circuit board and the small number of free running address lines, also GRAY coded, minimizes the digital noise.

4. 32-CHANNEL FASTBUS MODULE USING THE GATHER TECHNIQUE

The module described here is a double width FASTBUS unit housing 16 pairs of digitizing channels. The pairing of channels is designed to read out detectors with charge division. The GATHER logic is triggered by the analog sum of the pulses coming from one wire (see fig. 1).

The TRW TDC 1029 and its associated memory, two Fujitsu MBM 10422A-7, are laid on a 33 mm x 75 mm double sided minicard which plugs into a four layer FASTBUS mother board. Each pair of FADC minicards is driven from a subcard covering the other two (fig. 5), and holding the gain 7 preamplifiers plus the GATHER logic. The address logic, time memories, threshold and bias memory, together with the FASTBUS A/D line drivers, are located on the backplane side of the mother board as shown in fig. 6.

Fig. 5 Photograph showing two Flash ADC minicards together with the GATHER logic subcard.

Fig. 6 Photograph of the 32-channel mother board, two subcards are removed showing the modular construction.

The FASTBUS interface, placed on a board in the left hand station of the module, is the connecting link between the GATHER circuit and a FASTBUS segment. It contains circuitry for reading pulse height data as well as the associated time information of each wire. Offset and discriminator threshold values for each FADC channel are sent to or read from a separate memory on the GATHER circuit board.

The following FASTBUS functions (see fig. 7) are implemented: geographical address recognition, module identification in CSR # 0, secondary addressing mode for block transfer, SS-response for invalid address, busy and invalid command. Data are transferred as 16 bit words.

Fig. 7 FASTBUS interface logic.

The secondary addresses are:

- (1) 0 through 15: concatenated "left" and "right" pulse height data,
- (2) 16: time memory data,
- (3) 32: time register (time memory address plus GRAY address) and,
- (4) 64 through 127: thresholds and biases.

The time register, thresholds and biases are read/write. The pulse height memories and the time memory are considered as read-only FIFO registers.

Currently a modified ECL version of the coupler designed by G. FREMONT, CERN, EP Division, is used to evaluate the GATHER logic. Depending on the outcome of tests with experimental data, a TTL version using less power and space will be provided and, if desired, more features could be added.

The very good performance of the baseline cancellation is demonstrated by the computer outputs in fig. 8. Two pulses, 192 ns from each other are perfectly digitized with 4 prepulse samples even when they are only 2 LSBs above the pedestal. One can also notice some "ringing" on the first pulse and the exponential edges of the second (the latter is in fact the reflection of the first one at the open end of the input cable).

5. CONCLUSION

The above described pulse shape digitizer does not have the accuracy of CCDs [9] or the SLAC Microstore Analog Memory Unit [10]. It is designed for experiments with a large number of channels and significantly outperforms other designs on the grounds of memory time and sampling rate. It has now passed systematic laboratory tests and it will be evaluated on the prototype of the OPAL [11] central detector at CERN. The manufacturing cost should not exceed \$100 per channel and its modularity should minimize the maintenance problems.

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Fig. 8 Top: two ~ 17 count pulses as digitized by the GATHER circuit, note the "ringing" on the first pulse (right) and the exponential edges of the second one; Bottom: the same pulses attenuated to two counts above baseline.

Each channel can be accurately biased so that the pedestal is centered in one of the least significant bins. Fig. 9 shows three pedestal distributions for three equispaced bias settings. The histogram shapes are self explanatory and confirm the good performance of the FADC front end even when operated with an 8 bit dynamic range (1 LSB = 6 millivolts at the TDC 1029 input). The power dissipation does not exceed 5 Watts per channel.

Fig. 9 Three pedestal distributions for three equispaced bias settings.