ACQUISITION SYSTEM FOR THE HODOSCOPE SPECTROMETER GAMS-4000

IHEP¹ - IISN² - LANL³ - LAPP⁴

D. Alde³, F. Binon², D. Boget⁴, C. Bricman², S.V. Donskov¹,
G. Dromby⁴, J. Dufournaud⁴, P. Duteil⁵, M. Gouanère⁴,
V.A. Kachanov¹, D.B. Kakauridze¹, G.V. Khaustov¹, E. Knapp³,
C.D. Lac⁴, J.P. Lagnaux², A.A. Lednev¹, D. Michotte²,
Yu.V. Mikhailov¹, T. Mouthuy², J.P. Peigneux⁴, J. Potter³,
A. Possoz^{5*}, Yu.D. Prokoshkin¹, Yu.V. Rodnov¹, D. Sillou⁴,
J.P. Stroot², V.P. Sugonyaev¹

ABSTRACT

A data acquisition system with high amplitude resolution (12 bits), high speed conversion (clock frequency 50 MHz), used in an experiment with a large number of counters (~ 4200) is described. Physical quantities (masses and momentum transfer) are computed during data transmission itself, allowing improved trigger selectivity.

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1. Institute for High Energy Physics, Serpukhov, USSR
 2. Institut Interuniversitaire des Sciences Nucléaires, Brussels, Belgium
 3. Los Alamos National Laboratory, New Mexico, USA
 4. Laboratoire d'Annecy de Physique des Particules, France
 5. CERN, Geneva, Switzerland
 - *) Now at Enrico Fermi Inst. of Physics, University of Chicago, USA

1. INTRODUCTION

GAMS-4000 is a large photon (electron) detector installed in the North area of the SPS at CERN. It is essentially a lead-glass wall of nearly $2.5 \times 2.5 \text{ m}^2$, made of 4096 lead-glass cells ($38 \times 38 \times 450 \text{ mm}^3$) assembled in a 64×64 matrix.

Each high energy ($\geq 0.2 \text{ GeV}$) gamma ray (or electron) incident on the detector develops an electromagnetic shower inside the lead glass. The electrons and positrons from a shower emit Cerenkov light on their way through the glass, the amount of light being proportional to the energy of the incident gamma ray. Each lead-glass cell is viewed at one end by a photomultiplier tube which measures the intensity of the light emitted in that cell.

The width (38 mm) of each cell has been chosen to be of the same order as the lateral extension of the showers [as a result, at most 25 cells, (5×5) around the cell which contains the impact point of an incident photon, give a significant signal]. Thus by suitable summation of these signals it is possible to obtain the energy of the incident photon. Its coordinates can also be deduced, with a precision of the order of 1 mm, from the light distribution amongst the cells [1,2].

To achieve this, the signals delivered by the photomultipliers must be analysed in amplitude. The requirements on the amplitude analysis are rather stringent:

- (i) large dynamic range and good linearity. Therefore a gated charge-to-time converter (QTC) has been associated with each photomultiplier;
- (ii) fast conversion time, i.e. of the same order as the reading time, in order not to unduly block the system. This has led to the use of a 50 MHz clock for the time-to-digital conversion (TDC);
- (iii) good isolation against ground currents. After careful study of this problem, isolation by opto-coupler has been adopted.

Furthermore, an entirely new fast acquisition system has been developed. Its main characteristics are:

- (i) TDC data are transmitted as soon as the conversion is finished, even if some QTC are still in the conversion stage. This reduces to a minimum the dead time per event;
- (ii) pedestals are subtracted automatically and only meaningful results are further transmitted;
- (iii) simple hardware implemented algorithms allow calculation of physical quantities like the invariant mass and the transverse momentum of a physical system decaying to photons during the flow of data.

These points will now be considered one by one in more detail.

2. PRINCIPLE OF THE AMPLITUDE ANALYSIS

The photomultipliers (PM) used in GAMS are of the type FEU 84-3 (made in USSR), a 12 stage tube with a Venetian blind dynode structure. Details about voltage divider, gain tuning, etc. have been given elsewhere [3]. The signal delivered by the anode, measured on a $50\ \Omega$ load, shows good linearity for amplitudes not exceeding ~ 1.3 V.

The anode signal from each PM is transmitted through a 50 m long coaxial cable (type similar to RG 58-C/U) to its associated QTC circuit. This cable length provides the necessary delay to "make" the QTC gate signal from the trigger which is furnished by a suitable combination of signals given by beam counters. Due to the attenuation in the cable, a 1.3 V pulse on the anode is reduced to 0.8 V at the QTC input but, of course, the total charge in the pulse is conserved.

Thus, the largest pulse delivered at a QTC input, i.e. with the largest allowed amplitude compatible with PM gain linearity, has an amplitude (max) = 0.8 V, a rise time = 16 ns, a width = 30 ns (fwhm) and a full-width = 60 ns. This corresponds, in a $50\ \Omega$ load, to a maximum instantaneous current of 16 mA and to an integrated charge of ~ 500 pC.

The gated charge-to-time converter, which has been developed at our request, is the monolithic circuit MQT 200 from LeCroy Research Systems Co. Its output signal width is proportional to the input charge collected during the input gate time to a 0.025% accuracy. It has a standard full-scale sensitivity of 1000 pC and its full scale output width may be adjusted over a range between 50 μ s and 1 ms.

Each QTC is followed by a 12-bit scaler (49704 + SN74LS303 circuits). The output signal width from the QTC is measured by counting the number of pulses delivered by a 50 MHz quartz oscillator. If necessary, the scaler can be read several times as it is only reset at the beginning of the following event. The high frequency of the quartz oscillator allows the full dynamical range to be converted in $4096/(5 \times 10^7) = 82 \mu$ s.

3. CRATE ORGANISATION

The whole system consists of 11 EURONORM crates (but with a 280 mm depth). Each crate has 27 slots which, for the present application, have been divided into two parts, each half-slot leaving room for a 3 units height card.

24 slots are used for the charge-to-time converters and their associated scalers: the upper part is occupied by a printed board with 16 QTC mounted on it, while on the lower printed board are the 16 corresponding scalers and one 50 MHz quartz oscillator. The necessary electrical connections between upper and lower card are made by twisted pair wiring. The connection between a QTC and its corresponding scaler is made by opto-coupler. This layout insures good isolation between the analog and digital parts of the system thanks to the opto-couplers.

Thus, 24 slots in each crate are used for the analog-to-digital conversion part, each crate containing $24 \times 16 = 384$ electronic channels. Of the remaining half slots two are used for reset and triggering purposes, while the others are reserved for the crate controller.

4. CRATE CONTROLLER

Each crate controller gives access to the 384 scalers of the crate in a CAMAC addressing mode (Fig. 1). It contains also two sets of RAM memories:

- (a) a 384 x 9-bit RAM memory for the pedestals;
- (b) a 64 x 9-bit RAM memory for indirect addressing of a sample of cells, used for checking purposes.

Several functions are performed by the crate controller:

- (i) loading and reading of the pedestal memories;
- (ii) loading of the address of each cell or auto incrementation of this address at the next access;
- (iii) loading or reading of Δ , where Δ is a 4-bit constant value which takes into account the pedestal instabilities (see iv);
- (iv) reading of the content of the scalers, step by step or automatically in sequential mode, this last mode being commonly used during data taking. A comparator allows the information from channel i to be transferred only if the following condition is fulfilled:

$$\text{amplitude}(i) - \text{pedestal}(i) - \Delta > 0.$$

The CAMAC access to the crate controller is made by a CAMAC module (MIPCAM) designed to accept or deliver data in the form of 16-bit words. The crate controller can also be controlled in parallel by the MIPROC 16S processor (see below).

During acquisition, there is no CAMAC access to the controller. Therefore, the flow of data is controlled by a 2.2 MHz (450 ns/cycle) oscillator located in the crate controller itself, which is started by an "end of conversion" signal and stopped when the crate has been fully readout. The cards in each crate are looked at in a sequential mode, and data from a card are read and are further transmitted only if a signal "end of conversion" is received from that card. Thus the scan of some crates goes on eventhough QTCs are still in the conversion stage in other crates.

The data are sent to a "first in first out" buffer memory, or FIFO, through a fast bus of 24 bits (12 addressing bits, 12 data bits, plus two control lines, namely a "data valid" line to the FIFO and a "ready" line from the FIFO).

A block diagram of the complete system is given in Fig. 2.

5. FIFO BUFFERS

There are 11 FIFO modules, one for each crate of GAMS. Four FIFO buffers are mounted in a double CAMAC module. Each FIFO module may store up to 32 words of 24 bits. It can be loaded or read by standard CAMAC functions.

In general, the FIFO's will be read in parallel mode. Each event recorded by the GAMS detector usually contains between 2 to 10 gammas^(*), with a mean value of 5. An average of 10 to 12 cells are fired for each gamma, so that the mean number of "words" is ~ 60 , most of which ($\sim 75\%$) contain small amplitudes (less than 1/10 of the total energy). It follows that some FIFO's will be loaded very quickly after the beginning of an event with small amplitudes which can be read immediately by the computer while the conversion of higher amplitudes is still going on.

The FIFO modules can be read in three different ways which are, by increasing order of speed:

- (i) directly by CAMAC;
- (ii) by a MULTIPLEXER module (described below), controlled by CAMAC through a high speed bus;
- (iii) by direct memory access (DMA) to the MIPROC 16S fast micro-processor through the MULTIPLEXER module (100 ns/word minimum).

Priority arbitrations between the FIFO buffers are settled by a priority encoder. In view of the relatively large number of FIFO units,

(*) This is the case for the present experiment in which GAMS is used (NA12), i.e. in the study of neutral mesons M^0 decaying to photons (e.g.: π^0 , η , η' , ω , f , h ...) produced in the charge-exchange reaction $\pi^-p \rightarrow M^0n$.

this configuration has been preferred to a sequential access in order to obtain a reading time that is as short as possible. However the system can also be used in a sequential mode. Having scanned all GAMS channels, the sequential configuration is used to read some additional detectors like the guard system (set of 96 lead-glass counters surrounding the target), a hadron calorimeter, wire chambers, etc. Mixing of their addresses must be strictly avoided. For this purpose, one inhibit line connects the priority encoder with each device. It allows the output of the devices to be inhibited as long as the preceding ones have not been read.

6. THE MULTIPLEXER

This complex unit is mounted in a double CAMAC unit. It has several purposes:

- It provides the arbitration signals for access to the fast bus.
- It splits the 24-bit words from the FIFO's into two 12-bit parts (address and data) and transform them into two 16-bit words for DMA, including also a flag in the address word, characteristic of each device. It splits also each 24-bit word from the fast crate (see 11.2) into 2 x 16-bit words (1 word with the first 16 bits, the other with the remainder 8 bits and the fast crate flag).
- It generates a clock signal which controls the DMA and transmit the data in parallel to the MIPROC 16S and to the preprocessor.
- It controls the sequential reading of the various devices in the inhibit mode, and generates the interrupt for the floating point processor.
- It assures DMA to the MIPROC and direct access by CAMAC, each with its proper timing.

7. DATA NORMALISATION

The data transmitted to the preprocessor must be properly normalized before being processed to allow the computation of physically meaningful quantities. Therefore, the amplitude delivered by each lead-glass cell is multiplied by a coefficient which is determined in the calibration of GAMS

with electrons of known energy [4]. These coefficients are stored in a coefficient memory, which is a double CAMAC module, containing 4096x8-bit words, i.e. one coefficient for each cell of GAMS. Each coefficient is multiplied in this module by the corresponding data (amplitude minus pedestal) and the result is then transferred to the preprocessor.

8. PREPROCESSOR

The preprocessor is a set of multiplication and summation modules. It computes the five quantities (moments): $M^{(0)}$, $M_x^{(1)}$, $M_x^{(2)}$, $M_y^{(1)}$, $M_y^{(2)}$, later used by the processor (see below), which are defined by:

$$M_x^{(n)} = \sum_j \sum_i A_{ij} x_j^n$$

$$M_y^{(n)} = \sum_i \sum_j A_{ij} y_i^n$$

where A_{ij} is the amplitude measured by the cell located in the i^{th} line and j^{th} column of the GAMS matrix.

These calculations are performed in parallel while the data are transmitted. When all data have been transmitted, the contents of the adder and multiplier accumulators are converted to floating point format and are transmitted to the processor.

Each multiplier and adder is built in a double CAMAC unit. There are two multipliers (one which computes $A_{ij} x_j$ and $A_{ij} x_j^2$, the other $A_{ij} y_i$ and $A_{ij} y_i^2$) and three adders (which computes $M^{(0)}$, $M_x^{(1)}$ and $M_x^{(2)}$, $M_y^{(1)}$ and $M_y^{(2)}$ respectively) in total.

9. FLOATING POINT PROCESSOR:

The floating point processor computes the physical quantities [2]:

$$p_t^2 = K \cdot [M_x^{(1)^2} + M_y^{(1)^2}] \quad (\text{transverse momentum squared})$$

$$m^2 = K \cdot [(M_x^{(2)} + M_y^{(2)}) * M^{(0)}] - p_t^2 \quad (\approx \text{invariant mass squared})$$

and compares the results with some predefined limits which depend on the kind of problem which is studied. An interrupt is sent to the MIPROC 16S, at the end of the calculation, if the data should be rejected. If the data

are accepted, the processor transfers the computed numbers $M^{(0)}$, $M_x^{(1)}$, $M_x^{(2)}$, $M_y^{(1)}$, $M_y^{(2)}$ as well as p_t^2 and m^2 for later checking purposes.

TTL-S technology has been used for the processor. Multiplications are done by using base 2 logarithms contained in ROM memories. About 200 ns are necessary for one multiplication.

The microprogram word is 40 bits long. The size of the memory is 256 x 40 bits, of which 32 x 40 bits are RAM memories used for program debugging. It contains also 16 registers of 16 bits.

The accuracy of the calculations is 1 part in 128 which is sufficient to fix the cuts on p_t^2 and m^2 .

10. MICROPROCESSOR "MIPROC 16S"

The "MIPROC 16S" (trade name from PLESSEY) is a 16-bit microprocessor with a 250 ns instruction cycle in TTL-S technology. The essential features of this processor are:

- 16 K-words of program memory and 64 K-words of data memory used for data acquisition;
- 2 DMA channels: DMA1 for data acquisition up to a maximum rate of 10 million words per second; DMA2 for data transfer to the PDP 11/70 which then writes the data onto magnetic tapes;
- 1 parallel interface to the crate-controllers;
- 1 serial interface for program transfer from the PDP 11/70.

The essential purposes of this microprocessor are:

- (i) to read, load and control the pedestals in the crate controller;
- (ii) to receive and interpret interrupt signals sent from different sources during data acquisition and to ensure the suitable branching;
- (iii) to receive data through the DMA1 channel and to fill buffers up to a maximum size of 4 K-words of 16 bits which are then dumped into the PDP 11/70;

- (iv) to reset the event when it receives an interrupt from the floating point processor, i.e. when the computed physical parameters are found outside their predefined range.

11. EVENT TIMING

11.1 Crate timing (Fig. 3)

Once the fast decision logic has recognized a good event it delivers, at a time taken as $t = 0$, a trigger signal which, after a suitable delay, opens the QTC gates during 60 ns in order to collect the charge delivered by the PMs. At time $t = 150$ ns a signal is sent which resets all scalers and crate controllers (C.C.). At time $t \approx 200$ ns (internal QTC delay) each QTC gives an output signal whose width is proportional to the charge delivered by the corresponding PM. The proportionality constant has been chosen such that a ~ 600 pC charge corresponds to the full scale of the scalers (12 bits = 4095). This signal enables the associated scaler to count the number of pulses generated by the 50 MHz clock on the scaler card (cf. Fig. 1), i.e. the scaler conversion takes 82 μ s at most. The QTC pedestals normally have a value which corresponds to ~ 150 scaler counts, i.e. the minimum conversion time is ~ 3 μ s.

At the C.C. reset, the address register points to the first card of the crate at the scaler sub-address 0. As soon as all scalers on the first card have finished counting, an "end of conversion" signal is sent to the C.C. which starts its 2.2 MHz (450 ns/cycle) clock controlling the sequential reading of the scalers on that card. The contents of each scaler are read by the C.C. arithmetic unit which subtracts the corresponding pedestal, previously stored in the pedestal memory. The result is compared with Δ (4-bit max. value) and it is finally transferred to the FIFO buffer, together with the corresponding address, only if $\text{amplitude}(i) - \text{pedestal}(i)$ is larger than Δ .

When all scalers on a card have been read, the C.C. address register points to the next card at sub-address 0. This card is then read in its turn unless either the conversion of the corresponding QTC signals is not yet finished or the FIFO buffer is full in which cases the C.C. clock is stopped until an "end of conversion" signal is received from the card and/or a "ready" signal is sent by the FIFO buffer.

Taking as an example a rather "large" event with 8 gammas (cf. § 5), which corresponds to ~ 100 fired cells of which ~ 25 give large amplitudes, it is easy to understand that of the 384 QTC in each of the 11 crates only few will give a signal large enough to be further transmitted to their corresponding FIFO buffer and, since each of them may store up to 32 words, that the data flow in each crate up to the FIFO goes on essentially at the pace of the C.C. clock. Therefore, the minimum time needed to read a crate is $\sim 384 \times 450 \text{ ns} + 3 \text{ } \mu\text{s}$ (necessary time to convert the pedestals on the first card) which is equal to $\sim 180 \text{ } \mu\text{s}$. The maximum time needed to read a crate is $384 \times 450 \text{ ns} + 82 \text{ } \mu\text{s} \approx 260 \text{ } \mu\text{s}$ which happens when a maximum signal (4095 counts) has been registered by a scaler located on the first card in the crate.

11.2 FIFO to processor timing (Fig. 4)

In principle, data stored in the FIFO buffers could be immediately transmitted further but, in practice, this transfer starts $30 \text{ } \mu\text{s}$ after the beginning of the event as this time is used to read a fast CAMAC crate (cycle $\sim 300 \text{ ns}$) through the multiplexer. This crate contains scalers and input registers which can be read only.

After the reading of the fast crate starts the scanning of the FIFO buffers by the multiplexer at a rate given by its internal 2.85 MHz (350 ns/cycle) clock. Three clock cycles are necessary to handle the first FIFO word: the first one is used for priority arbitration, the second sends a 16-bit word, made of the first 12 bits (data) of the FIFO word, to the MIPROC and the 24 bits to the preprocessor, the third cycle sends a second 16-bit word, made with the last 12 bits (address) plus a device flag, to the MIPROC. If the next data are in continuous succession, only two clock cycles are necessary to read them (the last two). If there is an interruption in the data flow, three clock cycles are again necessary to restart the reading. Thus $\leq 1 \text{ } \mu\text{s}$ is necessary to read one FIFO word. Coming back to our example given above, one sees that it takes $\sim 100 \text{ } \mu\text{s}$ to store the information corresponding to a 8 gammas event in the MIPROC but, as this is done in parallel with the scanning of the crates by the C.C., the average time necessary to read an event is essentially fixed by the time needed to scan the crates, i.e. $\sim 200 \text{ } \mu\text{s}$.

11.3 Complete event timing (Fig. 5)

As soon as all FIFO's have been read, the floating point processor is started which transforms the five quantities $M^{(0)}$, $M_x^{(1)}$, $M_y^{(1)}$, $M_x^{(2)}$, $M_y^{(2)}$, stored in the preprocessor adders, into 24-bit floating-point words and saves them in an internal memory. Immediately after they are transferred to the multiplexer which transforms them into 2 x 16-bit words which are then sent to the MIPROC. This takes about 10 μ s.

The next 20 μ s are used by the floating point processor to compute p_t^2 and m^2 and to decide whether the event is good or not. In the former case it takes 30 μ s for the MIPROC acquisition program to set the event header, to compute the event length and to construct the event table.

12. TESTING PROCEDURES

The good functioning of such a complex data acquisition system needs to be regularly checked. A systematic check of ~ 4500 electronic channels can only be done by computer. The special interface unit MIPCAM (cf 4.) allows a direct dialogue between the PDP11/70 and the ADC crates in a Camac way through the ADC control bus. Dedicated programs have been written which execute automatically some well defined test procedures.

One program essentially checks the digital part of the crate electronics, i.e. the scalers and the C.C. (see Fig. 1). For example, it opens the gate of the scalers during a predetermined time and counts the number of clock pulses during that time. If the number of counts differs by more than one from the nominal value, an error message is delivered. It allows also to measure the pedestals of the ADC and their fluctuations. It gives an error message if they fall outside some predefined range. (A variant of this program makes essentially the same tests but it reads the crates through the whole acquisition system, i.e. FIFO buffers, preprocessor, floating point processor, multiplexer and MIPROC).

Another program tests the complete electronic channels, starting at the test input of the PM voltage dividers [3]. Therefore, a high voltage pulse (200 V max) is applied on the PM anode through a 10 K Ω resistor in parallel with the 50 Ω cable impedance matching resistor (on the QTC card). This pulse is provided by a specially made Camac unit which selects and

feeds all 64 dividers in one column of GAMS at a time. The pulse height is controlled by a DAC circuit. It can be varied between 0 V and 200 V in 256 equal steps. This procedure permits in particular to check the linearity of the ADC.

A third program tests the entire GAMS detector system. It makes use of the light calibration system of GAMS, namely a flash lamp whose light is distributed to all GAMS cells by optical fibers [3]. This program triggers the lamp and reads the amplitudes measured in all or part of the cells of GAMS. It can also be used to tune the gain of each photomultiplier [3].

13. CONCLUSION

A fast compact modular acquisition system with more than 4,000 12-bit ADC channels has been developed. Because the ADC pedestals are subtracted from the data by the crate controllers themselves, only meaningful data are further handled, the number of channels to be taken into account is immediately reduced by a factor 30-40 (depending on the kind of experiment performed: see note p.6). The maximum acquisition rate is ~ 3500 events/s for events with up to a few tens fired counters.

A wired preprocessor and floating point processor compute significant physical quantities while the data are flowing through the system. Fast tests can be made on these computed parameters in order to reject unwanted events before they are written onto magnetic tape, greatly reducing the number of tapes to be handled later in the off-line analysis.

This system has been in use since 1982 in the NA-12 experiment at CERN and a similar, but smaller, system [5] has been in use in a "sister" experiment at IHEP, for the last five years. Both systems have shown very good reliability since the beginning of their functioning.

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FIGURE CAPTIONS

- Fig. 1 Crate data flow diagram.
- Fig. 2 GAMS-4000 data acquisition system.
- Fig. 3 Crate timing.
- Fig. 4 FIFO to MIPROC timing.
- Fig. 5 Event timing.

Fig. 1

Fig. 2

Fig. 3

Fig. 4

Fig. 5