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Ongoing electronic development in the CERN Beam Instrumentation Group: challenges and solutions for the measurement of particle accelerator beam parameters.

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ABSTRACT: The Beam Instrumentation Group (BI) is responsible for designing, building and maintaining the instruments that allow observation of the particle beams and the measurement of related parameters for all CERN accelerators and transfer lines. This contribution is aimed to give an overview of the ongoing electronic developments within the beam instrumentation group both to improve the performances and ease the maintenance of instrumentation in the existing machines and to meet the requirements of future accelerators. Details on some of the challenges and proposed technical solutions will be presented.

KEYWORDS: Modular electronics; Front-end electronics for detector readout; Data acquisition concepts; Beam-line instrumentation (beam position and profile monitors; beam-intensity monitors; bunch length monitors)

¹On behalf of the beam instrumentation group.

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1 The beam instrumentation group (BI)

The Beam Instrumentation Group (BI) is responsible for designing, building and maintaining the instruments that allow observation of the particle beams and the measurement of related parameters for all CERN accelerators and transfer lines.

The CERN accelerator complex comprises ultra-relativistic and non machines, circular and linear accelerators and even an antiproton decelerator. The characteristic of those machines are so different that rarely the same instrument can be deployed on several of them.

Typical beam parameters to be measured and monitored are:

- beam position
- beam loss
- tune and chromaticity
- luminosity
- transfer line to accelerator injection point matching

- beam intensity (bunch charge and total current)
- beam profiles (transverse and longitudinal).

A first step toward standardization of the BI instrumentation has been done in the software section with the development of the Front End Software Architecture (FESA) [4]. The aim of the project was to give a common infrastructure to all the SW developers and a common interface to the end users. The project is now maintained by the control group and has been further developed to include tools for the automated generation of drivers and memory mapping.

A similar approach has been tried for the interfacing between the front end software and the digital acquisition systems: for the Large Hadron Collider (LHC) instrumentation BI decided to use a VME carrier, the DAB64x developed in collaboration with Triumph, as base of its digital acquisition systems. The DAB64x is a generic VME acquisition board based on FPGAs that is customized with pluggable modules (mezzanines) to adapt to the different front-end electronics.

The use of a common carrier has several advantages for a group like BI: it allows to share spares between different systems, it reduces the risks linked to new HW developments minimizing the complexity of new PCBs, allow the reuse of already developed firmware modules and provides a more standard interface to the software developers. The adoption of the DAB64x was successful and it is now used in several system: beam position monitors (BPM), beam loss monitors (BLM), beam current transformers (BCT), luminosity monitors, abort gap monitor, tune and chromaticity monitors.

In the following sections of this paper are presented the new BI standard carrier, the VME FMC carrier (VFC), and 3 ongoing developments, 2 of which are already using the VFC.

2 The new BI carrier: the VME FMC Carrier (VFC)

The DAB64x was successfully employed in many instruments, but most of its components are now obsolete. BI decided for this reason to develop a new carrier, this time in collaboration with the CERN control group (CO) and in the framework of the open hardware project (<http://www.ohwr.org/>).

The new carrier, the VME FMC Carrier (VFC), has the following characteristics:

- VME64x interface
- 2 small form factor pluggable (SFP) on the front panel
- 2 FPGAs, one dedicated to system functions and common to all the projects, and one fully dedicated to the specific application
- flexible clocking including a SPI programmable oscillator, 2 voltage controlled ones and low jitter PLLs
- 2 FPGA Mezzanine Card (FMC) slots
- pluggable Rear Transition Module on the P2 with 40 straight connection from the Application FPGA and 2 differential clocks from low jitter PLLs

Figure 1. The new BI standard carrier: the Vme FMC Carrier (VFC).

- 2 SRAM memory for the processing on the Application side and a DDR3 for the stocking of results on the System side.

2.1 Why VME again

The beam instrumentation group decided to keep VME as standard for the VFC mostly because of the amount of crates already installed and because it still satisfies all the requirements.

The drawback of the VME standard compared with the new emerging ones in the high energy physic community, like the uTCA one, is the lack of high bandwidth communication among the boards in the crate, but none of the identified new projects would require such capabilities.

The VFC is equipped, in addition to the VME bus, with 2 SFPs on the front panel. One is foreseen for beam synchronous timing distribution while the other is free and can be used to implement communication protocols, like TCP/IP for example, making the board capable of working out of a crate in case of highly distributed systems.

2.2 The split between system and application FPGAs

The VFC has 2 FPGAs as mentioned earlier: one dedicated to system functions (the SFPGA) and the other fully available to designers for their applications (the AFPGA). The communication

between the 2 FPGAs is implemented via 4×2.5 Gbit channels and some low speed communication lines.

From a firmware developer point of view this has the advantage of removing the need to include in the application specific design the system functionalities like the VME interface or the control of the PLLs. From a SW developer point of view this has the advantage that all the common interface are identical and mapped in the same space for all the applications. The price for this is latency on the VME accesses as they go through a serializer.

The last advantage of this architecture is the possibility to change the application FPGA configuration without any risk of losing the access to the VFC in case of errors during the programming phase as the SFPGA is never touched.

The WishBone (WB) bus has been chosen as internal interconnection infrastructure for the firmware modules. The access to the Application FPGA from VME or from the communication SFP is granted via a WB serializer implemented using 2 2.5 Gbs channels. WB is an open standard and is used as interface by several OpenCores (<http://opencores.org/>) modules. This improves once again reusability and access to pre-developed functions.

2.3 The FMC mezzanines

The DAB64x was using a custom mezzanine format, while for the VFC BI decided to adopt a VITA standard: the FPGA Mezzanine Card (FMC) also known as VITA-57. The use of a standard mezzanine format opens the door to commercial modules and leaves the possibility to reuse the designed mezzanine on other carriers than the VFC if needed, improving the reusability of designs and portability.

The FMC standard defines 2 connector types: the Low Pin Count (LPC) and the High Pin Count (HPC). The HPC, as the name suggests, has more connections than the LPC, but geometrically they are identical and a LPC mezzanine can be plugged on a HPC carrier. The VFC mounts HPC connectors but implements fully only the LPC connections. The Gbit links and the dedicated clock lines, coming from low jitter PLLs, are the only features of the HPC pin definition implemented.

3 The new Multi Orbit POsition System (MOPOS) project

The Super Proton Synchrotron (SPS) is the last element of the LHC injector chain but also provides beam for the Gran Sasso experiment on neutrinos and for fixed target experiments. The MOPOS is the new SPS beam position monitoring system and is foreseen to be installed in 2013.

3.1 System requirements

The beam position is measured with electrodes placed in couples on the opposite sides of the beam pipe. The closer the beam passes to an electrode the higher the amplitude of the induced signal on it. In first approximation the position of the beam is measured computing the ratio of the amplitudes of the signals on the opposite electrodes.

It is important to note that the signal induced on each electrode is not only a function of the distance of the beam from the electrode itself, but also of the beam current and the particles longitudinal distribution. The SPS, as mentioned, serves many different users, each with different beam type and also accelerated species. The front-end electronics as a consequence of this variability has

Figure 2. The FMC mezzanine developed for the MOPOS and compatible with the Matching monitor requirements.

to deal with signals going from 40 mVpp, for ion beams at injection, to 580 Vpp, for the nominal LHC bunches at ejection.

The required resolution is expressed in terms of aperture and is therefore independent on the signal intensity, leading to a required equivalent signal resolution of 200 μ V for ions at injection.

Pickups are distributed all around the circumference of the SPS. In some cases the distance between the measuring point and the crate areas is 1.5 km. For this reason, seen the high resolution required from the system, the front-end electronics must be placed close to the pickups, in zones where the expected total dose over 10 years of operation is 100 krad. Compared to the expected dose in the inner trackers of the LHC experiments this is very low, nevertheless all the components need to be qualified in terms of radiation tolerance. The low number of systems, 240, and the expected dose would not justify dedicated ASIC development and for the system it was decided to use Components Off-The-Shelf (COTS).

3.2 System architecture

The analog front-end electronics consists of band pass filters followed by logarithmic amplifiers and finally a differential stage. The output of the analog section is already an estimation of the position as $\text{Log}(A) - \text{Log}(B)$, where A and B are the signals from opposite electrodes.

The use of Logarithmic amplifiers not only allows to extract the position directly in the analog part of the chain, but also compresses the signals so that the whole dynamic range can be covered without the use of amplification stages with programmable gain. A switching mechanism had nevertheless to be implemented for the input band pass filters: the longitudinal distribution of the particles, and therefore the frequency spectra of the signal, varies too much from user to user in the SPS and a single band could not efficiently cover the whole range and suppress enough the noise.

The output of the differential amplifier, together with the sum of the signals from the 4 electrodes, is digitized with a 10 Msps 14 bit ADC and then packed and, time tagged with the turn number, sent to the back-end over a Gbit connection using an FPGA. The use of a programmable

Figure 3. The 3 boards used to test the FE architecture of the MOPOS. From left to right: the analog block with the filters and amplifiers, the ADC evaluation board and the communication board. In the final system, once chosen the ADC, those three modules will be implemented in a single PCB.

device is always to be carefully evaluated in an environment subject to radiation. The total dose is not expected to be a real issue in view of the level and the tolerance of the modern technologies, but the SEU rate could be a problem and therefore the logic in this FPGA is kept to the minimum, with all the processing performed in the back-end. Dedicated radiation tests are planned to estimate the expected failures per run due to SEU.

The back-end electronics consists of a VFC equipped with 2 FMC mezzanines. Each mezzanine has 2 SFPs connected to the Gbit lines of the connector for a total of 4 front-ends per carrier.

3.3 Project status

The back-end electronics is in an advanced status: the FMC mezzanine has been designed and tested on a VFC and a first version of the firmware has been deployed on a laboratory setup.

The front-end electronic is still in a prototyping phase.

A PCB with the front-end filters and the logarithmic amplifiers has been developed and qualified under radiation up to 100 krad. The performed tests proved that the Logarithmic amplifiers and the ADC drivers don't suffer of any noticeable degradation after irradiation. All the tested voltage dividers suffered as expected a drift of their output voltage after radiation, nevertheless 2 chips are compatible with the system requirements: the LT1963-KTT and the TPS7A4501KTT.

The ADC has still to be selected but there is already a list of possible candidates. An evaluation board is being used to perform the tests of the rest of the modules.

A PCB with a SPARTAN6 and 4 SFP has been designed and tested to assess the performances of the communication protocol and of the tagging with beam synchronous timing. This module has to be qualified for total dose and the SEU rate estimated, but a suitable SFP has been already identified after tests under radiation: the FFT-FT3A05D.

4 Matching monitor

A beam injected in an accelerator from a transfer line whose beam-line's parameters are not matched to those of the injection point results in oscillations of the beam cross section. Those oscillations are self dumped toward a bigger emittance.

Figure 4. The linear CMOS plugged on its PCB. The enclosure has a round opening designed to accommodate a lens and give the possibility to micro adjust its centering.

The role of the Matching Monitor is to verify the proper matching observing the transverse profile of the beam during the first turns after the injection. This is achieved in the LHC and SPS using Optical Transition screens to image the beam [5].

4.1 System requirements and architecture

The matching monitor imaging sensor needs only few tens of pixels to accommodate the position oscillations and achieve a sufficient resolution for the size ones, but must be capable of acquiring at the revolution frequency which is about 11 kHz in the LHC and 44 kHz in the SPS. Such a high frame rate can be achieved either by expensive fast cameras or by linear (mono-dimensional) pixel sensor observing separately the horizontal and vertical movements. It is the second option that has been chosen for the Matching monitor. The optical line designed for this detector uses cylindrical lenses to achieve different magnification in the 2 planes. The aim is to squeeze one of the two dimensions of the beam image in the height of a single pixel to decouple the actual size oscillations in the observed plane from position oscillations in the perpendicular one.

Figure 5. The Front end board of the Matching with its mechanical enclosure.

Figure 6. Profiles acquired with the Matching monitor in the LHC. Both size and position oscillations are visible.

The chosen sensor is from Hamamatsu: the S11105. It has 512 pixels and a pixel readout clock of up to 50 MHz. The actual readout clock used is a 40 MHz one, the same used to clock the ADC, the AD41240 [7], and the serializer, the Gigabit Optical Link (GOL) [6]. Those both chips are ASICs developed for LHC experiments and rad tolerant by design.

The sensor is the most sensitive element to radiation, but is not a major contributor to the system cost and can be easily replaced as it is sitting on a socket. In addition the system is used only during machine setup time and the front end can be removed while not used.

The serialized data stream is sent over an optical link to the backend, that is identical to that of the MOPOS except for the AFPGA firmware.

4.2 Project status

The system is in a prototyping phase, but all the electronic modules and optical lines have been developed and installed. In particular the LHC system has been already tested with beam. The SPS system was also recently installed but is still under test.

Figure 7. The custom crate designed for the BLMs equipped with 2 front end boards.

5 The new BLM system for the LHC injector chain

The characteristic of the accelerators constituting the injectors chain of the LHC are very variegated and many different types of detectors are used to monitor the beam losses in those machines. The aim of the new BLM system is to improve the performances but also to use the same front-end and back-end for all of them.

5.1 System requirements and architecture

The system, having to cope with many different type of detectors, is required to be able to measure currents of positive and negative polarity.

The dynamic range that the front end needs to cover is 146 dB, going from 10 pA for slow losses to 200 mA for fast events. To cover such wide dynamic range 2 measuring techniques are used on the same front-end. The higher currents, ranging from 100 μ A to 200 mA, are measured sampling the voltage drop on a shunt, while to measure the lower range currents, from 10 pA down to 10 mA, it has been designed a fully differential frequency converter. The selection of the proper measuring technique for the actual signal range is performed in an automated way by an FPGA sitting on the front-end board.

The fully differential frequency converter is an improved version of the traditional current to frequency converter scheme. In this new configuration the integrator is a differential one with one input connected to ground and the other to the source. Every time one of the 2 outputs of the integrator reaches a programmable threshold, the input connections are swapped using switches resulting in a saw tooth signal on each integrating output. This method is not affected by dead times and the measure does not depend on the polarity of the input signal. The residual of the voltage ramp at the output of the integrator is sampled at the end of a measuring period to further improve the resolution.

The front-end electronics is sitting in 6U boards designed to be plugged in a custom crate [2]. Each board can serve up to 8 detectors. The inputs from the detectors are routed on the backplane,

Figure 8. The results of the tests on one of the front end modules for the 2 working regimes. On the axes the measured current and the relative error with respect to the injected one.

that has been designed to maximize isolation between channels and to minimize possible interferences. On the front panel of the boards are 8 monitoring output, one per channel, and 2 SFP for data communication and system configuration via TCP/IP.

The onboard FPGA continuously monitor the functionality and working condition of each channel and power supply. Any possible malfunction is signaled immediately after its detection to the back-end and control system. The malfunctioning channels can be shut down and isolated to prevent them from affecting the others, making the system single channel fault tolerant.

The back-end is based on a mezzanine equipped with 2 SFPs and an FPGA mirroring the communication part of the front-end board. The carrier board for this mezzanine is a DAB64x.

5.2 Project status

The front-end board and the back-end mezzanine have been already produced and the firmware is being finalized. The first preliminary tests in the lab show that the performances meet the requirements [1].

The crate is still a prototype: the backplane is the final one, but a more advanced crate controller is being designed.

6 Conclusions

The projects presented in this paper are quite representative of the challenges BI is confronted with and the strategy the group is adopting.

The design of the VFC, aimed to be the standard platform for the digital designs in the group, is part of the group policy for standardization and reusability. This strategy is well integrated in the MOPOS and Matching monitor that shares exactly the same back-end. Those two project also share a common problem in BI: the need to install the front end electronics in zones subject to radiation. The design of ASICs is not common in BI, and for both projects alternative solutions had to be chosen: the use of already designed rad-hard ASICs in the case of the Matching monitor, and hence the great interest of BI in keeping a collaboration with the developers of the electronics for the experiments, and a campaign of qualification of COTS in the case of the MOPOS.

A very high dynamic range is quite typical in the BI instrumentation as illustrated by the MOPOS and the BLM system described. In the latest the specifications were such that it was

necessary to develop new strategies and also to develop a new type of crate and backplane to meet them. In parallel to this project a new BLM ASICs [3] , sharing the same strategies, is being developed for the LHC system.

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