Upgrade Analog Readout and Digitizing System for ATLAS TileCal Demonstrator

Fukun Tang
On Behalf of the ATLAS Tile Calorimeter Group
The University of Chicago

1. Motivation & Objectives
2. Overview of Tile Calorimeter Readout System at LHC
3. TileCal Upgrade Electronics in Demonstrator
4. Summary & Plans
LHC upgrade program aims at 5-10 fold luminosity increase, higher radiation tolerance required for the on-detector electronics.

Higher event rates require more efficient trigger algorithms

Aging electronics → the present system was designed in 90s, originally planned operation time is ~10 years.

Currently digitized data stored on the detector, readout only for Level-1 triggered events

Completed re-design of TileCal electronics for upgrade in 2022. (Phase II)

Upgraded electronics should transfer all digitized data off the detector

Fully digital trigger with higher selectivity possible

Implementing Demonstrator readout system in 2014

- Discover and solve issues for the new designs
- Gain field experience for Phase II upgrade
- Evaluate digital trigger capability
- Compare performance of analog and digital in real time
• 256 TileCal detector modules and electronics drawers
• Process ~10,000 PMT signals
• 16-bit dynamic range with bi-gain readout channels covering an energy range of 30MeV to 2Tev
• 40Msps continuous digitization
• Analog trigger
• Cesium, laser and electronic calibrations
• TTC trigger/timing/controls
• 2x redundant data transferring to off-detector
Electronics in a drawer:
- Up to 45 PMT Blocks with HV bases
- Up to 45 3-in1 cards (Front-end board)
- 4 mother boards
- 8 digitizer boards
- one optical interface board
- one TTC receiver mezzanine card
- up to 10 analog summing mezzanine cards
- one integrator readout board (CANbus)
- HVPS and distribution boards
- LVPS and distribution and sense adapters
The present a single drawer electronics to process up to 45 PMT signals

- The highest-pT jet with pT of 1.5 TeV collected in 2011
- The two leading jets are central high-pT jets with an invariant mass of 2.8 TeV
- (pT, y) of (1.5 TeV, -0.58) and (1.0 TeV, 0.44), respectively
- The missing ET in the event is 310 GeV
3 optional front-end readout boards in development
- Shaper + bi-gain + slow integrator, developed by The University of Chicago, USA
- FATALIC ASIC chip, developed by University of Clermont-Ferrand, France
- QIE ASIC chip, developed by Argonne National Laboratory and Fermilab, USA

Demonstrator electronics
- Adapted front-end electronics developed by University of Chicago
- Raw data from each channel to off-detector sROD
- Mixed Analog and Digital Level-1 trigger
A Demonstrator Electronics Drawer

1. 48 PMT blocks with FE electronics and HV distribution electronics
2. 4 identical Main Boards
   - 24-ch digitizers for low/high gain channels of 12 PMTs
   - Sampling phase adjustment for digitizers
   - Slow controls (calibration, Integrator gain settings, ADC input bias settings, status monitoring etc.)
3. 4 identical Daughter Boards
   - Concentrate data and control Main Board
   - 4-QSFP+ transmit data to and interface off-detector sRODs
   - Of 2 downstream links of QSFP+ (in redundancy) are used in GBTx protocol to send TTC information to on-detector electronics

Alternative readout chips of FATALIC or QIE are also in development by Clermont-Ferrand and ANL & Fermilab.
TileCal Analog Front-end Electronics For Demonstrator

(1) Fast signal processing
- 7-pole LC shaper and bi-gain clamping amplifiers with gain ratio of 32

(2) Slow signal processing
- 6-gain integrator for Cs calibration and monitoring minimum bias current of proton-proton collisions

(3) Charge injection calibration and controls

(4) Retain analog trigger capability for Demonstrator
Readout Linearity Improvement

Low Gain Channel

High Gain Channel

- 3-in-1 Card
- Analog Front-end Board

ADC Counts (kE3)

Linear Fit - Data (counts)

0.0pC 400pC 800pC

0.0pC 400pC 800pC

0.0pC 400pC 800pC

0.0pC 400pC 800pC
Readout Noise Improvement

Low Gain Channel RMS Noise

3-in-1 Card

Analog Front-end Board

High Gain Channel RMS Noise

3-in-1 Card

Analog Front-end Board
TileCal Data Digitization and Data Acquisition System (1 of 2 Sections)

- PMT
- FE Board
- Main Board
- Daughter Board
- sROD

**PMT**
- Shaper
- Integrator charge injection

**Main Board**
- Shaper
- Integrator charge injection
- ADC logain
- ADC higain
- 3-ch Integrator ADCs

**Daughter Board**
- FPGA0
  - Control Timing etc.
  - SPI bus
  - 6-ch ADC Serial bus
- FPGA1
  - Control Timing etc.
  - SPI bus
  - 6-ch ADC Serial bus

**Main Board**
- FPGA Data Organizer
  - Control Timing & House Keeping etc.
  - SPI bus
  - 6-ch ADC Serial bus

**5 voltages in 9 loads from +10V**
A Single PMT Readout Data Flow

Front-end Board (3-in-1)

- Analog low gain
- Analog high gain
- Analog Integrator

PMT

Σ1
Σ2
Σ9

Analog Summing Board

12-bit 40Msps ADC (low gain)
12-bit 40Mbps ADC (hi gain)

ADC Input Bias Settings

FPGA (Cyclone IV)

16-bit SAR ADC

Slow Signal Processing

Fast Signal Processing

Analog Trigger Tower Output

2-ch ADC Serial Bus

LG ADC data (560Mbps)
HG ADC data (560Mbps)
Data frame (280MHz)
Data clock (40MHz)

Integrator ADC I²C Bus

16-bit SAR ADC

16-bit SAR ADC

Spi Bus & Timing

FEB Control Bus

To other 2 Front-end Boards

Analog Trigger

Σ1
Σ2
Σ9
Main Board & Layout

- **6** signal layers
- **8** power layers including **3** redundant ground layers (continuous solid plane) for signal integrity and tandem crosstalk reduction

**Complexity and Challenges:**
- **High speed:** (560 Mbps)
- **Max. trace length:** (20 inches)
- All routes are basically in same direction
- Crosstalk consideration: (parallel and tandem)
- **Mixed signals** (low noise analog and high speed digital)
- Equal timing high speed traces
- Current rate constraints for supplies
- Avoid **Swish-cheesed power planes** (via usage limitation)
- Many other challenges to suppress DC/DC switchers noise

**Exposure in higher radiation**
- **6** signal layers
- **8** power layers including **3** redundant ground layers (continuous solid plane) for signal integrity and tandem crosstalk reduction
Daughter Board Development

- Daughter Board development is at Stockholm University
- First prototype manufactured and tested in 2011 with SNAP-12
- Second prototype manufactured in 2012 with both SNAP-12 and QSFP+ placed
  ✔ Testing and evaluation in final phase
- Third prototype with QSFP+ only is in development

Diagram of second prototyping board

Kept SNAP-12 on for radiation evaluation in 2\textsuperscript{nd} prototype, but no longer used in 3\textsuperscript{rd} generation Daughter Board
In-System FPGA Configuration

- 2x redundant QSFP+ data transmission (80Gbps per Daughter Board) in 3rd prototype board
- Adaptable programming structure that allows cross-FPGA reprogramming if necessary (using before GBTx available)
- Enabling the GBTx JTAG connections by resistors or jumpers on the board
- Extended Daughter Board/Main Board JTAG programming chains

Diagram of 3rd prototyping Daughter Board
Super Readout Driver AMC

sROD in Demonstrator
- PMT readout for 4 Mini Drawers, supporting up to 45 PMTs
- Data concentration and processing (pipeline memories, reconstruction,...)
- TTC signals distribution & DCS management
- L0/L1 Calo functionality

sROD data reconstruction
- Merge Demonstrator data with other 7 drawers in present system for data reconstruction
- Synchronized with the TTC system
- Provide digital trigger information for evaluation
Double mid-size AMC will be ready in mid-November 2013 for testing

- Plugged in a ATCA carrier or in a µTCA platform
- Sized 180.6 mm x 148.5 mm
- Gigabit communication with carrier/other AMCs
- ATCA test bench installed in building 175 at CERN
Demonstrator System Testing Setups

One of 4 testing setups for the prototyping Demonstrator at University of Chicago
Summary & Acknowledge

• Analog Front-end Board passed performance and radiation tests in 2012, it well meets the requirements both in operation and radhard.
• Main Board, Daughter Board, sROD, LVPS, HVPS performance and radiation tests are planned in 2013-2014
• Demonstrator insertion (one drawer) is scheduled in 2014
• Phase II System Upgrade in 2018-2020

Authors contributed to this presentation:
K. Anderson, K. Hildebrand and M. Oreglia (The University of Chicago)
H. Akerstedt, C. Bohm and S. Muschter (Stockholm University)
G. Drake and A. Paramonov (Argonne National Laboratory)
A. Biot and F. Carrio (University of Valencia)

We wish to take this opportunity to extend our sincere thanks to all participants in the TileCal Demonstrator project.