Upgrade Analog Readout and Digitizing System for ATLAS TileCal Demonstrator

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Motivation & Objectives

- LHC upgrade program aims at 5-10 fold luminosity increase, higher radiation tolerance required for the on-detector electronics.
- Higher event rates require more efficient trigger algorithms
- Aging electronics → the present system was designed in 90s, originally planned operation time is ~10 years.
- Currently digitized data stored on the detector, readout only for Level-1 triggered events
- Completed re-design of TileCal electronics for upgrade in 2022. (Phase II)
- Upgraded electronics should transfer all digitized data off the detector
- Fully digital trigger with higher selectivity possible

Implementing Demonstrator readout system in 2014

- ❑ Discover and solve issues for the new designs
- ❑ Gain field experience for Phase II upgrade
- ❑ Evaluate digital trigger capability
- ❑ Compare performance of analog and digital in real time

Overview of Present TileCal Readout System at LHC

- 256 TileCal detector modules and electronics drawers
- Process $\sim 10,000$ PMT signals
- 16-bit dynamic range with bi-gain readout channels covering an energy range of 30MeV to 2TeV
- 40Msps continuous digitization
- Analog trigger
- Cesium, laser and electronic calibrations
- TTC trigger/timing/controls
- 2x redundant data transferring to off-detector

Present TileCal on-Detector Electronics at LHC

Electronics in a drawer:

- Up to 45 PMT Blocks with HV bases
- Up to 45 3-in1 cards (Front-end board)
- 4 mother boards
- 8 digitizer boards
- one optical interface board
- one TTC receiver mezzanine card
- up to 10 analog summing mezzanine cards
- one integrator readout board (CANbus)
- HVPS and distribution boards
- LVPS and distribution and sense adapters

The Present Single Drawer Readout Architecture

The present a single drawer electronics to process up to 45 PMT signals

Performance of Current TileCal System at LHC

Event display of Run 167607, Event 63115223, (ATLAS-CONF-2011-047, CERN, March 2011)

- The highest- p_T jet with p_T of 1.5 TeV collected in 2011
- The two leading jets are central high- p_T jets with an invariant mass of 2.8 TeV
- (p_T, y) of (1.5 TeV, -0.58) and (1.0 TeV, 0.44), respectively
- The missing ET in the event is 310 GeV

Tasks of TileCal Phase II Upgrade

3 optional front-end readout boards in development

- Shaper + bi-gain + slow integrator, developed by The University of Chicago, USA
- FATALIC ASIC chip, developed by University of Clermont-Ferrand, France
- QIE ASIC chip, developed by Argonne National Laboratory and Fermilab, USA

Demonstrator electronics

- Adapted front-end electronics developed by University of Chicago
- Raw data from each channel to off-detector sROD
- Mixed Analog and Digital Level-1 trigger

TileCal Analog Front-end Electronics For Demonstrator

Bi-gain readout resolution

(1) Fast signal processing

- 7-pole LC shaper and bi-gain clamping amplifiers with gain ratio of 32

(2) Slow signal processing

- 6-gain integrator for Cs calibration and monitoring minimum bias current of proton-proton collisions

(3) Charge injection calibration and controls

(4) Retain analog trigger capability for Demonstrator

Analog front-end board

Readout Linearity Improvement

Low Gain Channel

High Gain Channel

Readout Noise Improvement

Low Gain Channel RMS Noise

High Gain Channel RMS Noise

TileCal Data Digitization and Data Acquisition System (1 of 2 Sections)

A Single PMT Readout Data Flow

To other 2 Front-end Boards

Main Board & Layout

Complexity and Challenges:

- High speed: (560 Mbps)
- Max. trace length: (20 inches)
- All routes are basically in same direction
- Crosstalk consideration: (parallel and tandem)
- Mixed signals (low noise analog and high speed digital)
- Equal timing high speed traces
- Current rate constraints for supplies
- Avoid Switch-cheesed power planes (via usage limitation)
- Many other challenges to suppress DC/DC switchers noise

⚡ Exposure in higher radiation

- 6 signal layers
- 8 power layers including 3 redundant ground layers (continuous solid plane) for signal integrity and tandem crosstalk reduction

Daughter Board Development

- Daughter Board development is at Stockholm University
- First prototype manufactured and tested in 2011 with SNAP-12
- Second prototype manufactured in 2012 with both SNAP-12 and QSFP+ placed
 - ✓ Testing and evaluation in final phase
- Third prototype with QSFP+ only is in development

Diagram of second prototyping board

Kept SNAP-12 on for radiation evaluation in 2nd prototype, but no longer used in 3rd generation Daughter Board

In-System FPGA Configuration

- 2x redundant QSFP+ data transmission (80Gbps per Daughter Board) in 3rd prototype board
- Adaptable programming structure that allows cross-FPGA reprogramming if necessary (using before GBTx available)
- Enabling the GBTx JTAG connections by resistors or jumpers on the board
- Extended Daughter Board/Main Board JTAG programming chains

Diagram of 3rd prototyping Daughter Board

GBTx remote configuration

Super Readout Driver AMC

sROD in Demonstrator

- PMT readout for 4 Mini Drawers, supporting up to 45 PMTs
- Data concentration and processing (pipeline memories, reconstruction,...)
- TTC signals distribution & DCS management
- L0/L1 Calo functionality

sROD data reconstruction

- Merge Demonstrator data with other 7 drawers in present system for data reconstruction
- Synchronized with the TTC system
- Provide digital trigger information for evaluation

Super Readout Driver Platform

Double mid-size AMC will be ready in mid-November 2013 for testing

- Plugged in a ATCA carrier or in a μ TCA platform
- Sized 180.6 mm x 148.5 mm
- Gigabit communication with carrier/other AMCs
- ATCA test bench installed in building 175 at CERN

sROD AMC layout

Double AMC ATCA-1200 Carrier + RTM

Demonstrator System Testing Setups

One of 4 testing setups for the prototyping Demonstrator at University of Chicago

Summary & Acknowledge

- Analog Front-end Board passed performance and radiation tests in 2012, it well meets the requirements both in operation and radhard.
- Main Board, Daughter Board, sROD, LVPS, HVPS performance and radiation tests are planed in 2013-2014
- Demonstrator insertion (one drawer) is scheduled in 2014
- Phase II System Upgrade in 2018-2020

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