FTK and the Associative Memory (AM) System

FTK is an electronics system that rapidly finds and reconstructs high quality tracks in the inner-detector plane and SCT layers for every event that passes the level-1 trigger. It operates in two stages: in the first stage, 8 of the 12 ATLAS Pixel and SCT layers are used to perform pattern recognition and do the initial track fitting. Pattern recognition is carried out by a dedicated system called the Associative Memory (AM); tracks from the first stage pass to the second stage where they are extrapolated into the 4 logical Pixel and SCT layers not used in stage 1.

The AM system consists of the Associative Memory chip (AMchip04), an ASIC designed by INFN and optimized for this particular application, and two types of boards, a 9U VME board (AMBFTK) on which are mounted four local associative memory boards (LAMBFTK), mezzanines that hold 32 AMchips each. Both the boards and the chip are under evolution, and only the two most recent versions will be presented here.

The AMBFTK and LAMBSLP

The AMBFTK design and tests

The AMBFTK is a 9U VME board on which 4 LAMBFTKs are mounted. The figure to the right shows the AMBFTK layout, highlighting one of the LAMBFTKs in yellow. A network of high speed serial links characterizes the bus distribution on the AMBFTK: 12 internal serial links (in red) that carry the ATLAS Pixel and SCT detector hits from the PCI to the connector and, to 16 output serial links (each blue arrow represents 4 links) that carry the road numbers from the LAMBFTKs to PCI.

• The data rate is up to 2 Gb/s on each serial link. The control logic is placed inside a group of FPGA chips, visible in the figure. They are Xilinx Spartan FPGAs which feature Low-Power Gigabit Transceivers (GTPs). This ultra-fast data transmission requires specialized, dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues.

• Prototypes were available and were extensively tested in lab. An AMBFTK with one LAMBFTK mezzanine is shown in the picture to the right. Two main tests were performed:
  - Serial links. The test measured the Bit Error Rate (BER), using Pseudorandom Bit Sequence (PRBS). In the transmission, a PBB is selected and the receiver counts a signal that is asserted when there is an error detection in the links incrementing a counter. The measured BER was less than 10^-10.
  - Pattern-matching. This test validates the entire functionality of the AM system. A simulated pattern bank has been fast generated and loaded into each chip. With an iterative JTAG procedure, each pattern correct writing is checked. Then an input file with random bits is generated and loaded in memories. The stimulated pattern bank was compared to the matched output data generated by the on-board AMs, the result was a pattern error over 16 events.

The evolution of the AMBFTK: the LAMBSLP

Recently, a new approach on the data distribution strategy for the AM system has been adopted, totally based on VME. The new system, called Serial Link Processing, allows a high number of serial link buses at 2Gb/s bandwidth. An Xilinx Artic 7 FPGA receives the 12 input data buses and distributes them to the upper part and lower part of the board. The first prototype of this new board is shown to the left. It is currently used in test in the lab.

LAMBFTK and LAMBSLP

The LAMBFTK design and tests

The LAMBFTK and the LAMBSLP communicate through an SD interface placed in the center of the LAMBFTK, inside the yellow central rectangle in the figure to the right. Each LAMBFTK contains 32 AMchips, 16 on the component side and 16 on the solder side of the board. Their core voltage, 1.2 V, is provided through the large current (up to 25 A) LAMBFTKs connectors in the yellow boxes at the bottom of the figure, while the 1.05 V voltage, 3.3 V, is provided by the mezzanine central SD connector. The 32 AM chips in each LAMBFTK are connected as eight 4-chip pairs (4 pins on the top side 4 pins on the bottom side of the mezzanine). The GLUE chips are Xilinx Spartan FPGAs containing high-speed GTP serial links that are partially used to transfer data to the motherboard through the SD connector.

The tests for each event, organized in 8 lines, arrive at the LAMBFTKs from the AMBFTK through the SD connector and are fed partially in parallel, partially serially, using the GTPs. The mixed results of this data transfer then serial, half parallel, is due to the clock option having serial 1/2. The red arrows in the figure show how each bus is split four ways and distributed by the Spartan FPGAs while the blue arrows show the bus distribution by a pair of CPUs.

The LAMBSP

The LAMBSP, shown in the picture to the right, was tested in lab together with the AMBFTK. See above for the procedures and results of the tests.

The LAMBSLP

The LAMBSLP has a critical layout, because of the presence of the parallel buses. Its layout, showing the degree of complexity, is visible in the bottom figure to the left. Moreover, it requires many FPGAs for handling the input fan-out and the glue logic. In order to minimize the impact of these weaknesses on the system functionality, a new approach is under development, the LAMBSLP.

This new mezzanine is designed to match the AMBFTK board. The absence of FPGAs, as shown in the central figure on the bottom, makes the layout design simpler and more compact. The new layout is visible in the bottom figure to the right.

The prototypes of this new mezzanine will be available in the next months, and tests with the AMBFTK are planned to start just after the CDF 2012.