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INITIAL MEASUREMENTS ON A PROTOTYPE INDUCTIVE ADDER FOR THE CLIC KICKER SYSTEMS

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Abstract

The CLIC study is exploring the scheme for an electron-positron collider with high luminosity and a nominal centre-of-mass energy of 3 TeV. The CLIC pre-damping rings and damping rings will produce, through synchrotron radiation, ultra-low emittance beam with high bunch charge. To avoid beam emittance increase, the damping ring kicker systems must provide extremely flat, high-voltage, pulses. The specifications for the extraction kickers of the DRs are particularly demanding: the flattops of the pulses must be ± 12.5 kV with a combined ripple and droop of not more than ± 0.02 % (± 2.5 V). An inductive adder is a very promising approach to meeting the specifications. To achieve ultra-flat pulses with a fast rise time the output impedance of the inductive adder needs to be well matched to the system impedance. The parasitic circuit elements of the inductive adder have a significant effect upon the output impedance and these values are very difficult to calculate accurately analytically. To predict these parameters, the 3D geometry of the adder stack and its primary circuits has been modelled using FastHenry simulation code.

Recently, a five layer prototype has been built and measurements have commenced. The parasitic elements of the primary and secondary circuits of the prototype have also been measured and these values are compared with predictions. In this paper, initial results of the measurements are described and conclusions are drawn concerning the design of the prototype inductive adder.

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The CLIC study is exploring the scheme for an electron-positron collider with high luminosity and a nominal centre-of-mass energy of 3 TeV. The CLIC pre-damping rings and damping rings will produce, through synchrotron radiation, ultra-low emittance beam with high bunch charge. To avoid beam emittance increase, the damping ring kicker systems must provide extremely flat, high-voltage, pulses. The specifications for the extraction kickers of the DRs are particularly demanding: the flattops of the pulses must be ± 12.5 kV with a combined ripple and droop of not more than $\pm 0.02\%$ (± 2.5 V). An inductive adder is a very promising approach to meeting the specifications.

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I. INTRODUCTION

High-energy electron-positron colliders, such as CLIC [1], will be needed to investigate the TeV physics revealed by the LHC. They would provide very clean experimental environments and steady production of all particles within the accessible energy range. To achieve high luminosity at the interaction point, it is essential that the beams have very low transverse emittance: the Pre-Damping Rings (PDRs) and Damping Rings (DRs) damp

Figure 1. Schematic of an inductive adder with constant voltage layers and an analogue modulation layer.

the beam emittance to extremely low values in all three planes.

Kickers are required to inject beam into and extract beam from the PDRs and DRs. Jitter in the magnitude of the kick waveform causes beam jitter at the interaction point [2]. In particular, the DR extraction kicker must have a very small magnitude of jitter: the 2 GHz specifications call for a pulse of 160 ns duration flattop, 12.5 kV, 250 A, with a combined ripple and droop of not more than $\pm 0.02\%$ [1]. In addition, the kicker system must have low longitudinal and transverse beam coupling impedances [3].

II. THE INDUCTIVE ADDER

A review of literature of existing pulse generators has been carried out and an inductive adder (Fig. 1) has been selected as a very promising means of achieving the specifications for the PDR and DR kickers [4]. The inductive adder is a solid-state modulator, which can provide relatively short and precise pulses. The specifications for the PDR are less demanding than for the DR [3], hence, with a careful design of the adder, it may be possible to directly meet the ripple and droop requirements of the PDR kicker [5]: studies have shown

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that analogue modulation may also provide a solution to meet the specifications for the DR kicker [5, 6]. The reasoning for choosing the main components of the inductive adder has been given in [6]. Recently, a 5-layer prototype inductive adder has been assembled at CERN: initial measurements are presented below.

III. THE PROTOTYPE INDUCTIVE ADDER

The first prototype inductive adder (Fig. 2) is currently being tested at CERN. The specifications for this 5-layer prototype adder are the following: 3.5 kV output voltage, 70 A output current, 1 μ s pulse duration and up to 50 Hz repetition rate.

Figure 2. A prototype inductive adder.

Each layer of the inductive adder stack consists of two half-layer printed circuit boards (PCBs). Each half-layer PCB (Fig. 3) includes four primary circuit branches in parallel, each of which consists of a single 12 μ F NWL T00216 pulse capacitor [7], an APT12067LFLG MOSFET switch from Microsemi [8] and a driver board with an IXYS IXDD614SI gate driver circuit [9].

Figure 3. A half-layer printed circuit board. Charging resistors for the pulse capacitors are on a separate daughter board (labelled as connector board in

Fig. 2), which is connected to each half-layer PCB with a plug-in connector and receptacle. These daughter boards are supplied from a high voltage DC source to charge pulse capacitors and to provide low voltage DC for the gate drivers. The semi-circularly shaped boards, shown on the top of the stack in Fig. 2 are diode boards and contain both diodes and transient voltage suppressors for clamping transient voltages.

IV. INITIAL TESTS OF THE ADDER STACK WITH HALF-LAYERS

Various measurements have been carried out to test the operation of the prototype inductive adder. At first, the daughter boards were tested to ensure their correct operation when connected to the half-layer PCBs. Subsequently, the proper operation of single branches of half-layer PCBs was confirmed. After the single branches had been successfully tested, the half-layer cards were tested with all four branches powered.

A. Adder Stack with a Single Half-Layer PCB

The operation of the inductive adder was verified initially with a single half-layer PCB installed into the stack. The test setup is shown in Fig. 4.

Figure 4. Adder stack with one half-layer PCB and a diode board.

Fig. 5 shows measured load voltage V_{Load} , voltage over the MOSFET switch V_{D-S} and trigger reference signal V_{Tr} . The voltages were recorded using a Tektronix DPO5034 oscilloscope. The load used was a low inductance 10 Ω resistor. Pulse duration was 1 μ s and the 12 μ F pulse capacitors were initially charged to 20 V. In this measurement, a single branch of the inserted half-layer PCB was triggered-on. In Fig. 5 it can be seen that the trigger signal V_{Tr} turns-on the MOSFET switch,

discharging the pulse capacitor through the primary circuit and therefore a voltage V_{Load} is induced on the secondary winding. This indicates that the adder stack is functioning as designed. The maximum output pulse voltage is 59% of the initial primary voltage. The output voltage does not reach 100% of the initial primary voltage for several reasons:

- a) voltage drop across the on-state resistance of the MOSFET: with 2 half-layers plugged in there would be 8 parallel MOSFETs, therefore significantly reducing the proportion of voltage dropped across the MOSFETs;
- b) voltage droop of the capacitors: with 2 half-layers plugged in there would be 8 parallel capacitors, therefore significantly reducing the proportion of voltage droop. The capacitor voltage droop is a result of both the load current and magnetizing current – the relatively long rise time of the output voltage (see below) results in a higher drop by the time that the maximum output voltage is obtained.

In Fig. 5 the output voltage swings back and peaks to a considerable reverse amplitude after turn-off of the MOSFET. This happens because all the absent layers in the stack were not equipped with free-wheeling diodes and the diode board which was installed was not optimized for the applied voltage range.

Figure 5. V_{Load} (magenta), V_{D-S} (cyan) and V_{Tr} (yellow) of the prototype adder with a single branch of a half-layer card powered (load connected to the top of the stack).

Two pulse generators are needed to feed a stripline kicker magnet in the CLIC DR kicker system [5]. The pulse generators provide, ideally, identical pulses but with opposite polarities. The inductive adder can generate a positive, negative or bipolar pulse, depending on the grounding point of the adder stack. The ground and output of the adder stack were interchanged to confirm the effect on the output pulse. The measurement setup was otherwise identical to the measurement shown in Fig. 4. The output pulse is shown in Fig. 6: as expected the measured load voltage is nearly identical, but opposite polarity, to the output pulse shown in Fig. 5.

The rise time of the output pulse in Fig. 5 and Fig. 6 is relatively slow (~ 500 ns). This long rise-time is attributable to the fact that even where PCB layers are not plugged in there are transformer cores in the adder geometry. These cores result in a current-dependent inductance, of several microHenries for the load currents during these tests, in series with the load resistor: thus the rise-time of the load current, and load voltage, is substantially increased.

Figure 6. V_{Load} (magenta), V_{D-S} (cyan) and V_{Tr} (yellow) of the prototype adder with a single half-layer card with the load connected to the bottom of the stack.

B. Adder Stack with Two Half-Layers

The prototype adder stack was also tested with half-layer PCBs inserted for two different primary windings. The aim of this test was to demonstrate that the output voltage is the sum of the individual layers. In addition, at the positions of the three absent layers of the adder stack,

Figure 7. A single branch of a half-layer PCB with a short-circuit visible on an absent layer.

Figure 8. V_{Load} (magenta), V_{D-S} (cyan) and V_{Tr} (yellow) of the prototype adder with two half-layer cards in each of which a single branch is powered and absent layers replaced with short-circuits.

a conducting piece was placed to ‘short-circuit’ the inductance of the cores (Fig 7). Fig. 8 shows the output voltage of the adder stack.

The duration of the pulse was 1 μ s. The maximum load voltage measured was 64% of the sum of the initial capacitor voltages, and this was limited by both the voltage drop across each MOSFET switch and because only one capacitor per layer was present. Clearly, the adder stack sums the voltages of two individual half-layer cards and therefore works as expected. In comparison with Fig 5. and Fig. 6, the rise time of the output voltage in Fig. 8 is much faster, less than 100 ns: this is due to ‘short-circuiting’ the inductance of the magnetic transformer cores of the missing layers (see above).

V. 3D MODELLING STUDIES

Good impedance matching between the inductive adder and the load is desirable in order to avoid reflections and hence to achieve short rise time for the output pulse. As explained in detail in [11], simulations have been carried out to estimate the parasitic circuit elements of the inductive adder, in order to design the pulse generator to have the desired output impedance. Fig. 9 show a cross-section of a single branch of a layer of an inductive adder with the main parasitic elements, namely primary leakage.

Figure 9. Cross-section of a single branch of an inductive adder with the main parasitic elements: primary leakage inductance L_{kpsl} , coupling capacitance C_c and secondary leakage inductance L_{ks} .

inductance for a single current loop L_{kpsl} , coupling capacitance C_c and secondary leakage inductance L_{ks} . Measurement details of these parameters, for the prototype adder, were presented in [11]

The primary and secondary leakage inductances have been modelled using FastHenry, which is a 3D simulation code [10]. Table 1, below, which was also presented in [11], has been updated with the latest results for the numerical predictions for the parameter L_{ks} . The 3D simulation method, once fully verified, will be used to predict the parasitic circuit elements for the next version of the CLIC DR inductive adder: this will permit high precision matching of the output impedance of the inductive adder and the impedance of the load without several iteration steps.

Table 1. Analytical estimates and predicted and measured values for primary leakage inductance (for a single loop), secondary leakage inductance and coupling capacitance.

	L_{kpsl} (nH)	L_{ks} (nH)	C_c (pF)
Analytical	n/a	6.3	6.2
Computational	36.7	7.9	n/a
Measured	43	6.6	7.0

VI. SUMMARY AND FUTURE WORK

The prototype inductive adder is currently being tested at CERN. The initial measurements have verified that the basic electrical design of the prototype adder stack is correct. The next measurements will be carried with more layers installed in the stack: the initial primary voltage and repetition rate will be gradually increased to at least the nominal specifications of the 5-layer prototype. The prototype adder has also been used to verify 3D predictions of the parasitic circuit elements and the results of these studies confirm that this method can be used to determine the values for future high precision pulse modulators.

As soon as testing of the prototype inductive adder is completed, another 5-layer prototype adder will be built. These two prototype devices will be used to test active and passive compensation methods for the ripple and droop of the output pulse as well as stability of the adders when used to feed bipolar pulses to a stripline kicker.

Significant future challenges include the measurement, in the laboratory, of the pulse ripple and droop to the required accuracy. Commercially available oscilloscopes are generally not capable of measuring the shape of the pulse flattop to the required accuracy. One measurement approach being considered for confirming that the analogue modulation layer (Fig. 1) can actively modulate the flattop of the pulse to the required accuracy is to feed the output of two inductive adders in the opposite sense through a single current-transformer (CT), such that the output of the CT is nominally zero. The analogue

modulation layer of only one of the inductive adders will then be operated – the CT should thus allow measurement of the effect of the output current of this layer sitting upon the load current.

Finally, two prototype devices will be built with nominal specifications for the CLIC DR kicker extraction system. These 12.5 kV pulse modulators will be tested with a stripline kicker in an accelerator facility. The deflection angle and the induced jitter to the beam will be recorded to verify the performance of the pulse modulators and the kicker stripline.

VII. REFERENCES

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