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FIRST RESULTS FROM A SILICON-STRIP DETECTOR WITH VLSI READOUT

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ABSTRACT

A 256-strip silicon detector with 25 micron strip pitch, connected to two 128 channel NMOS VLSI chips (Microplex), has been tested using straight through tracks from a Ruthenium beta source. The readout channels have an pitch of 47.5 microns. A single multiplexed output provides voltages proportional to the integrated charge from each strip. The most probable signal height from the beta traversals is approximately 14 times the rms noise in any single channel.

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INTRODUCTION

Silicon microstrip detectors with strip pitches that are two or more orders of magnitude smaller than the size of the amplifiers necessary to read them out have been in use for several years [1]. The discrete electronics and large fanout boards used in these experiments will not be practical around the intersection points of colliding beam machines such as SLC and LEP, where tens to hundreds of thousands of channels might be packed within a radius of a few cm. To make such arrays possible, an integrated circuit has been designed and fabricated which has 128 input channels with an input pitch of 47.5 microns. It has a single multiplexed output which provides a series of 128 pulses whose voltages are proportional to the integrated charge in each channel. The chip uses 5 micron NMOS technology and has an active area 4.7 mm wide and 6.4 mm long.

Preserving pulse height information provides a number of important advantages. Weighting channel location with pulse height for the fraction (often half or more) of tracks making pulses in one or more adjacent channels provides the most accurate position determination. Noise and pedestal levels can be tracked and thresholds set automatically. By using software correction algorithms, one RAM replaces thousands of screwdriver adjustments. Energy loss information can be used to search for particles having other than unit charge, and can help in recognizing unresolved track pairs. Noise pickup from the back plane of the detector can be subtracted using information from channels without tracks. Finally, possible detector and noise problems can more easily be recognized and diagnosed.

DETECTOR ASSEMBLY

For collider applications, special low density mountings will be necessary to minimize multiple Coulomb scattering. For this test, however, we have simply glued the components to a ceramic plate. Mounted on this plate is a small printed circuit fanout to attach the chip outputs and drive-line inputs to their external connections. This assembly is shown in Figure 1a. The silicon strip diode detector had an active length of 59 mm, a thickness of 280 μm , and a strip pitch of 25 μm . It was

supplied by Micron Semiconductor [2]. One part of the assembly is not at all standard. The connections between the detector and the chip must be made at a density that is 4 times the maximum normally used in the semiconductor industry. This density is achieved by having 4 paired rows of staggered bonding pads, with different loop heights for each paired row. The chips and detector used for this work are connected with gold wires which have 0.2 mm diameter quartz rods separating the wires of adjacent rows. The units currently under construction use 25 micron diameter aluminum wire which is stiff enough so that quartz rods are no longer needed. Figure 1b shows a photograph of one such bond set. The 128 input leads for an entire chip can be bonded in about 2 minutes using an automated wedge bonder [3].

THE CIRCUIT

A preliminary version of the chip has already been described [4]. A detailed description of the current version, which has significant improvements, is in preparation [5]. The special techniques needed to pack all the necessary components for one channel in a 35 micron wide strip and to keep them from oscillating in both the reset and integrating modes is described there. We include here a brief summary of how the chip operates. Figure 2 shows a schematic diagram of the circuit. Two inputs are provided to each channel: one from the strip detector, and one capacitively coupled from one of four calibration lines, each one of which supplies every fourth channel. (Multiple lines are used to permit the measurement of channel-to-channel cross coupling, particularly from detector strip-to-strip capacitance.) The coupling capacitors are as small as possible, consistent with reliable lithography (about 0.01 pF) to reduce the amount of noise entering the amplifier from the calibration lines. Figure 3 shows the response of the output pulse height with injected charge. A 5 volt calibration signal corresponds to an input charge that is 15 times larger than the charge obtained from a single ionizing particle. Input protection for negative overvoltages is provided by a diode formed from a section of the input path in the n^+ diffusion layer and the p type substrate below it. The same section runs parallel to a grounded gate, and on the other side of that gate, a grounded diffusion. The normally off transistor formed by these three elements shorts large positive signals to ground.

The amplifier runs on a +5 volt supply, has an open loop gain, A , of about 300, a rise time of 20 ns, and a settling time, at the percent level, of 200 ns. A substrate bias of -2 to -3 volts is required for proper operation of the output shift register. This value depends, in part, on transistor threshold values set in fabrication, and may not be necessary in future versions. In normal operation, each amplifier draws a substantial current, 3.5 mA, to provide a low noise first stage. Although it can be on continuously with good heat sinking, (and was in these tests), we plan, for operation at a collider, to pulse it on about 2 to 3 microseconds before the start of data collection to reduce heating. During this time the reset and store switches are closed and the output switches are open. Between 0.5 and 1.0 microseconds before data collection, the reset switch is opened, allowing the integrating capacitor to accumulate charge. During the last half of this period, after the C_{store} voltages have settled, the switch to storage capacitor C_{store1} is opened. A charge, q , coming from the detector produces a change in voltage on the integration capacitor, C_{int} , of q/C_{int} which is also impressed on C_{store2} . A small C_{int} produces a large output voltage, but it must be made large enough so the effective amplifier input capacitance, $(A+1) \cdot C_{int}$, is much larger than the capacitance of the detector strips. Then most of the generated charge will be collected, rather than remaining on the strip and inducing a significant voltage on adjacent strips. We have chosen $C_{int} = 0.1$ pF as a reasonable compromise between the desires for a large output and for small spreading of the signal.

At the end of data collection, the switch to C_{store2} is opened. Figure 4a shows the input switching sequence. During readout, the switches controlled by the shift register are closed sequentially, one channel at a time, as a high-voltage level makes its way along the read-bit path of the two phase, shift register. The voltages of C_{store1} and C_{store2} appear at the gates of transistors which control the currents flowing into the two output buses. When these currents enter the inputs of a differential amplifier, everything that produced equal charges on the storage capacitors, such as switching transients, noise from the reset transistor (an important effect), $1/f$ noise from the input transistor, leakage from the storage capacitors, and channel-to-channel variations in the quiescent output voltage of the amplifiers, are subtracted out. Switching transients from the shift register are also removed. Settling times at the output of the differential amplifier (a 733 in our case) are between 200 and 300 nsec per channel. The sequence of signals during readout is shown in Figure 4b.

The output signals of many chips can be multiplexed onto a common output line. At the end of the readout cycle, the high-voltage level associated with the read-bit appears at the end of the shift register. This is amplified in a three stage pad driver using a "super buffer" [6] and brought to an output pad. It can then be connected to the read-bit input pad of the next chip. Individual off-chip amplifiers, such as the 733 now used, will be needed for each signal output, but such devices are quite small (about 1 mm x 1 mm) compared with our chip. The capacity of C_{store} is designed to be large (about 0.6 pF) to minimize the decay rate of the voltage signal. With proper shielding of the chip against incident light, the decay over 50 ms was less than the measuring accuracy of 2%.

THE BEAM

No high energy test beams were available to us when the detector was first assembled, so we used electrons from a Ru^{106} source. Some care must be used in setting up the trigger. All the electrons from the low energy decays of the parent Ru nuclei, and many from the fast daughter Rh, will tend to scatter in the 280 micron thick silicon, crossing on paths that send the ionization into ten or more of the 25 micron wide channels. To minimize triggering on such events we used three scintillation counters S1, S2, and S3. S1, adjacent to the source, is only 1 mm thick and so greatly reduces triggers from the large number of gammas emerging from the source. S2 is in anticoincidence and has a hole slightly smaller than the silicon detector. It is placed far enough from S1 so electrons traversing S1 and entering the hole do so almost normal to its plane and that of the silicon detector immediately behind. S3 is large enough to stop all primary electrons, and is in turn placed far enough from S2 to intercept only those particles leaving the silicon detector on nearly perpendicular paths. The dimensions are given in Table 1. The threshold for S3 is set close to 3 MeV. This triple requirement: straight in, high energy, straight out, produces a population of events confined mostly to 1, 2 and 3 channels.

Table 1

<u>Element</u>	<u>Vertical</u>	<u>Horizontal</u>	<u>Length of element</u>
source	± 1 mm	± 15 mm	0 mm
window	--	--	0.4
space	--	--	2
S1	± 2	± 20	1
space	--	--	90
S2-scint.	± 22.5	± 32.5	5
S2-hole	± 2	± 15	5
space	--	--	5
silicon	± 3.2	± 30	0.28
space	--	--	90
S3	± 7.5	± 25	25

DATA ACQUISITION

Data is collected by repeatedly cycling through the acquisition control signal sequence shown in Figure 4. When a scintillator coincidence is detected during the time interval between the isolation of C_{store1} and C_{store2} , the readout sequence is entered. Due to limitations of the present off-chip ADC electronics, the cycle time is 10 microseconds per channel, more than an order of magnitude slower than the maximum possible. Three types of data are taken; on-time electron events, delayed trigger accidental events, and calibration data.

DATA ANALYSIS

In a preliminary run, taken without the electron trigger, pedestal values and their rms variations, σ_1 , are recorded for each channel. Figure 5 shows a pulse height distribution for single channel noise pulses taken during such a run. The data show a distribution that is roughly Gaussian without long tails. Data is then taken with the electron trigger and the pedestal values are subtracted channel by channel for each event. In addition, to compensate for short term baseline shifts, the difference in the average pulse height of the entire event being analysed and the pedestal average is further subtracted. Figure 6 shows a channel-by-channel display of four typical beta events with pulse heights plotted in units of each channel's σ_1 .

For further pulse height analysis, we search in each event for sets of one or more adjacent channels, each of which has a pulse height of more than $3.5 \sigma_1$. If either of the two immediately adjacent channels exceeds $1.75 \sigma_1$, they are also included. The pulse heights of the second through sixth channels on each side are averaged and used for a further subtraction to compensate for possible non-uniformities in the original baseline correction. Figure 7 shows the resulting pulse height distribution from a run with the electron trigger on time, and from a run with it delayed.

Events with more than one cluster of pulses satisfying the above criteria are also accepted and included in the histograms of Figure 7. Thus the high amplitude tail of the noise spectrum also appears in these plots, with its left side cutoff set by the acceptance criteria. This tail is seen in both the gate-delayed and the on-time distributions. About 4.53 times as many triggers were taken in accumulating the on-time sample, so about $4\frac{1}{2}$ times as many events would be expected in its noise peak. The observed number is 4.6. Noise events were confined entirely to the one-channel samples, although several would be expected by chance in the two-channel samples if there were no channel-to-channel noise correlations.

Signal events from beta traversals, mostly collected on 1 or 2 strips, are visible in the on-time distributions of Figure 7. There are 18 events, not shown in the figure, collected on 4 or more strips with pulse heights ranging from 19 to 48 channels. A channel-by-channel gain calibration using single-channel beta traversals would require considerably more data and has not been done for this sample. Comparing signal and noise data, we find the most probable signal pulse height is 14 times the rms noise in a single channel. Substantially all the noise counts in Figure 7 are below $8 \sigma_1$, while more than 98% of the beta counts are above that level.

RADIATION HARDNESS

A number of measurements of detector radiation hardness have already been made [7]. We plan to make a full set of such measurements on the Microplex MOS chip, with exposures to minimum ionizing radiation, neutrons, and synchrotron radiation. Thus far, only a preliminary set of measurements has been made using minimum ionizing radiation from a 2/3 Krad/hour Co^{60} source. More must be taken with the Co^{60} source, as well as with the others. The gate oxide is expected to be a major source of failures with power on, since hole-electrons pairs generated by ionization along particle tracks are separated by the electric field. The holes have a large trapping probability, and accumulate, either in the gate oxide, or at the oxide-silicon interface [8]. The field induced by this accumulation shifts the transistor thresholds, and eventually causes the device to fail.

The first change seen from irradiation is an increase in the magnitude of the substrate bias which is now required to cancel the effect of this trapped charge and permit proper operation of the shift register. About 100 microvolts per rad is needed up to 20 Krads, and above that about 25 microvolts per rad. With power on at a 25% duty cycle, gain changes begin to be observed at about 50 Krads (12.5 Krads with power, 37.5 without), and failure has occurred between about 50 and 200 Krads. With power off, one chip failed between 100 and 150 Krads, and two are still working after 900 and 1,200 Krads. We have also tested two chips of the preliminary version, one with power on that failed before completion of the first 15 Krad exposure, and one with power off that still works after 2,000 Krads.

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Figure Captions

- Fig. 1a Photograph of assembled detector.
- Fig. 1b Microplex chip and bonding to detector.
- Fig. 2 Schematic diagram of the circuit.
- Fig. 3 ADC channel number as a function of the voltage step applied to a calibrate input.
- Fig. 4 Sequence of control and output signals during (a) data collection and (b) readout. A 350 mV calibrate signal producing an output (67 mV) comparable to that of a minimum ionizing particle, is visible in the third channel on one of the two output traces. Smaller voltage differences between the two traces in the other channels are due to strip-to-strip capacitative coupling and to noise.
- Fig. 5 Pulse height distribution for single channel noise pulses.
- Fig. 6 Pulse heights of the 256 detector channels for 4 different β -events. (Pulse height is expressed in each channel's noise rms value, σ_1 .)
- Fig. 7 Pulse height distribution for (a) pulses passing loose criteria for electron tracks with the silicon detector store gates out of time, (b) pulses passing same criteria with the gates in time.

a)

b)

Fig.1

Fig.2

Fig. 3

Fig. 4

Fig.5

Fig.6

Fig. 7