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A radiation-hard PLL for frequency multiplication with programmable input clock and phase-selectable output signals in 130 nm CMOS

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ABSTRACT: A PLL (ePLL) is presented that is intended to be used as a frequency multiplier. The ePLL accepts 40, 80, 160 or 320 MHz as a reference and generates clocks at the same frequencies, regardless of the input clock. Moreover, the outputs are available with a phase resolution of 90° for the 40, 80 and 160 MHz output and 22.5° for the 320 MHz output. The radiation-hard design, integrated in a 130 nm CMOS technology, is able to operate at a supply voltage between 1.2 V and 1.5 V.

KEYWORDS: Analogue electronic circuits; Radiation-hard electronics; VLSI circuits

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1 Introduction

The ePLL has been developed in the framework of the GBT project which is currently under development at CERN as part of the LHC upgrade program. This project aims at the development of a radiation-hard chipset to be used as an on-detector transceiver for the LHC experiments. A bi-directional optical link operating at 4.8 Gbit/s connects this transceiver with the counting room while up to 56 front-end modules can be connected by means of electrical links (e-links).

Clocking is an important task in such an application. Although a 40 MHz machine clock is readily available, one typically needs clock frequencies that are a multiple of this. In the GBT design case, the e-links can be operated at 80 Mbit/s, 160 Mbit/s or 320 Mbit/s. Clock frequencies of 80 MHz, 160 MHz or 320 MHz need thus to be generated by means of a PLL. Another example in the GBT project can be found in the high-speed deserializer which converts the incoming 4.8 Gbit/s bit stream into 120 40 Mbit/s streams. Because of the division ratio of 120, which is not a power of 2, the divided clock has a distorted duty cycle. A PLL is needed to correct for this distortion.

The ePLL has been developed to address this kind of issues. In order to fit the needs of a broad range of applications, the ePLL accepts a wide range of input frequencies, namely 40, 80, 160 and 320 MHz, while always outputting these frequencies. Moreover, the phase of the 320 MHz output clock can be programmed with a resolution of 22.5° while the 40, 80 and 160 MHz clocks have a resolution of 90° . This enables the front-ends to align their clock to the LHC bunch crossings.

The topology of the ePLL is shown in section 2, some design aspects are discussed in section 3 and the measurement results are presented in section 5. A conclusion is drawn in section 6.

Figure 1. Topology of the ePLL.

2 Topology of the ePLL

The topology of the ePLL is depicted in figure 1. The input clock is fed to an input divider which divides the input frequency always to a 40MHz signal. Therefore, it has a programmable divider ratio: from 1 for a 40MHz input clock to 8 if the input clock has a frequency of 320MHz. On the contrary, the feedback divider has a fixed divider ratio of 8 because its input signal is always the 320MHz of the voltage-controlled oscillator (VCO). Besides generating the feedback clock, the feedback divider also produces the 40, 80 and 160MHz output clocks with a programmable phase resolution of 90°.

The phase-frequency detector (PFD) is able to measure the difference in frequency and phase of its input signals. Because of that, the acquisition range of the loop is actually only limited by the tuning range of the VCO which is indeed very wide. The PFD is composed of 2 edge detectors and a NOR gate to reset both of them [1]. If the feedback clock rises first, the first edge detector is triggered and generates a DOWN signal for the charge pump (CP) in order to decrease the VCO oscillation frequency. The rising edge of the input clock then triggers the second edge detector and generates an UP signal. The UP and DOWN signals being both high result in the resetting of both detectors by the NOR gate. The inverse happens if the rising edge of the input clock comes first. It is important to realize that both the UP and DOWN signals go high every clock cycle for a very short amount of time which is determined primarily by the delay of the NOR gate. Although the PFD has 3 *valid* states, this effect leads to the fact that in reality the 4th state, namely both UP and DOWN high, is part of the operation procedure as well.

The UP and DOWN signals of the PFD are converted to a current by means of the charge pump which will be discussed in more detail in section 3.1. The charge pump current is steered through a 1st order low-pass filter (LPF) to generate the control voltage for the VCO. The LPF is referenced to the supply voltage because of the pMOS current sources in the VCO as explained in section 3.2. In order to alleviate the effects of temperature and process variations on the loop behavior, the resistance of the LPF can be programmed with a 3-bit word between 1 k Ω and 15 k Ω . For the same reason, the filter capacitance can be set to 400pF or 500pF.

Figure 2. Circuit diagram of the charge pump.

3 Design aspects

3.1 Charge pump

The circuit diagram of the charge pump in the ePLL is shown in figure 2. The output current can be programmed by means of a 6-bit current-output DAC. The appropriate gate voltages for the nMOS and pMOS current sources in the charge pump output stage are generated by means of their diode-connected counterparts.

If the UP signal is high while the DOWN signal is low, the lower right and upper left switches are closed while the other 2 are open. As such, the current of the nMOS current source is steered to the output so that it flows through the loop filter, discharging its filter capacitor. Consequently, the oscillation frequency increases as decided by the PFD. At the same time, the current of the pMOS current source is absorbed by the unity-gain amplifier. On the contrary, if the UP signal is low while the DOWN signal is high, the current of the pMOS current source flows through the loop filter so the filter capacitor is charged and the oscillation frequency decreases. The nMOS current is then sourced by the unity-gain amplifier.

In the other cases, namely if the UP and DOWN signals are both high or low, the current of the pMOS source is absorbed by the nMOS current source without flowing in the unity gain amplifier or loop filter and thus affecting the control voltage. However, this is only true if the sink and source currents are exactly equal to each other. If they are not, a fraction of the current will still flow through the loop filter if the UP and DOWN signals are high or in the unity-gain amplifier if both are low. While the latter is not a real issue, the former should be prevented as it leads to a static phase error between the input clocks of the PFD. Therefore, a lot of effort has been put in the optimization of the matching between both currents. The most important aspect in this regard is the output resistance of all current sources involved which should be maximized. Firstly, this leads to a better copy of the DAC output current. Secondly, this reduces the imbalance between sink and source current that originates from a varying control voltage.

Figure 3. Topology of the VCO and circuit diagram of a delay cell.

Even if the sink and source currents are exactly equal to each other a static phase error can show up because of charge sharing between the filter capacitor and the parasitic drain capacitance of the current sources. As explained above, one should design the current sources with a long length to maximize their output resistance. This inevitably results to large devices with a fairly large drain capacitance as well. Therefore, it is of the utmost importance to keep the drain voltage of the current sources always equal to each other and thus equal to the control voltage. This is guaranteed by the unity-gain amplifier which consequently serves a dual functionality next to the sinking or sourcing of the current for the current source that is not used. The open-loop gain of the amplifier has been maximized in order to minimize the voltage difference between its input and output.

3.2 VCO

The VCO in the ePLL is a ring-oscillator composed of 8 cascaded delay cells as can be seen in figure 3. The VCO always oscillates at 320MHz when the PLL is locked and therefore the cell delay equals 195.3125ps, namely $1/16^{\text{th}}$ of the oscillation period. As this is a fairly large delay for the used 130nm CMOS technology, the input pairs of the delay cells are biased at a relatively small overdrive voltage in order to slow them down. Instead of using only nMOS current sources as load for the differential pair, nMOS diodes have been added [2]. This has been done in order to avoid the need for a common-mode feedback circuit to regulate the output common-mode level for each delay cell. Obviously, adding these diodes decreases the small-signal gain of the delay stages which is required to invoke oscillation. Therefore, a trade-off exist between the small-signal gain and the stability of the common-mode output level.

The cell delay is controlled by means of the gate voltage of the pMOS current sources, i.e. the current it sources to the differential pair. A lower control voltage leads to a smaller cell delay and thus a higher oscillation frequency because of the larger current flowing through the differential

Figure 4. VCO delay cell with 4 current sources which model the effect of an SET.

pair. The gate voltage of the nMOS current sources in the active load is generated by means of a replica biasing circuit which is common for all 8 delay cells.

The oscillation amplitude of the *analog* delay cells is significantly smaller than the supply voltage. However, the feedback divider expects a *digital* signal level at its input because it is basically conceived as a digital counter. Therefore, 8 differential to single-ended (D2S) converters are included in the design in order to generate a full swing digital signal from the differential signals in between all 8 delay cells. Doing so, 8 of the required phases of the 320MHz clock are generated: 0° , 22.5° , 45° , 67.5° , 90° , 112.5° , 135° and 157.5° . In order to save power, the other 8 phases are generated by inverting the already existing phases instead of using another 8 D2S converters. As can be seen in figure 3, transmission gates have been included in the initially generated phases so as to compensate for the delays of the inverters. In order to save on power even more, all D2S converters, except for the first one, can be turned off. The first D2S converter which generates the 0° phase is required to close the loop and drive the feedback divider and thus needs to be active at all times.

3.3 Radiation hardness

As this ePLL has been integrated in a 130nm CMOS process, the total ionizing dose effects can largely be neglected [3]. However, in order to keep the drain-source leakage to a minimum, all transistor gates have a width of at least $1\mu\text{m}$.

The radiation hardness of the ePLL basically depends on the radiation hardness of the VCO. This is especially the case for single-event transients (SETs) which can pull the PLL out of a locked state. This is because an SET on 1 of the oscillating nodes in the VCO can generate a large phase jump which is transferred to the PFD by the feedback divider. The PLL then needs to find lock again and this can take a considerable amount of time, determined partly by the natural frequency of the loop. Two approaches can be taken in order to alleviate this kind of problems. Firstly, one can increase the natural frequency of the PLL so as to reduce the amount of time it takes to find lock again. However, the problem with this approach is that one typically wants to set the natural frequency rather low to filter the jitter of the input clock which would lead to a long locking time after a phase jump. Secondly, one can design the VCO so that it shows a minimal phase jump after an SET. Although this approach comes with a certain power penalty, it is the preferred choice in this design as it is inherently the more robust solution.

The radiation hardness of a VCO delay cell has been assessed by means of the model as represented in figure 4. Currents I_1 , I_2 , I_3 and I_4 which mimic the charge deposit after an SET,

are injected in the sensitive nodes. These current sources inject a charge of 0.1 pC, 0.2 pC or 0.3 pC in 10 ps to model different types of impinging particles [4]. Simulations have shown that the maximum resulting phase shift on the 320 MHz output clock is around 615 ps and that the ePLL is able to recover from such a phase shift in only a few 40 MHz clock cycles.

4 Parameter selection

The ePLL is intended to be operated from a wide range of supply voltages between 1.1 V and 1.65 V. Moreover, it should work at a temperature ranging from -30°C up to 100° and obviously all process corners. The major consequence of these widely varying operating conditions is that the VCO gain can shift dramatically. Simulations have shown that it has a range from 182 MHz V^{-1} to 1200 MHz V^{-1} which is indeed very significant. Obviously, such a large spread on the VCO gain has its effect on the loop behavior. This can be quantified by observing the natural frequency ω_n and damping factor ζ of the ePLL which is a 2nd order charge pump PLL:

$$\omega_n = \sqrt{\frac{I_{cp}K_{vco}}{2\pi N C_{lpf}}} \quad (4.1)$$

$$\zeta = \frac{R_{lpf}}{2} \sqrt{\frac{I_{cp}C_{lpf}K_{vco}}{2\pi N}} \quad (4.2)$$

where I_{cp} is the charge pump current, K_{vco} is the VCO gain, N is the feedback divider ratio and C_{lpf} and R_{lpf} are the loop filter capacitance and resistance respectively. In order to stabilize the natural frequency and damping over all process corners and operating conditions, the charge pump current can be programmed from $0.8\text{ }\mu\text{A}$ up to $54\text{ }\mu\text{A}$ by means of a 6-bit DAC as mentioned in section 3.1. The damping factor can then be set independently by means of the filter resistance. The intended natural frequency is around 1 MHz while the intended damping factor is in the range 0.7-1.5.

5 Measurement results

The ePLL has been designed in a 130 nm CMOS process. At a supply voltage of 1.5 V, the power consumption of the ePLL equals 29 mW if only a single D2S converter is activated. If a 320 MHz output clock phase which is different from 0° or 180° is required, an extra D2S converter needs to be activated and the power consumption rises to 30.5 mW. If one needs all 16 phases, all 8 D2S converters can be turned on and the power consumption tops at 41.5 mW.

The measurement of the programmable output phase of the 320 MHz output clock is shown in figure 5. It can be noticed that the phase step is almost always an ideal 22.5° . As mentioned before, this feature can be used in the front-ends to align the clock to the LHC bunch crossing. The output phases of the 40, 80 and 160 MHz output clocks have a similar ideal behavior, however with a phase step of 90° in this case. The phase resolution of these latter output clocks can be increased to 11.25° , 5.625° and 2.8125° for the 160, 80 and 40 MHz clocks respectively by resampling them with one of the 320 MHz output clocks.

The measured output jitter with a clean input clock source in 2 different configurations is shown in figure 6. It can be noticed that the measured jitter as a function of charge pump current and loop filter resistance behaves more or less identical in both cases. This is because the loop is

Figure 5. Measured programmable phases of the 320 MHz output clock.

Figure 6. Measured RMS output jitter with different input clock and output clock configurations.

not altered when another input frequency is applied or when a different output clock is observed. It can be concluded that the RMS jitter is below 10 ps with a careful choice of the loop parameters.

The RMS output jitter when periodic jitter with a peak-to-peak amplitude of 125 ps is applied at the input is shown in figure 7. The ePLL tracks the input jitter at low frequencies because of the low-pass character of the ePLL. On the contrary, at very high jitter frequencies the loop is not able to track the input clock anymore and the output jitter falls back to its nominal value as presented in figure 6 without any input jitter. The cut-off frequency is basically the natural frequency of the loop. As expected from simulations, it is between 1 MHz and 3 MHz dependent on the loop parameters.

6 Conclusion

A highly flexible ePLL has been presented with a programmable input clock frequency of 40, 80, 160 or 320 MHz while always outputting these 4 frequencies. The phase of the 320 MHz output clock can be programmed with a resolution of 22.5° in order for the end user to be able to align

Figure 7. RMS output jitter versus frequency of the input jitter with 125 ps peak-to-peak amplitude.

the clock to the LHC bunch crossing. Moreover, the 40, 80 and 160 MHz output clocks have a programmable phase with a resolution of 90° . At a supply voltage of 1.5 V, the ePLL has a power consumption between 29 mW and 41.5 mW dependent on the number of output phases that are required. Measurements have shown splendid jitter performance below 10 ps RMS. Moreover the jitter transfer measurement has shown that the natural frequency is indeed as expected from design between 1 MHz and 3 MHz.

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