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SENSITIVITY ANALYSIS FOR THE CLIC DAMPING RING INDUCTIVE ADDER

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Abstract

The CLIC study is exploring the scheme for an electron-positron collider with high luminosity and a nominal centre-of-mass energy of 3 TeV. The CLIC pre-damping rings and damping rings will produce, through synchrotron radiation, ultra-low emittance beam with high bunch charge, necessary for the luminosity performance of the collider. To limit the beam emittance blow-up due to oscillations, the pulse generators for the damping ring kickers must provide extremely flat, high-voltage pulses. The specifications for the extraction kickers of the CLIC damping rings are particularly demanding: the flattop of the output pulse must be 160 ns duration, 12.5 kV and 250 A, with a combined ripple and droop of not more than $\pm 0.02\%$. An inductive adder allows the use of different modulation techniques and is therefore a very promising approach to meeting the specifications. PSpice has been utilised to carry out a sensitivity analysis of the predicted output pulse to the value of both individual and groups of circuit components: these results are used to define component performance requirements, nominal values and tolerances. This paper reports the simulation results as well as tests and measurements of the various candidate components, including semiconductor switches, pulse capacitors and transformer cores.

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Sensitivity Analysis for the CLIC Damping Ring Inductive Adder

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ABSTRACT

The CLIC study is exploring the scheme for an electron-positron collider with high luminosity and a nominal centre-of-mass energy of 3 TeV. The CLIC pre-damping rings and damping rings will produce, through synchrotron radiation, ultra-low emittance beam with high bunch charge, necessary for the luminosity performance of the collider. To limit the beam emittance blow-up due to oscillations, the pulse generators for the damping ring kickers must provide extremely flat, high-voltage pulses. The specifications for the extraction kickers of the CLIC damping rings are particularly demanding: the flat-top of the output pulse must be 160 ns duration, 12.5 kV and 250 A, with a combined ripple and droop of not more than $\pm 0.02\%$. An inductive adder allows the use of different modulation techniques and is therefore a very promising approach to meeting the specifications. PSpice has been utilised to carry out a sensitivity analysis of the predicted output pulse to the value of both individual and groups of circuit components: these results are used to define component performance requirements, nominal values and tolerances. This paper reports the simulation results as well as tests and measurements of the various candidate components, including semiconductor switches, pulse capacitors and transformer cores.

Index Terms — Inductive adder, kicker system, CLIC, pulse power modulator

I. INTRODUCTION

High energy e⁺e⁻ colliders, such as CLIC [1], will be needed to investigate the TeV physics unveiled by the LHC. They would provide very clean experimental environments and regular production of all particles within the accessible energy range. To achieve high luminosity at the interaction point, it is essential that the beams have very low transverse emittance: the Pre-Damping Ring (PDR) and Damping Ring (DR) damp the beam to an extremely low emittance in all three dimensions. The design parameters of the PDR and DR are defined by target performance of the collider, the injected beam characteristics or compatibility with the downstream system parameters: the emittances of the positrons must be damped by several orders of magnitude [2].

Figure 1. Schematic of an inductive adder with “constant” voltage layers, a digital modulation layer and an analogue modulation layer.

Kickers are required to inject beam into and extract beam from the PDRs and DRs. Jitter in the magnitude of the kick waveform causes beam jitter at the IP [2]. Thus the PDR and DR kickers, especially the DR extraction kicker, must have a very small magnitude of jitter: the 2 GHz specifications call for a 160 ns duration flat-top of 12.5 kV, 250 A, with a combined ripple and droop of not more than $\pm 0.02\%$, and low longitudinal and transverse beam coupling impedances [3-5].

II. THE INDUCTIVE ADDER

A review of literature of existing pulse generators has been carried out and an inductive adder (Figure 1) has been selected as a very promising means of achieving the specifications for the PDR and DR kickers [6]. The inductive adder is a solid-state modulator, which can provide relatively short and precise pulses. With a proper design of the adder it may be possible to

directly meet the ripple and droop requirements of the PDR kicker [7]: studies have shown that analogue modulation may also provide a solution to meet the specifications for the DR kicker [7, 8]. Reasoning for choosing the main components of the inductive adder has been given in [7].

III. EVALUATION OF COMPONENTS

A. PULSE CAPACITORS

The pulse capacitors chosen for the inductive adder are manufactured by NWL Capacitors [9]; each capacitor is nominally 12 μF , rated for a peak pulse current of 280 A and a voltage of 1 kV, d.c.. The inductance of 10 pulse capacitors has been determined by individually short-circuiting a charged capacitor and measuring the resonant frequency. A 4 cm wide, 6 cm long and 0.6 mm thick copper plate has been used to short-circuit the pins of the capacitor to each other.

The capacitance values were measured with a Fluke 289 digital multimeter and the output voltage, an exponentially decaying sine wave, with a Tektronix DPO5034 oscilloscope. The resonant frequency was determined from the time interval between two consecutive peaks of the output waveform, which gives the fundamental period. The resistance was computed from the damping factor of the decaying curve. A lumped element model and the equations for calculating inductance and resistance have been presented in [10].

The results of these measurements have been summarized in Table 1. The average inductance of the ten pulse capacitors is approximately 14 nH. In the inductive adder several pulse capacitors will be connected in parallel, which further decreases the effective inductance of the pulse capacitors in the primary loop circuit. However the circuit board layout is important for minimizing the total primary circuit inductance.

Table 1. Average values and standard deviation of capacitance, inductance and resistance of 10 NWL pulse capacitors.

C/ μF	$\sigma_C/\mu\text{F}$	L/nH	σ_L/nH	R/m Ω	$\sigma_R/\text{m}\Omega$
12.12	0.15	14.35	0.40	16.66	2.73

B. SWITCHING MOSFETS AND IGBTs

A selection of fast switching MOSFETs and IGBTs has been tested using the IXYS IXDN409YI gate drive circuit. The load resistor was 2 Ω . The circuit diagram (Figure 2) of the test setup is shown with a MOSFET switch but was similar for the IGBT tests.

Figure 2. A test circuit for fast switching MOSFETs and IGBTs.

For the CLIC DR kicker, the desired rise and fall time of the pulse is below 100 ns [7]. Several promising candidate switches have been identified and tested: the results of these

measurements have been shown in [10]. The next step for continuing these tests is to use higher charging voltage, up to 700 V, and an inductive load. The inductive load may reduce the rise times significantly, as shown in [11].

C. LINEAR MOSFETS

In order to apply analogue modulation techniques linear MOSFETs are required. In the proposed design of the inductive adder [6], the operating voltage range for the linear switches is up to 200 V, with a current capability requirement up to 10 A per layer. Initially, the linear MOSFETs were tested in a static operating mode using a d.c. power supply as the gate drive circuit.

Figure 3 shows the measured current I_D as function of U_G for several MOSFETs. According to these tests, ARF466AG, ARF449AG, ARF460AG and ARF463AP1G are the most promising candidates for further tests because they have the largest linear range. However, more measurements are required to verify their performance in the desired voltage and frequency range.

Figure 3. Current I_D as function of voltage U_G for selected linear MOSFETs (d.c. measurements).

D. TRANSFORMER CORES

Transformer cores are currently being evaluated for the inductive adder to determine the linearity of the B-H curve. The results of these measurements will be used to build mathematical models of the cores for simulating the magnetization current during the pulse and its contribution to the voltage droop and ripple of the output voltage of the adder. In addition the temperature stability of the cores will be measured. The maximum pulse width of the inductive adder type modulator is limited by the voltage – time integral of the transformer core and the cores should not be driven into saturation in any operation condition. The d.c. characteristics of the cores need to be verified to design a reset circuit for the cores.

IV. SIMULATION MODEL

An equivalent circuit of the inductive adder has been developed and simulated using PSpice software. The

simplified equivalent circuit of a single layer of the inductive adder, which is based on the model shown in [12], is presented in figure 4. The model consists of 18 identical layers, each of which includes storage capacitor C_s , primary leakage inductance L_{kp} , magnetizing inductance L_m , secondary leakage inductance L_{ks} , coupling capacitance C_c and switches. The parasitic electrical parameters of the adder stack are based on the physical dimensions of the adder stack. The equations for dimensioning the adder stack have been presented in [13] and the preliminary design parameters for the CLIC damping ring inductive adder have been shown in [6]. The semiconductor switches have been modeled as ideal switches. Snubber and diode clamping circuits, which are necessary for protecting switches in the real device, are not, initially, modelled.

Figure 4. Equivalent circuit of a layer of an inductive adder with a load.

V. SENSITIVITY ANALYSIS

A. DESIGN PARAMETERS OF THE ADDER STACK

The output impedance of the inductive adder should ideally be matched to the load. However, during the initial design phase, the value of primary leakage inductance L_{kp} may not be known exactly and it affects the output impedance significantly. The output impedance also depends upon the secondary leakage inductance L_{ks} and coupling capacitance C_c , the values of which depend on the outer diameter of the secondary winding and the insulation material between the primary winding and the secondary winding. Therefore, the diameter of the secondary winding can be adjusted to obtain the desired output impedance for the adder.

Table 2 shows the parameters for the sensitivity analysis: a nominal value of 20 nH was assumed for L_{kp} and the values of L_{ks} and C_c calculated, from the equations of [12], to obtain an output impedance of 50 Ω . The value of L_{kp} was then changed by $\pm 30\%$ and the values of L_{ks} and C_c were recalculated, by effectively changing the diameter of the secondary winding, so that the output impedance was still 50 Ω : it was assumed that the insulation material between the primary and secondary windings is polyethylene with permittivity of 2.3.

Figure 5 shows the predicted output voltage of an 18-layer inductive adder for the 3 sets of parameter values shown in Table 2. The output of the adder is in all cases matched to the load according to equations shown in [12], and an ideal 50 Ω load is modelled. The different values of the stack inductance,

Table 2. Parameters for sensitivity analysis.

$C_s/\mu\text{F}$	C_c/pF	$R_p/\text{m}\Omega$	$L_m/\mu\text{H}$	L_{ks}/nH	L_{kp}/nH
320	10.8	6	20	6.94	20
320	8.71	6	20	7.85	14
320	12.9	6	20	6.32	26

coupling capacitance and primary leakage inductance affect the rise time, ringing and settling time of the pulse. The table 3 summarizes the results. The transit time of the ideal switch was set to 100 ns, which is consistent with the rise times of tested switches [10], therefore the rise times shown in table 3 are not necessarily the minimum rise times which can be achieved with these design parameters. Theoretically, the rise time of the output pulse corresponding to values of L_{kp} , L_{ks} and C_c of the first row of table 2 is 19.4 ns, calculated by the equation shown in [12]. Settling time is taken from the end of the rise time to the time when the ripple has settled below $\pm 0.02\%$.

Figure 5. Output voltage of an 18-layer inductive adder with three different sets of parameters.

Table 3. Summary of sensitivity analysis simulations

L_{kp}/nH	Rise time/ns (10...90%)	Settling time/ns ($\pm 0.02\%$)
20	22.8	27
14	20.7	26
26	24.9	36

B. TIME VARIANT LOAD

The resistance of the terminating load may change during the pulse. This effect was studied by simulating either a linear or an exponential change for the load resistance. The output of the inductive adder was simulated as a controlled voltage source V_s and the kicker magnet and cables as ideal transmission lines T_1 and T_2 , as shown in figure 6. The time variant load was implemented by a parallel terminating resistor R_{load} and controlled current source I_1 .

Figure 6. PSpice model for simulating effects of time variant load.

Figures 7 and 8 show the simulated responses of the load voltages for linear and exponential changes of the load resistance. In both simulations, the load resistance was changed from 49.5 Ω to 50.5 Ω during the flattop pulse. Figure 7 shows that the effect of the linear change of the load resistance causes a response which is of transient nature: after the delays of the kicker magnet and transmission line (in total 40 ns), the pulse remains constant for duration of linear change.

Figure 7. Kicker system response for a linearly time variant load.

Figure 8. Kicker system response for an exponentially time variant load.

Ideally, this could be compensated by changing the charging voltage of the storage capacitors. On the contrary, figure 8 shows that the exponential change of the load resistance causes distortion for the pulse during its full length. The response

approaches the linear case when the rate of change of the load resistance approaches a constant asymptotic value. The exponential change of load resistance may be compensated by an active means, for example applying analogue modulation to the output voltage.

VI. CONCLUSION

Initial results from measurements of components, for finding the best candidates for the high precision inductive adder, have been obtained. Promising candidates for both on-off type and linear type semiconductor switches, to be used for the prototype inductive adder for the CLIC damping ring kickers, have been identified. Simulations studies have been completed for verifying the design parameters of the adder stack. The effects of time variant load was also studied and the means for compensating its effects have been proposed.

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