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FASTBUS IN EXPERIMENTS IN EUROPE

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Abstract

FASTBUS is currently being specified for the electronics of nearly all the new generation of high energy physics experiments in Europe. The emphasis in FASTBUS device development has shifted from design and test support towards electronics dedicated to read-out systems for detectors, event formatting and on-line processing. This paper offers a rationale, illustrated by several of the more important recent developments, for the adoption of FASTBUS as the appropriate standard for use in the European Physics environment.

Introduction

The year 1985 has been fertile for FASTBUS developments in Europe. The lay-out of several data acquisition and processing systems in FASTBUS has taken shape, for example those of the four experiments at the Large Electron Positron collider (LEP). Others, such as the UA-2 collaboration have adopted FASTBUS for the upgrade of the front end electronics, and the data acquisition and trigger system of the experiment. FASTBUS systems have become operational in the experiments NA-31 and UA-1, and successfully started taking data.

All these implementations are or will be operational at CERN. At DESY in Hamburg, West Germany, the use of FASTBUS is being considered for future experiments at HERA, the Hadron-Electron Ring Accelerator.

The ESONE Advanced System Study Group (ASSG) has met once this year, to discuss amendments and errata in the FASTBUS specification. The publication of the specification as an ESONE document has been prepared but awaits final agreement on the above mentioned points.

At CERN regular meetings have been organized between representatives from experiments and support groups to discuss and agree on common designs and practices, wherever possible, both for the hardware and the software.

A well attended and fruitful FASTBUS software workshop has been organized at CERN. The presentations summarized nicely software activities in the US and Europe, and gave rise to many constructive discussions.

As happened for NIM and CAMAC, European industry is gradually building up a range of FASTBUS hardware. In particular, crates and power supplies are becoming available at a price which makes FASTBUS cheaper than CAMAC, VME, etc.

In the following sections more details are given on the major implementations and general purpose developments.

FASTBUS in the LEP Experiments

The construction of the LEP collider at CERN progresses according to schedule. The machine, 27 km in circumference, is situated across the border between France and Switzerland, and reaches from the Jura mountains to nearby the Lake of Geneva. Its implantation is shown in Fig. 1. The first particles are planned to be accelerated by the end of 1988. Four

experimental areas are foreseen to house one large experiment each. The experiment L3 will be installed in area 2, ALEPH in area 4, OPAL in area 6 and DELPHI in area 8 (see Fig 1). All the experimental areas are far below the surface, 2 at ≈ 51 m, 4 at ≈ 145 m, 6 at ≈ 100 m and 8 at ≈ 104 m.

Fig. 1. Plan showing the implantation of the Large Electron Positron collider (LEP) at CERN.

Each experiment has a large central detector and numerous "subdetectors". The front end, trigger, filtering and formatting electronics will be down in the experimental area, whereas most of the computers and peripherals are planned at the surface. High speed FASTBUS links are foreseen for communication between these two parts.

The electronics in each of the experiments is expected to dissipate 300-500 kW and, in view of the limited space, water-based cooling is foreseen.

All four experiments plan to use a large quantity of FASTBUS equipment, of which the design is in progress. A strong effort is being made to specify and use units of common interest, but of course there is also a need for detector specific electronics. The systems of ALEPH and DELPHI are virtually completely planned in FASTBUS, OPAL and L3 are considering a mixture of CAMAC, FASTBUS and VME.

In what follows a summary is given of the data acquisition systems, as well as some details on the major FASTBUS developments for these experiments, listed in alphabetical order.

ALEPH

A lay-out of the central data acquisition system of this experiment is shown in Fig. 2. It is both a modular and hierarchical architecture to allow for independent testing of subdetectors, multilevel triggering and event building. Each subdetector has a "sub-

detector crate", with an Event Builder (EB)¹⁾ and a Local Trigger Supervisor (LTS). This EB collects the data from the read-out processors in the front-end electronics and stores it in its multi-event memory, under control of the LTS. Data in the EB can be accessed by the subdetector VAX for testing or monitoring. Data for complete events is taken from the EBs by the Main Event Builder (MEB) under control of the Main Trigger Supervisor (MTS). Finally the Event Processor will take data from the MEB for on-line processing of complete events.

Fig. 2. Lay-out of the data acquisition system of ALEPH.

The central detector of ALEPH is a Time Projection Chamber (TPC) of which signals are read-out from 6500 wires and 41000 pads. The read-out electronics which is being developed consists of Flash ADC (FADC) based charge digitizers (TPD) and 68020 based read-out controllers (TPP). Each TPD module (3 U) contains 64 signal processing channels (shaping and digitizing). One TPP controls the electronics for one TPC sector (≈ 1200 channels). The system²⁾ will be housed in ≈ 110 FASTBUS crates.

Another large detector in this experiment is the electromagnetic calorimeter (a lead/wire chamber sandwich). It has a total of ≈ 225000 channels. Charge integration and signal multiplexing will be done by electronics mounted on the detector. ADC modules are being developed with 10 bits accuracy and 16 bits dynamic range. The system will require ≈ 10 FASTBUS crates.

Further FASTBUS equipment is foreseen for the hadron calorimeter and muon detectors, the inner tracking chamber, the minivertex detector and others.

The total number of FASTBUS crates in ALEPH is estimated to become approximately 250.

DELPHI

DELPHI has the largest number of subdetectors. Therefore an organized effort is being made to limit the variety of electronics and thus to standardize the front end as well as the data acquisition electronics.

Fig. 3. Schematic diagram of the data acquisition system of DELPHI

A simplified version of the data acquisition system is shown in Fig. 3. Again the architecture of the data acquisition system provides for independent subdetector read-out and multi-level triggers. Sub-detector event building is done by a combination of General Purpose Master (GPM)³⁾, Dual Slave Memory (DSM)³⁾ and Blockmover (BM)⁴⁾. GPMs and DSMs are also foreseen for compilation of data from subdetectors to form complete events. An "Emulator Farm" based on the 3081/E⁵⁾ is foreseen to process this data.

The central detector of DELPHI is a T.P.C., with ≈ 2000 wires and ≈ 20000 pads to be read-out. The electronics under development, consists of FADC based charge digitizers. The analogue signal processing circuitry is separated from the digitizing part. Ninety-six analogue channels are mounted per module (3 U) and the associated 96 digitizing channels in another module (3 U). The system will be assembled in ≈ 90 FASTBUS crates ($\approx 50\%$ of a low power version for the analogue part).

Many subdetectors in DELPHI need time digitizers, with a high resolution (≥ 2 ns), a wide dynamic range (≥ 32 μ s) and multiple hit capability. A general purpose unit, the L.T.D. (LEP Time Digitizer) has been specified, which covers the needs of most of DELPHI's detectors in this respect. A CAMAC prototype, responding to the specifications has been designed and successfully tested. Each input channel has a fine time (2 ns) interpolator, whereas all inputs share the coarse time (32 ns) measuring part. Currently a 48 channel FASTBUS module (1 U) is being designed.

L3

As for all LEP experiments the system is again modular and has a hierarchical structure for triggering and data filtering. The combination of Block Mover (BM) and GPM (General Purpose Master) performs event building, both as "Local" (subdetector) and "Main" (central crate) event builder. Dual Slave Memories (DSM) are used in spy-mode at the subdetector crate level, as circular buffers at the central crate and partitioned buffers for the "level 2" trigger results. As "level 2" trigger processor the XOP (Expandable On line Processor)⁶ is foreseen and 3081/E as "level 3" processors. In Fig. 4, the F682C is a XOP to FASTBUS interface and the MMB is a Multi-port Multi-event Buffer. The latter unit has eight fast independent event buffers (2 k x 16) per port (front panel ECL inputs) and is organized as circular FIFO.

OPAL

CAMAC and a special in-house standard⁷⁾ will be used for most of the front-end electronics. The central data acquisition system is completely based on VME, of which the description falls outside the context of this paper.

A number of smaller FASTBUS systems are in operation or in preparation. Firstly, there is the FASTBUS system in the experiment NA-31⁸⁾. During the CERN SPS fixed target running period from April to August 1985, the full FASTBUS data acquisition system for this experiment on CP-violation was commissioned. The system consists of three FASTBUS crate segments and one FASTBUS cable segment, and has more than 50 individual FASTBUS modules of 17 different types. During a full three-week data-taking cycle, 80 Gigabytes of data were obtained through FASTBUS. The system, which takes data into a VAX 11/750 either directly through a CFI or indirectly through a Block Mover and a 168E subsystem, performed reliably during this period. Few major changes are envisaged for the run in 1986, although a second FASTBUS cable segment will probably be installed.

A major FASTBUS system is in preparation for the UA-2 experiment. The UA2 detector is presently being upgraded to prepare for higher luminosity running in Fall 1987. A new multi-level trigger is required and the instrumentation of the detector is being improved. The increased data flow and the need for embedded processors imposes a large burden on the data acquisition system, currently based in CAMAC/REMUS. A FASTBUS architecture will be used for the new system. This system will consist of ≈ 12 FASTBUS crates, of which ≈ 10 will contain the front-end electronics (largely ADCs plus FASTBUS to REMUS branch drivers to access the electronics already contained in CAMAC).

Each front-end crate contains a powerful local processor to format and buffer the data, in addition to the digitizing modules themselves. The next level of the system contains a processor for assembling the event from the front-end crates, plus additional processors for performing high-level event filtering. The final level contains the connection to the host VAXes, which see only filtered and formatted events.

General Purpose FASTBUS Developments

An increasing amount of basic FASTBUS system hardware, development tools and diagnostic devices is becoming available. A few topics are listed in the following.

Very interesting offers from European industry have been obtained at CERN for the supply of an integrated general purpose design¹¹⁾ of a FASTBUS crate, power supply and cooling. FASTBUS thus becomes cheaper than CAMAC, VME, or any other bus system of this kind available on the market.

Further work has been done on couplers or module-bus interface circuits. A TTL-PAL based design has been made, which is now available in hybrid form¹²⁾. Another TTL-PAL based coupler with different characteristics, as well as a high speed coupler based on ECL-PALs are now also available¹³⁾. A variant of these couplers including the ADI-chips has also been designed

A monolithic high speed slave coupler based on ECL gate arrays is under development¹⁴⁾. Two circuits, DATPRO (data protocol) and ADPRO (address protocol) form the core of this coupler. The DATPRO design is completed and chips have been produced and successfully tested.

In many applications all facilities of the standard Segment Interconnect are not required, in particular in front-end electronics. For these cases a Crate Clustering Card has been developed¹⁵⁾ which can replace standard Segment Interconnects, and thus give important savings. It allows the interconnection of up to 4 crates, and replaces the Ancillary Logic as well. Only one crate in a cluster needs Ancillary Logic. Extended Geographical Addressing is not possible, and bits 24 and 25 from the Group field are used to identify crates in the cluster. FASTBUS masters are allowed in any number of the four crates.

In Europe the interfacing of FASTBUS systems to a host computer is still mostly done via CAMAC. The CFI (CAMAC-FASTBUS Interface)¹⁶⁾ and the FIORI¹⁷⁾ are normally used, but for special applications also the FASTBUS Sequencer (FSEQ)¹⁸⁾ and the LRS-SM1821. A direct UNIBUS-CFI interface (DRE11) has been developed¹⁹⁾, as well as direct interfaces from the VME bus (VIOR²⁰⁾) for the CFI, FSEQ and FIORI.

Acknowledgement

FASTBUS developments are now under way over a very wide front and therefore it has become difficult to give a complete account of all activities in such a short presentation. Many friends, too numerous to mention, have provided me with information. I gratefully acknowledge their contributions.

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