Upgrade of the LHCb Vertex Locator

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On behalf of the LHCb VELO Upgrade Group
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- Forward detector designed to search for New Physics by studying CP violation and rare decays of beauty and charm particles at the LHC.

- Excellent Vertex & Momentum resolution, particle ID and flexible triggering.
**VELO Detector Overview**

**SENSORS**
- 300 µm Silicon 42 R and 42 Φ sensors, 2048 strips.
- Active area at 8.2 mm from Beam line.
- Certified up to 700 V Bias voltage.

**FE chip Beetle:**
- 128 analogue readout channels.
- 40 MHz clock, 1 MHz readout.
- Peaking time < 25 ns.
- S/N = 20.
- Radiation hardness > 10 Mrad.

- Operation in secondary Vacuum
- Corrugated RF foil
- Cooling by evaporated CO2

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**Stable beam**

**Injection**

**✓ Centers around the beam every fill**

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Talk by Tim Head, Performance and Radiation Damage Effects in the LHCb Vertex Locator
Physics goal:
No deviation observed from the Standard Model, more statistics need.

- LHCb runs at ~20% of ATLAS & CMS Luminosity, may accept more from LHC.
- LHCb runs at double Luminosity as been designed.

As part of LHCb tracker the VELO should be modified to cope with Luminosity $2 \times 10^{33}$ cm$^{-2}$ s$^{-1}$

- Readout whole detector at 40 MHz clock every bunch crossing, 25 ns
- Fully software trigger, no L0 trigger
- Completely new Front End ASIC
- Pixels instead of strips, give faster pattern recognition
- Active area at 5.1 mm from Beam line
- New microchannel cooling system
- New thinned RF foil
- Radiation hardness up to 400 Mrad (10 years)

All these points should provide the desired resolution and tracking as well as the necessary data rate.
Full detector consists of 26 stations.
Station consists of two L-shape modules, one on each side of the beam.
Varying spacing along the beam, minimum 24 mm between stations.
Geometrical efficiency > 99 %.
Total active area \( \sim 1240 \text{ cm}^2 \).
Upgrade in details I, Sensors

- Planar Silicon n-in-n or n-in-p.
- 200 micron thickness.
- Tile for 3 VeloPix chips: ~ 43 x 14 mm
- 55 x 55 micron pixel size.
- Non homogeneous design of Guard rings:
  - Fluence difference factor of ~40 on hot and on far ends.
  - Bias Voltage ~1000V at the end of lifetime, 50 fb⁻¹
  - Guard ring width ~450 micron.
- Possible vendors – Micron/Hamamatsu
24 ASIC mounted on two L-shape modules.

Four sensor tiles, two on each sides of substrate.

Power and Readout traces on Kapton flex.

Silicon substrate with etched micro-channels for evaporated CO2 cooling.

41 Megapixels in total.
New **VeloPix** ASIC based on the Medipix family (TimePix, TimePix3).

- TimePix3 ASIC is used as prototype for Beam tests by VELO group.
- VeloPix designed by CERN medipix group and Nikhef.
- Matrix of 256 x 256 pixels, ~14 x 14 mm² active area.
- 130 nm CMOS technology, radiation hardness up to 400 MRad.
- First submission in summer 2014, production in 2015.

**VeloPix features:**

- Data driven readout, hits immediately transferred to the output.
- [4 x 2] pixels with fixed boundaries compose Super-pixel to reduce the data volume.
  Typical cluster size is 2-4, removes duplicated address and timestamp.
- Time stamp and label of output data (BCID).
- Binary readout.
- Time-of-Arrival and Time-over-Threshold measurements, all hits are ToA, but ToT available at low rate.
- Output bandwidth 13 Gbit/s; 4 links @ 5 Gbit/s.
- Zero suppressed data.
- Fast front-end: Timewalk < 25 ns.
- Power dissipation < 3 Watts per chip @ 1.5V (1.5 W/cm²).
- Expected threshold ~1000 e-.
Upgrade in details IV, Data acquisition

- Differential copper link from ISIC (Kapton ~1 m) inside of vacuum tank.
- Vacuum feed through.
- Electrical to optical conversion outside of vacuum tank.
- Optical link ~300 m long.
- 4 mezzanines with powerful FPGA (ALTERA, Stratix-V).
- DAQ module TELL40, common for LHCb, ATCA standard.
- 12 x 10 Gigabit Ethernet outputs.
- CPU farm.

Data flow of whole VELO ~ 2.5 Terabit/s

- Packet receiver
- Time ordering
- Event buffering
- Packet decoding

TEL40 (ATCA)

- max. 24 optical links
- max. 24 optical links
- max. 24 optical links
- max. 24 optical links

Earth surface

CPU farm

Data flow:

- differential copper links
- differential copper links
- differential copper links
- differential copper links
**Key Features**

- Method: evaporated CO$_2$ flow via **microchannels etched in Silicon substrate**.
- Bring the coolant directly to power dissipation areas.
- Keep the sensors at -20 °C to reduce the radiation damage.
- Good uniformity of material in sensitive region, **no CTE difference**. Less material.
- Channel cross section 200 x 120 $\mu$m$^2$.
- Detectors in vacuum, hence leakage/breakage is a serious concern.

**R & D** started in summer 2012. After 1.5 year efforts we have **achieved**:

- Required operational pressure ~15 Bar at -30 °C, and ~60 Bar at room temperature.
- Withstand on safety limits of 150 Bar.
- Stress test of samples at ~700 Bar.
- Thermal and pressure cycling long term tests (-40 .. +40 °C, 0 .. 200 Bar).

First prototype

Looks promising

Microchannel cooling connector

Microchannel Silicon substrates

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**Requirements:**

- Separates Accelerator (10^{-9} mbar) and VELO (10^{-7} mbar) vacua.
- Vacuum tight, leakage < 10^{-9} mbar l/s.
- Electrically conductive: guides beam mirror current.
- Low mass: located at R=3.5 mm from beam line.
- Thermally stable and thermally conductive.

**Material and fabrication:**

- Aluminum (AlBeMet) <300 \mu m thick top foil, 500 \mu m thick walls.
- Milled from solid block of Aluminum.
- Local chemical thinning with NaOH after milling, *under discussion.*

30% of real length
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<th>25 ns</th>
<th>-</th>
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<td>$\mathcal{L}$ Instant</td>
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<td>3 - 4 x 10^{32}</td>
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<td>$4 x 10^{32}$</td>
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<tr>
<td>$\mathcal{L}$ Integrated</td>
<td>3 fb^{-1}</td>
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<td>5 - 7 fb^{-1}</td>
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VELOPIX installation in 2019
Luminosity $2 \times 10^{33}$ (factor of 5 increase vs current VELO)
No L0 trigger, all data to CPU farm
Planar silicon pixels, 55 x 55 $\mu$m$^2$
Active area at 5.1 mm from the beam
Fluence at hot end of sensor $8 \times 10^{15}$ MeV n$_{eq}$/cm$^2$
VELOPIX ASIC based on Medipix Family, 130 nm CMOS
Data flow: 20 Gbit/s output bandwidth per ASIC
Evaporative CO$_2$ cooling in Silicon microchannel substrate
300 $\mu$m thick RF-box milled from solid block of Aluminum

Upgrade is going well and on schedule, many novel techniques
Total Material of Upgrade VELO as described in TDR
Artist impression of installed upgraded VELO detector, produced by Nikhef Mechanical Engineering Department.
 VELOPIX Expectations

IPx resolution for long tracks for VELO Upgrade compared to expected performance of current VELO design in upgrade conditions, as described in TDR.